1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

MLB-S, X2257

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
3	0036004128	ENGINEERING RELEASED	2022-06-10

LAST_MODIFICATION=Fri Jun 10 11:19:41 2022

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-08156	1	SCHEM,MLB-S,X2527	SCH	CRITICAL	SCH
820-02890	1	PCBF,MLB-S,X2527	PCB	CRITICAL	PCB

CHECKPLUS RULE CONFIGURATIONS	
CHECK VOLTAGE IC - LEVELS	?
PCB TESTPOINTS ALLOWED	YES
CHECK FATAL PACK_OPTION	YES
CHECK RESISTOR VOLTAGE	NO

SCHEM, MLB, T728

DRAWING TITLE: SCHEM,MLB-S,X2527

Apple Inc.

DRAWING NUMBER: 051-08156 | SIZE: D
REVISION: 3.0.0
BRANCH: evt-1
PAGE: 1 OF 700
SHEET: 1 OF 159

SGA MLB Support Pages

19,51-53,84,92,120,130-132,135-141,145,156,162-163,166,170,179,196
230,234,236,248,249,252-255,266-268,270-271,294
400-402,405,410,500-503,998

Unfortunatly, designCompiler doesn't support multiple table entries of the same design, leading to the extra-large table entry below

Reference Design Pages Ref designs common with SGA MLB are synced from there

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/ SOFT	SYNC_DATE/TIME
T585	REF_SOC_H14S	5,6,8,10,12,14,16,20,23,25,27,29,31,33,35,37,39,41,42	0.16.0	S	2022_05_17_10:51:09
T585	REF_VR_ICEMAN	57,58	1.46.0	S	2022_05_17_10:50:54
T585	REF_VR_AUSTRINGER	93-95	0.34.0	S	2022_05_17_10:49:05
T585	REF_CLVR_MIRABEAU	101-102,106	0.30.0	S	2022_05_17_10:49:58
T585	REF_PMIC_MAVERICKS_H14	76-84,403-404	0.36.0	S	2022_05_17_10:49:20
T585	REF_MAGSAFE_ACE2	52-56,59	0.113.2	S	2022_05_17_10:51:21
T585	REF_SE_EOS	50	0.2.2	S	2022_05_17_10:48:13
T585	REF_VR_5V_TPS62130	122	0.20.0	S	2022_05_17_10:52:05
T585	REF_USBC_LFKA_3PRT_ACE2	147-149,150-157,160,162-164,166-167	0.55.0	S	2022_05_17_10:52:21
T585	REF_CIO_RDVR_COLUMBUS	181,182	0.12.0	H	2022_05_24_13:48:38
T585	REF_USBC_VR_LT8642_1	158	0.11.0	S	2022_05_17_10:49:29
T585	REF_USBC_VR_TPS62180	168	0.9.0	S	2022_05_17_10:51:57
T585	REF_IMU_SOVEREIGN	144	0.15.0	S	2022_05_17_10:51:48
T585	REF_HDMI_COBRA	175-179	0.46.0	S	2022_05_17_10:51:40
T585	REF_SDCARD_GL9755_V2	195-198	0.11.0	S	2022_05_17_10:51:30
T585	REF_WIRELESS_WILLAMETTE	200-201	0.28.0	S	2022_05_31_15:32:47
T585	REF_STORAGE_S5E_MARK2	220-229	0.16.0	S	2022_05_17_10:50:09
T585	REF_PANELPWR_2D	237	0.8.0	S	2022_05_17_10:50:18
T585	REF_BLC_LUXE	238	0.35.0	S	2022_05_17_10:50:27
T585	REF_SECDIS_LAS_H14X	242	0.3.0	S	2022_05_17_10:48:56
T585	REF_SECDIS_H14X	243	0.6.0	S	2022_05_17_10:49:37
T585	REF_CODEC_CARLOW	245	1.6.0	S	2022_05_17_10:50:45
T585	REF_SPKRAMP_SN012776	246,247	3.8.0	S	2022_05_17_10:49:46
T585	REF_BLC_BEN_KBD_ONLY	250	0.7.0	S	2022_05_17_10:50:35
T585	REF_IPD	251-254	0.30.0	S	2022_05_17_10:48:31
T585	REF_VR_RT13_PORTABLES	159,169	0.13.0	S	2022_05_24_12:01:21

Original Ref Design Name Table Entries

```
!DEF  TBL_HIER_DESIGN_NAME=REF_SE_CERES                !DEF  TBL_HIER_DESIGN_PAGES=50
!DEF  TBL_HIER_DESIGN_NAME=REF_MAGSAFE_ACE2 Hard       !DEF  TBL_HIER_DESIGN_PAGES=54,55,56
!DEF  TBL_HIER_DESIGN_NAME=REF_VR_ICEMAN_HP            !DEF  TBL_HIER_DESIGN_PAGES=57,58
!DEF  TBL_HIER_DESIGN_NAME=REF_PMIC_MAVERICKS          !DEF  TBL_HIER_DESIGN_PAGES=77-83,403,404
!DEF  TBL_HIER_DESIGN_NAME=REF_VR_VIPER                !DEF  TBL_HIER_DESIGN_PAGES=93-96
!DEF  TBL_HIER_DESIGN_NAME=REF_CLVR_MONACO             !DEF  TBL_HIER_DESIGN_PAGES=101-105
!DEF  TBL_HIER_DESIGN_NAME=REF_VR_5V_TPS62130          !DEF  TBL_HIER_DESIGN_PAGES=122
!DEF  TBL_HIER_DESIGN_NAME=REF_IMU_COBOL               !DEF  TBL_HIER_DESIGN_PAGES=144
!DEF  TBL_HIER_DESIGN_NAME=REF_USBC_ACE2 Hard          !DEF  TBL_HIER_DESIGN_PAGES=150-155,157,160,164,167
!DEF  TBL_HIER_DESIGN_NAME=REF_CIO_RDVR_COLUMBUS       !DEF  TBL_HIER_DESIGN_PAGES=158
!DEF  TBL_HIER_DESIGN_NAME=REF_USBC_VR_LT8642          !DEF  TBL_HIER_DESIGN_PAGES=168
!DEF  TBL_HIER_DESIGN_NAME=REF_USBC_VR_TPS62180        !DEF  TBL_HIER_DESIGN_PAGES=169
!DEF  TBL_HIER_DESIGN_NAME=REF_HDMI_MADEA              !DEF  TBL_HIER_DESIGN_PAGES=175-178
!DEF  TBL_HIER_DESIGN_NAME=REF_SDCARD_GL9755           !DEF  TBL_HIER_DESIGN_PAGES=195,197-199
!DEF  TBL_HIER_DESIGN_NAME=REF_WIRELESS_TYPHOON        !DEF  TBL_HIER_DESIGN_PAGES=200,201
!DEF  TBL_HIER_DESIGN_NAME=REF_STORAGE_S5E             !DEF  TBL_HIER_DESIGN_PAGES=220-229
!DEF  TBL_HIER_DESIGN_NAME=REF_PANELPWR_2D             !DEF  TBL_HIER_DESIGN_PAGES=237
!DEF  TBL_HIER_DESIGN_NAME=REF_BLC_LUXE                !DEF  TBL_HIER_DESIGN_PAGES=238,239
!DEF  TBL_HIER_DESIGN_NAME=REF_SECDIS_LAS              !DEF  TBL_HIER_DESIGN_PAGES=242
!DEF  TBL_HIER_DESIGN_NAME=REF_SECDIS_SAK              !DEF  TBL_HIER_DESIGN_PAGES=243
!DEF  TBL_HIER_DESIGN_NAME=REF_CODEC_CARLOW            !DEF  TBL_HIER_DESIGN_PAGES=245
!DEF  TBL_HIER_DESIGN_NAME=REF_SPKRAMP_SN012776        !DEF  TBL_HIER_DESIGN_PAGES=246,247
!DEF  TBL_HIER_DESIGN_NAME=REF_BLC_BEN_KBD_ONLY        !DEF  TBL_HIER_DESIGN_PAGES=250
!DEF  TBL_HIER_DESIGN_NAME=REF_KBD_34PIN Hard          !DEF  TBL_HIER_DESIGN_PAGES=251
!DEF  TBL_HIER_DESIGN_NAME=REF_MESA_SUPPORT Hard       !DEF  TBL_HIER_DESIGN_PAGES=256
!DEF  TBL_HIER_DESIGN_NAME=REF_MESA_BACKLIGHT          !DEF  TBL_HIER_DESIGN_PAGES=257
```

Pages Not Synced from Anywhere

Page Name	Reasoning
CSA 004: PD Parts	Unique PD design for SOC region
CSA 019: SOC Shared Support	Extra content relative to SGA
CSA 021: SOC Project Support	Extra content relative to SGA
CSA 120: CLVR Support	Extra CLVRs compared to SGA MLB
CSA 402: CLVR Aliases	Extra CLVRs compared to SGA MLB
CSA 407: Signal Aliases 3	Signals NC'd on SGA are connected on CGA
CSA 408: NC Aliases	Signals NC'd on SGA are connected on CGA
CSA 420: SGA/CGA Aliases	Fix net name diffs between SGA and CGA
CSA 60x: BOM Configuration	Each design has unique APNs
CSA 7xx: Pack Options	Unique combination of pack options

Reference Design Overrides

Page Name	Changes made
CSA 101: Monaco 0	
CSA 102: Monaco 1	
CSA 103: Monaco 2	
CSA 104: Monaco 3	Fix missing MAKE_BASE
CSA 105: Monaco 4	Fix missing MAKE_BASE

Old MLB sync pages

22,50-51,84,92,122,130-132,135-141,144-145,150-158,160,162-164,166-170,175-179,195-201,220-230,234,236-239,242,245-257,266-268,270-271,294,400-401,405-406,410,500,610,998

!DEF TBL_PINDELAY_REFDES=U0600 !DEF TBL_PINDELAY_CSVFILE_NAME=CGA_PINDELAY_2020-05-01.CSV

Pin delay table removed due to pin delay import error causing fatal checkplus error
Recommend adding the table entry back once error is resolved

SYNC_DATE=

PAGE TITLE
REFERENCE DESIGN TABLE

Apple Inc.

DRAWING NUMBER 051-08156 | SIZE D
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BRANCH evt-1
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SHEET 2 OF 159

MAGSAFE BOSS

BS0450
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS0451
2.7X1.8R-1.4ID-1.7H-SM
860-01714

L USBC BOSS

BS04F0
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04F1
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04F2
2.7X1.8R-1.4ID-1.7H-SM
860-01714

R USBC BOSS

BS04G0
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04G1
2.7X1.8R-1.4ID-1.7H-SM
860-01714

ANTENNA BOSS

BS04L0
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04L1
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04L2
BOSS-2.9X4.7-2.1H-SM
860-01841

DISP, CAM BOSS

BS04P0
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04P1
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BKLT BOSS

BS04P2
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04P3
2.7X1.8R-1.4ID-1.7H-SM
860-01714

LAS BOSS

BS04R0
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04R1
2.7X1.8R-1.4ID-1.7H-SM
860-01714

L SPEAKER BOSS

BS04R2
2.7X1.8R-1.4ID-1.7H-SM
860-01714

R SPEAKER BOSS

BS04R3
2.7X1.8R-1.4ID-1.7H-SM
860-01714

AUDIO JACK BOSS

BS04R4
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04R5
2.7X1.8R-1.4ID-1.7H-SM
860-01714

TRACKPAD BOSS

BS04T0
3.4OD1.75ID-2.01H-SM
860-01805

BS04T1
3.4OD1.75ID-2.01H-SM
860-01805

TOUCHID BOSS

BS04T2
2.7X1.8R-1.34H-SM
860-01936

BS04T3
2.7X1.8R-1.34H-SM
860-01936

DFM DUMMY CAPS

C0400 15UF 20% 2.5V X6S 0402-1
C0401 15UF 20% 2.5V X6S 0402-1
C0402 15UF 20% 2.5V X6S 0402-1

BUMPERS

860-01715

BM0400 2.8OD1.2ID-2.0H-SM
BM0401 2.8OD1.2ID-2.0H-SM
BM0402 2.8OD1.2ID-2.0H-SM
BM0403 2.8OD1.2ID-2.0H-SM
BM0404 2.8OD1.2ID-2.0H-SM
BM0405 2.8OD1.2ID-2.0H-SM
BM0406 2.8OD1.2ID-2.0H-SM
BM0410 2.8OD1.2ID-2.0H-SM
BM0413 2.8OD1.2ID-2.0H-SM
BM0407 2.8OD1.2ID-4.6H-SM
BM0408 2.8OD1.2ID-4.6H-SM

BOTTOM BUMPERS

860-01839

BM0430 2.8OD1.2ID-4.0H-SM
BM0431 2.8OD1.2ID-4.0H-SM
BM0432 2.8OD1.2ID-4.0H-SM
BM0412 2.8OD1.2ID-4.0H-SM
BM0411 2.8OD1.2ID-4.0H-SM
BM0433 2.8OD1.2ID-4.0H-SM
BM0434 2.8OD1.2ID-4.0H-SM
BM0435 2.8OD1.2ID-4.0H-SM
BM0436 2.8OD1.2ID-4.0H-SM
BM0437 2.8OD1.2ID-4.0H-SM
BM0438 2.8OD1.2ID-4.0H-SM

POGO PINS

870-12862

PG0400 POGO-2.3OD-4.88-LOW FORCE SM
PG0401 POGO-2.3OD-4.88-LOW FORCE SM
PG0402 POGO-2.3OD-4.88-LOW FORCE SM
PG0403 POGO-2.3OD-4.88-LOW FORCE SM
PG0404 POGO-2.3OD-4.88-LOW FORCE SM
PG0405 POGO-2.3OD-4.88-LOW FORCE SM
PG0406 POGO-2.3OD-4.88-LOW FORCE SM
PG0407 POGO-2.3OD-4.88-LOW FORCE SM
PG0408 POGO-2.3OD-4.88-LOW FORCE SM
PG0409 POGO-2.3OD-4.88-LOW FORCE SM
PG0410 POGO-2.3OD-4.88-LOW FORCE SM

SHIELD CAN SLOTS

998-04440

SH0400 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0401 TH-NSP SL-1.2X0.4-1.5X0.7	Left 2 Burnside USBC Ports
SH0402 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0403 TH-NSP SL-1.2X0.4-1.5X0.7	Left Viper
SH0404 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0407 TH-NSP SL-1.2X0.4-1.5X0.7	Right Viper
SH0405 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0406 TH-NSP SL-1.2X0.4-1.5X0.7	Columbus Retimer
SH0408 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0409 TH-NSP SL-1.2X0.4-1.5X0.7	SDCARD
SH0410 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0411 TH-NSP SL-1.2X0.4-1.5X0.7	Right 1 Burnside USBC Port
SH0412 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0413 TH-NSP SL-1.2X0.4-1.5X0.7	HDMI Madea HDMI Madea
SH0414 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0415 TH-NSP SL-1.2X0.4-1.5X0.7	North Maverick Slave
SH0416 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0417 TH-NSP SL-1.2X0.4-1.5X0.7	Iceman
SH0418 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0419 TH-NSP SL-1.2X0.4-1.5X0.7	Top Left Viper
SH0422 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0423 TH-NSP SL-1.2X0.4-1.5X0.7	Top Right Viper

BOTTOM 1 TP TP-P4 WSHR01
BOTTOM 1 TP TP-P4 WSHR02
BOTTOM 1 TP TP-P4 WSHR03
BOTTOM 1 TP TP-P4 WSHR04
TOP 1 TP TP-P4 SOCFNC01

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-34812	1	Left 2 Burnside USBC Ports	SH0400	CRITICAL	
806-34814	1	Left Viper	SH0402	CRITICAL	
806-34815	1	Right Viper	SH0404	CRITICAL	
806-36335	1	Top Left Viper	SH0418	CRITICAL	
806-36336	1	Top Right Viper	SH0422	CRITICAL	
806-34809	1	Columbus Retimer Fence	SH0405	CRITICAL	
806-34667	1	SDCARD Fence	SH0408	CRITICAL	
806-34811	1	Right 1 Burnside USBC Port Fence	SH0410	CRITICAL	
806-34810	1	HDMI Cobrs Fence	SH0412	CRITICAL	
806-34685	1	North Maverick Slave Fence	SH0414	CRITICAL	
806-34813	1	Iceman Fence	SH0416	CRITICAL	
806-36016	1	SOC Fence	SOCFNC01	CRITICAL	
860-01926	4	WASHER, SMT	WSHR01,WSHR02,WSHR03,WSHR04	CRITICAL	

PAGE TITLE
PD PARTS

Apple Inc.

DRAWING NUMBER 051-08156
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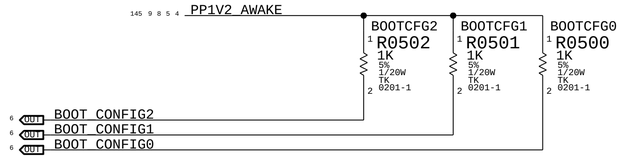
BOOT CONFIG

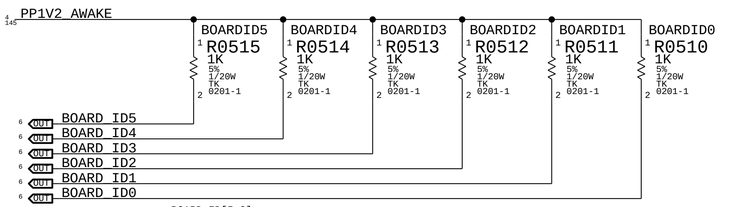


BOOT_CONFIGFG[2:0]	MODE
000	SPI1 NOR (12MHZ)
001	SPI1 NOR (12MHZ) TEST
010	SPI0 NAND (12MHZ)
011	SPI0 NAND (12MHZ) TEST
POR ---> 100	SPI1 NOR (40MHZ)
101	SPI1 NOR (40MHZ) TEST
110	SPI1 NOR (6MHZ)
111	SPI1 NOR (6MHZ) TEST

SW READ FLOW

1. SET GPIO AS INPUT
2. ENABLE IPD
3. WAIT 100 MILLISECONDS
4. READ VALUES
5. DISABLE GPIOS

BOARD ID

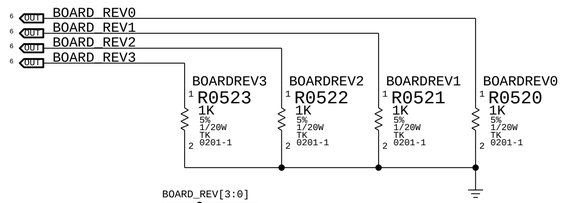


BOARD_ID[5:0]	
000000	RHODESREF
000001	RHODESSUIREF
00001X	J474
00010X	J414
00011X	J416

HW READ FLOW

- HARDWARE SAMPLED BEFORE AP TAKEN OUT OF RESET
- SEE CHIPPADS INTEGRATION SPEC, SECTION 2.4.7

BOARD REV



BOARD_REV[3:0]	
0000	TEMP
0001	TEMP
0010	TEMP
0011	TEMP
0100	TEMP
0101	TEMP
0110	TEMP
0111	TEMP
1000	TEMP
1001	TEMP
1010	TEMP
1011	TEMP
1100	TEMP
1101	TEMP
1110	TEMP
1111	TEMP

SW READ FLOW

- SAMPLED IN IBOOT ONCE AP IS RUNNING

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: CONFIG STRAPS

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REVISION 3.0.0
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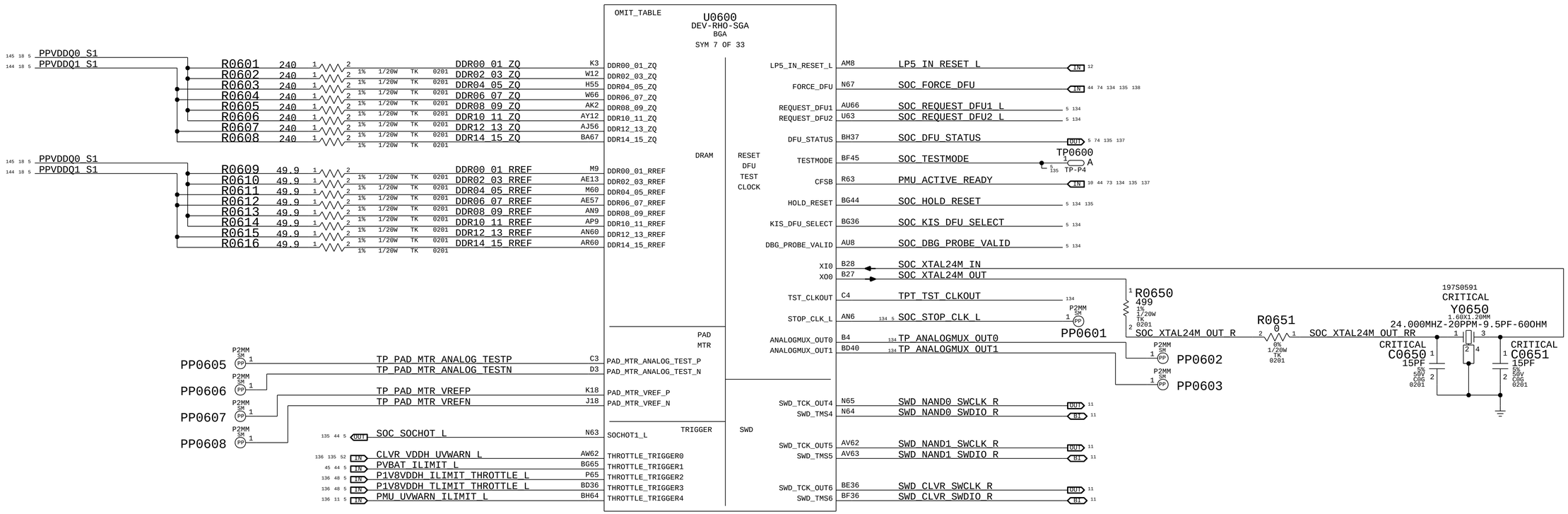

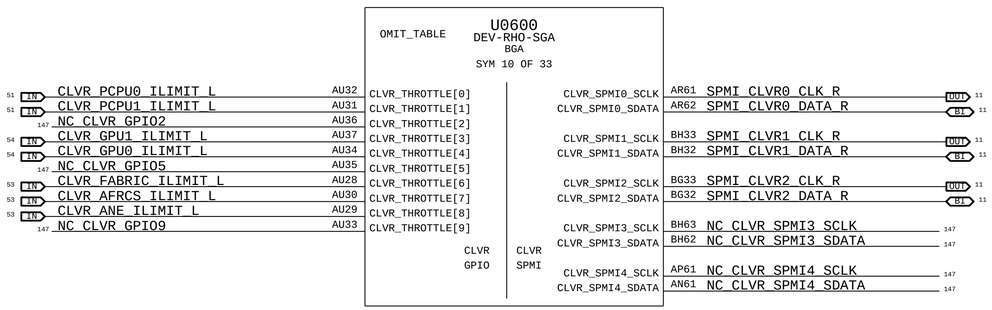

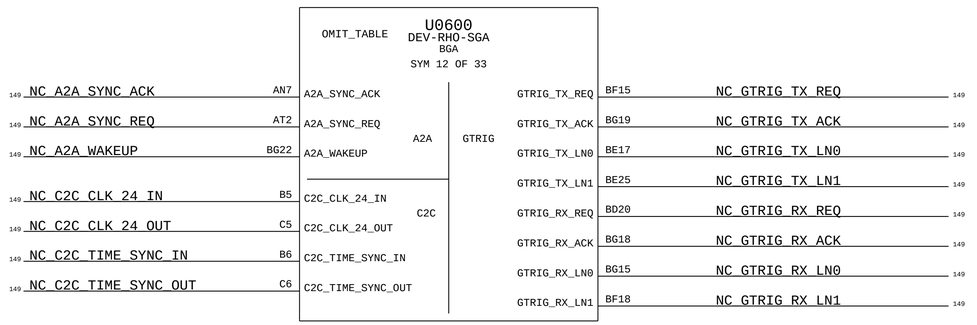

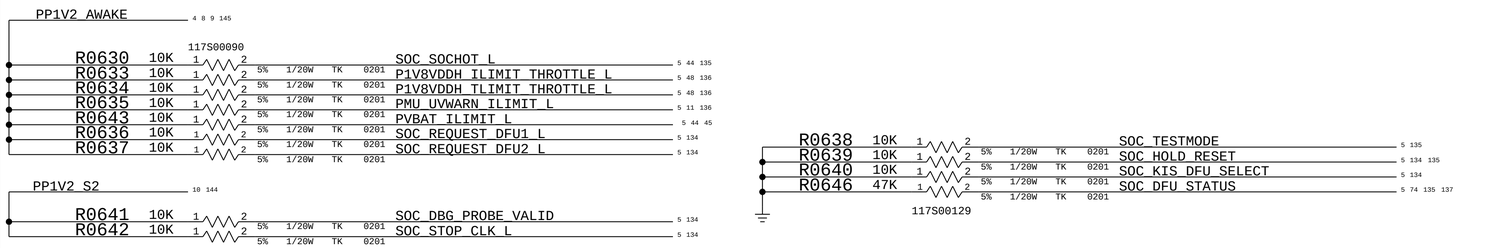

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: RESETS, CLOCKS, SWD

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DRAWING NUMBER	051-08156
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REVISION	3.0.0
BRANCH	evt-1
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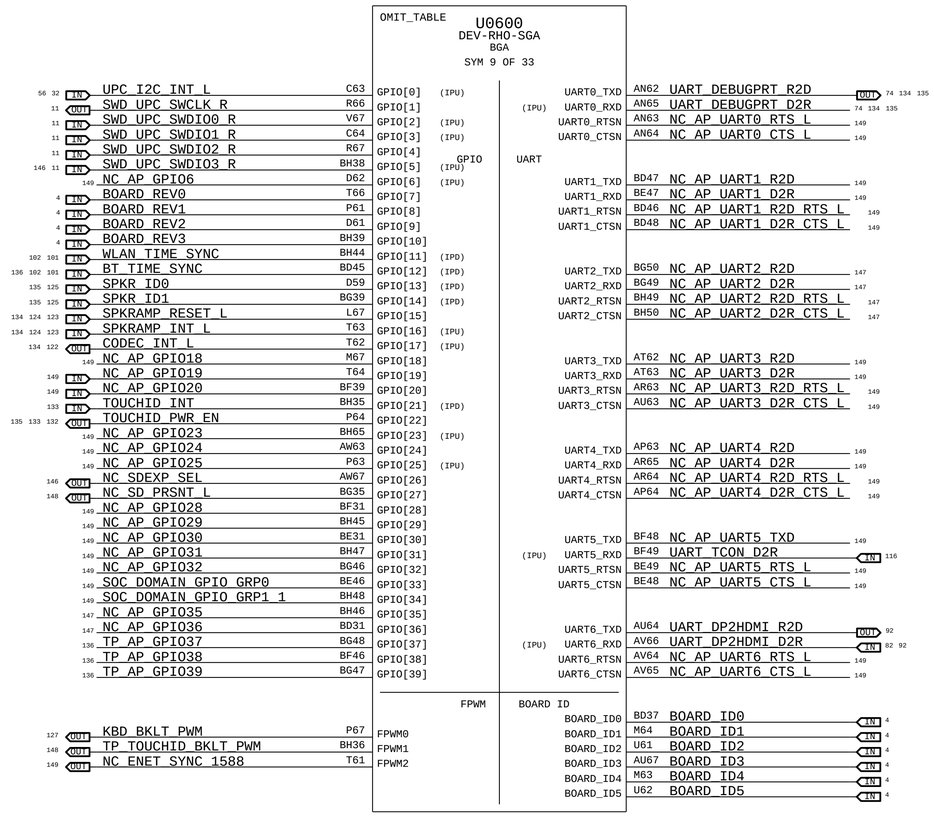
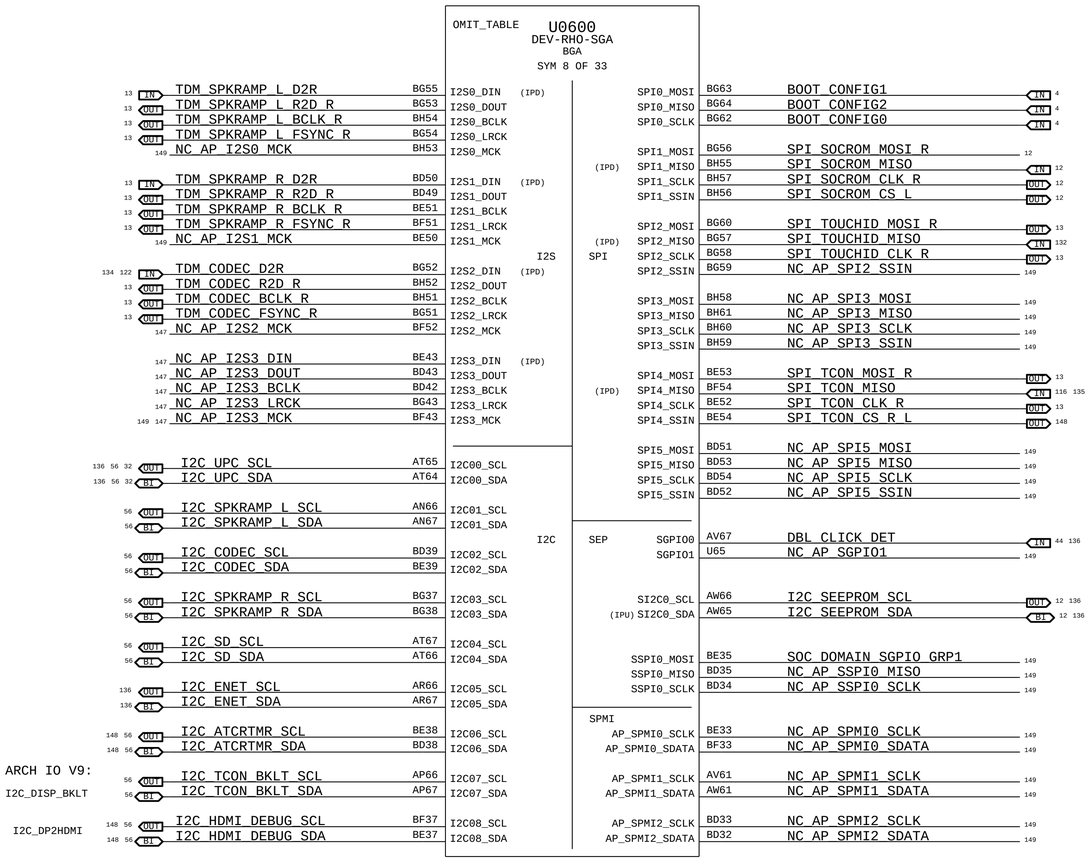
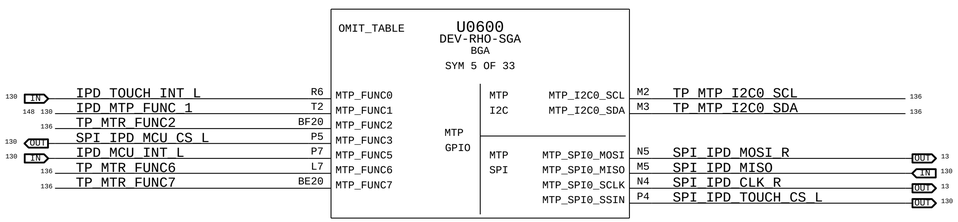




ARCH IO V9:
I2C_DISP_BKLT
I2C_DP2HDMI



BOM_COST_GROUP=SOC

PAGE TITLE
SOC: GPIO, I2C, I2S, SPI, UART

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REVISION 3.0.0
BRANCH evt-1
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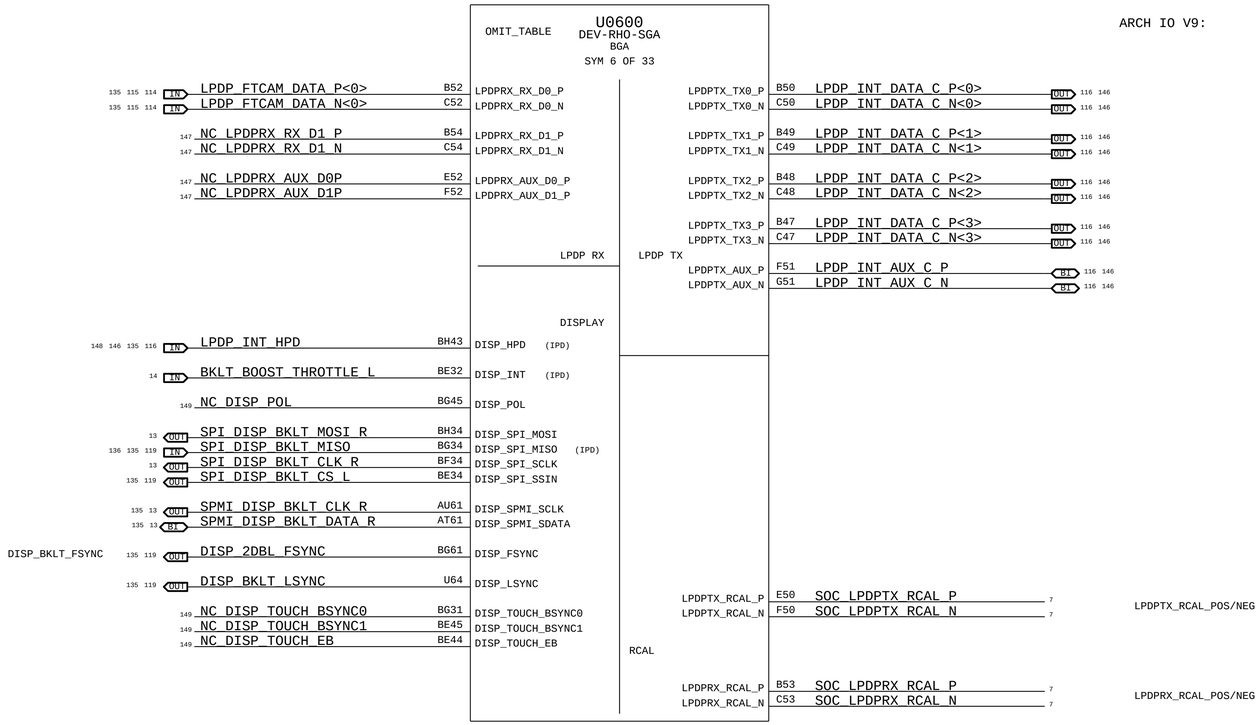
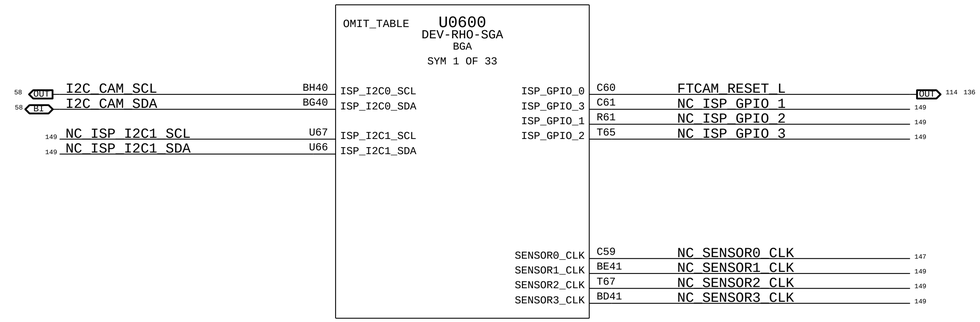
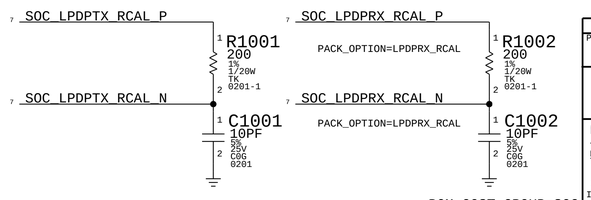
ARCH IO V9:



ARCH IO V9:





PAGE TITLE

SOC: CONFIG STRAPS

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ARCH IO V9:

U0600
DEV-RHO-SGA
BGA
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OMIT_TABLE

PCIE_NAND0_R2D_C_P<0>	E38	ST0_PCIE_TX0_P	ST0 PCIE PORT 0	ST1 PCIE PORT 0	ST1_PCIE_TX0_P	E42	PCIE_NAND1_R2D_C_P<0>
PCIE_NAND0_R2D_C_N<0>	F38	ST0_PCIE_TX0_N			ST1_PCIE_TX0_N	F42	PCIE_NAND1_R2D_C_N<0>
PCIE_NAND0_D2R_P<0>	B38	ST0_PCIE_RX0_P			ST1_PCIE_RX0_P	B42	PCIE_NAND1_D2R_P<0>
PCIE_NAND0_D2R_N<0>	C38	ST0_PCIE_RX0_N			ST1_PCIE_RX0_N	C42	PCIE_NAND1_D2R_N<0>
PCIE_CLK100M_NAND0_0_1_P	J41	ST0_PCIE_REF_CLK0_1_P			ST1_PCIE_REF_CLK0_1_P	J45	PCIE_CLK100M_NAND1_0_1_P
PCIE_CLK100M_NAND0_0_1_N	K41	ST0_PCIE_REF_CLK0_1_N			ST1_PCIE_REF_CLK0_1_N	K45	PCIE_CLK100M_NAND1_0_1_N
NAND0_CLKREQ0_L	BH42	ST0_PCIE_CLKREQ0_L			ST1_PCIE_CLKREQ0_L	P66	NAND1_CLKREQ0_L
PCIE_NAND0_R2D_C_P<1>	F39	ST0_PCIE_TX1_P	ST0 PCIE PORT 1	ST1 PCIE PORT 1	ST1_PCIE_TX1_P	F43	PCIE_NAND1_R2D_C_P<1>
PCIE_NAND0_R2D_C_N<1>	G39	ST0_PCIE_TX1_N			ST1_PCIE_TX1_N	G43	PCIE_NAND1_R2D_C_N<1>
PCIE_NAND0_D2R_P<1>	C39	ST0_PCIE_RX1_P			ST1_PCIE_RX1_P	C43	PCIE_NAND1_D2R_P<1>
PCIE_NAND0_D2R_N<1>	D39	ST0_PCIE_RX1_N			ST1_PCIE_RX1_N	D43	PCIE_NAND1_D2R_N<1>
NC_PCIE_CLK100M_NAND0_1P	H40	ST0_PCIE_REF_CLK1_P			ST1_PCIE_REF_CLK1_P	H44	NC_PCIE_CLK100M_NAND1_1P
NC_PCIE_CLK100M_NAND0_1N	J40	ST0_PCIE_REF_CLK1_N			ST1_PCIE_REF_CLK1_N	J44	NC_PCIE_CLK100M_NAND1_1N
NAND0_CLKREQ1_L	N62	ST0_PCIE_CLKREQ1_L			ST1_PCIE_CLKREQ1_L	P62	NAND1_CLKREQ1_L
PCIE_NAND0_R2D_C_P<2>	E40	ST0_PCIE_TX2_P	ST0 PCIE PORT 2	ST1 PCIE PORT 2	ST1_PCIE_TX2_P	E44	PCIE_NAND1_R2D_C_P<2>
PCIE_NAND0_R2D_C_N<2>	F40	ST0_PCIE_TX2_N			ST1_PCIE_TX2_N	F44	PCIE_NAND1_R2D_C_N<2>
PCIE_NAND0_D2R_P<2>	B40	ST0_PCIE_RX2_P			ST1_PCIE_RX2_P	B44	PCIE_NAND1_D2R_P<2>
PCIE_NAND0_D2R_N<2>	C40	ST0_PCIE_RX2_N			ST1_PCIE_RX2_N	C44	PCIE_NAND1_D2R_N<2>
PCIE_CLK100M_NAND0_2_3_P	J39	ST0_PCIE_REF_CLK2_3_P			ST1_PCIE_REF_CLK2_3_P	J43	PCIE_CLK100M_NAND1_2_3_P
PCIE_CLK100M_NAND0_2_3_N	K39	ST0_PCIE_REF_CLK2_3_N			ST1_PCIE_REF_CLK2_3_N	K43	PCIE_CLK100M_NAND1_2_3_N
NAND0_CLKREQ2_L	BG42	ST0_PCIE_CLKREQ2_L			ST1_PCIE_CLKREQ2_L	B60	NAND1_CLKREQ2_L
PCIE_NAND0_R2D_C_P<3>	F41	ST0_PCIE_TX3_P	ST0 PCIE PORT 3	ST1 PCIE PORT 3	ST1_PCIE_TX3_P	F45	PCIE_NAND1_R2D_C_P<3>
PCIE_NAND0_R2D_C_N<3>	G41	ST0_PCIE_TX3_N			ST1_PCIE_TX3_N	G45	PCIE_NAND1_R2D_C_N<3>
PCIE_NAND0_D2R_P<3>	C41	ST0_PCIE_RX3_P			ST1_PCIE_RX3_P	C45	PCIE_NAND1_D2R_P<3>
PCIE_NAND0_D2R_N<3>	D41	ST0_PCIE_RX3_N			ST1_PCIE_RX3_N	D45	PCIE_NAND1_D2R_N<3>
NC_PCIE_CLK100M_NAND0_3P	H38	ST0_PCIE_REF_CLK3_P			ST1_PCIE_REF_CLK3_P	H42	NC_PCIE_CLK100M_NAND1_3P
NC_PCIE_CLK100M_NAND0_3N	J38	ST0_PCIE_REF_CLK3_N			ST1_PCIE_REF_CLK3_N	J42	NC_PCIE_CLK100M_NAND1_3N
NAND0_CLKREQ3_L	B59	ST0_PCIE_CLKREQ3_L			ST1_PCIE_CLKREQ3_L	N66	NAND1_CLKREQ3_L
NAND0_PCIE_RESET_L	BF42	ST0_PCIE_PERST_L			ST1_PCIE_PERST_L	B61	NAND1_PCIE_RESET_L
SOC_ST0_PCIE_RCAL_POS/NEG							
SOC_ST0_PCIE_RCAL_P	E47	ST0_PCIE_RCAL_P	RCAL	NAND SUPPORT	NAND_SYS_CLK0	L61	NAND0_CLK24M_R
SOC_ST0_PCIE_RCAL_N	F47	ST0_PCIE_RCAL_N			NAND_SYS_CLK1	M66	NAND1_CLK24M_R
SOC_ST1_PCIE_RCAL_POS/NEG							
SOC_ST1_PCIE_RCAL_P	F48	ST1_PCIE_RCAL_P			SSD_BFH	B62	NAND_BFH
SOC_ST1_PCIE_RCAL_N	G48	ST1_PCIE_RCAL_N			SSD_RESET0_L	BE42	SOC_DOMAIN_HGPIO_GRP0_0
					SSD_RESET1_7_L	L62	SOC_DOMAIN_HGPIO_GRP0_1

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PCIE_WLBT_R2D_C_P	E34	GP_PCIE_TX0_P	GP PCIE PORT 0	GP PCIE PORT 2	GP_PCIE_TX2_P	E36	NC_GP_PCIE_TX2_P
PCIE_WLBT_R2D_C_N	F34	GP_PCIE_TX0_N			GP_PCIE_TX2_N	F36	NC_GP_PCIE_TX2_N
PCIE_WLBT_D2R_P	B34	GP_PCIE_RX0_P			GP_PCIE_RX2_P	B36	NC_GP_PCIE_RX2_P
PCIE_WLBT_D2R_N	C34	GP_PCIE_RX0_N			GP_PCIE_RX2_N	C36	NC_GP_PCIE_RX2_N
PCIE_CLK100M_WLBT_P	J35	GP_PCIE_REF_CLK0_P			GP_PCIE_REF_CLK2_P	H34	NC_GP_PCIE_REF_CLK2_P
PCIE_CLK100M_WLBT_N	K35	GP_PCIE_REF_CLK0_N			GP_PCIE_REF_CLK2_N	J34	NC_GP_PCIE_REF_CLK2_N
WLBT_CLKREQ_L	BH41	GP_PCIE_CLKREQ0_L			GP_PCIE_CLKREQ2_L	L63	NC_GP_PCIE_CLKREQ2_L
WLBT_RESET_L	B64	GP_PCIE_PERST0_L			GP_PCIE_PERST2_L	BG41	NC_GP_PCIE_PERST2_L
PCIE_SD_UHS2_R2D_C_P	F35	GP_PCIE_TX1_P	GP PCIE PORT 1	GP PCIE PORT 3	GP_PCIE_TX3_P	F37	NC_GP_PCIE_TX3_P
PCIE_SD_UHS2_R2D_C_N	G35	GP_PCIE_TX1_N			GP_PCIE_TX3_N	G37	NC_GP_PCIE_TX3_N
PCIE_SD_UHS2_D2R_P	C35	GP_PCIE_RX1_P			GP_PCIE_RX3_P	C37	NC_GP_PCIE_RX3_P
PCIE_SD_UHS2_D2R_N	D35	GP_PCIE_RX1_N			GP_PCIE_RX3_N	D37	NC_GP_PCIE_RX3_N
PCIE_CLK100M_SD_UHS2_P	J37	GP_PCIE_REF_CLK1_P			GP_PCIE_REF_CLK3_P	H36	NC_GP_PCIE_REF_CLK3_P
PCIE_CLK100M_SD_UHS2_N	K37	GP_PCIE_REF_CLK1_N			GP_PCIE_REF_CLK3_N	J36	NC_GP_PCIE_REF_CLK3_N
SD_UHS2_CLKREQ_L	B63	GP_PCIE_CLKREQ1_L			GP_PCIE_CLKREQ3_L	M61	NC_GP_PCIE_CLKREQ3_L
SD_UHS2_RESET_L	L65	GP_PCIE_PERST1_L			GP_PCIE_PERST3_L	B65	NC_GP_PCIE_PERST3_L
SOC_GE_PCIE_RCAL_POS/NEG							
SOC_GP_PCIE_RCAL_P	F27	GP_PCIE_RCAL_P	GP RCAL				
SOC_GP_PCIE_RCAL_N	E27	GP_PCIE_RCAL_N					
NC_GE_PCIE_TX0P	E30	GE_PCIE_TX0_P	GE PCIE PORT 0	GE PCIE PORT 2	GE_PCIE_TX2_P	E32	NC_GE_PCIE_TX2P
NC_GE_PCIE_TX0N	F30	GE_PCIE_TX0_N			GE_PCIE_TX2_N	F32	NC_GE_PCIE_TX2N
NC_GE_PCIE_RX0P	B30	GE_PCIE_RX0_P			GE_PCIE_RX2_P	B32	NC_GE_PCIE_RX2P
NC_GE_PCIE_RX0N	C30	GE_PCIE_RX0_N			GE_PCIE_RX2_N	C32	NC_GE_PCIE_RX2N
NC_GE_PCIE_TX1P	F31	GE_PCIE_TX1_P	GE PCIE PORT 1	GE PCIE PORT 3	GE_PCIE_TX3_P	F33	NC_GE_PCIE_TX3P
NC_GE_PCIE_TX1N	G31	GE_PCIE_TX1_N			GE_PCIE_TX3_N	G33	NC_GE_PCIE_TX3N
NC_GE_PCIE_RX1P	C31	GE_PCIE_RX1_P			GE_PCIE_RX3_P	C33	NC_GE_PCIE_RX3P
NC_GE_PCIE_RX1N	D31	GE_PCIE_RX1_N			GE_PCIE_RX3_N	D33	NC_GE_PCIE_RX3N
NC_GE_PCIE_REF_CLKP	J33	GE_PCIE_REF_CLK_P	GE REFCLK & SUPPORT				
NC_GE_PCIE_REF_CLKN	K33	GE_PCIE_REF_CLK_N					
NC_GE_PCIE_CLKREQ_L	N61	GE_PCIE_CLKREQ_L					
NC_GE_PCIE_PERST_L	L66	GE_PCIE_PERST_L					
NC_GE_PCIE_RCALP	G28	GE_PCIE_RCAL_P	GE RCAL				
NC_GE_PCIE_RCALN	F28	GE_PCIE_RCAL_N					

PP1V2_AWAKE

117S00129

R1210	47K	5%	1/20W	TK	0201	NAND0_CLKREQ0_L	8 13 134
R1211	47K	5%	1/20W	TK	0201	NAND0_CLKREQ1_L	8 13 134
R1212	47K	5%	1/20W	TK	0201	NAND0_CLKREQ2_L	8 13 134
R1213	47K	5%	1/20W	TK	0201	NAND0_CLKREQ3_L	8 13 134
R1214	47K	5%	1/20W	TK	0201	NAND1_CLKREQ0_L	8 13 134
R1215	47K	5%	1/20W	TK	0201	NAND1_CLKREQ1_L	8 13 134
R1216	47K	5%	1/20W	TK	0201	NAND1_CLKREQ2_L	8 13 134
R1217	47K	5%	1/20W	TK	0201	NAND1_CLKREQ3_L	8 13 134
R1218	47K	5%	1/20W	TK	0201	WLBT_CLKREQ_L	8 101 102
R1219	47K	5%	1/20W	TK	0201	SD_UHS2_CLKREQ_L	8 146
R1220	47K	5%	1/20W	TK	0201	NC_GP_PCIE_CLKREQ2_L	8 147
R1221	47K	5%	1/20W	TK	0201	NC_GP_PCIE_CLKREQ3_L	8 149

117S00129

R1222	47K	5%	1/20W	TK	0201	NAND0_PCIE_RESET_L	8 103 104 105 106 134
R1223	47K	5%	1/20W	TK	0201	NAND1_PCIE_RESET_L	8 108 109 110 111 134
R1224	47K	5%	1/20W	TK	0201	WLBT_RESET_L	8 101 102 136
R1225	47K	5%	1/20W	TK	0201	SD_UHS2_RESET_L	8 146
R1226	47K	5%	1/20W	TK	0201	NC_GP_PCIE_PERST2_L	8 147
R1227	47K	5%	1/20W	TK	0201	NC_GP_PCIE_PERST3_L	8 149

PACK_OPTION=SDCARD
PACK_IGNORE=TRUE
PACK_OPTION=ENET
PACK_IGNORE=TRUE
PACK_OPTION=USBHC

NC_GE_PCIE_RCALP → R1203 200 1% 1/20W TK 0201-1 → SOC_ST0_PCIE_RCAL_P → R1200 200 1% 1/20W TK 0201-1 → SOC_ST1_PCIE_RCAL_P → R1201 200 1% 1/20W TK 0201-1 → SOC_GP_PCIE_RCAL_P → R1202 200 1% 1/20W TK 0201-1

PACK_IGNORE=TRUE
PACK_OPTION=GE_PCIE_RCAL

NC_GE_PCIE_RCALN → C1203 10PF 5% 25V C0G 0201 → SOC_ST0_PCIE_RCAL_N → C1200 10PF 5% 25V C0G 0201 → SOC_ST1_PCIE_RCAL_N → C1201 10PF 5% 25V C0G 0201 → SOC_GP_PCIE_RCAL_N → C1202 10PF 5% 25V C0G 0201

PACK_OPTION=SDCARD
PACK_IGNORE=TRUE
PACK_OPTION=ENET
PACK_IGNORE=TRUE
PACK_OPTION=USBHC

PACK_IGNORE=TRUE
PACK_OPTION=GE_PCIE_RCAL

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: PCIE

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ARCH IO V9:

CIO_ATC0_LSTX/RX

CIO_ATC1_LSTX/RX

SOC_ATCPHY0_RCAL_POS/NEG

SOC_ATCPHY1_RCAL_POS/NEG

ARCH IO V9:

CIO_ATC2_LS

CIO_ATC3_LS

SOC_ATCPHY2_RCAL_POS/NEG

SOC_ATCPHY3_RCAL_POS/NEG

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OMIT_TABLE

71 OUT	USBC_ATC0_R2D_C_P<1>	G21	ATCPHY0_TX0_P	USB-C PORT 0	USB-C PORT 2	ATCPHY2_TX0_P	G19	USBC_ATC2_R2D_C_P<1>	OUT 95
71 OUT	USBC_ATC0_R2D_C_N<1>	H21	ATCPHY0_TX0_N			ATCPHY2_TX0_N	H19	USBC_ATC2_R2D_C_N<1>	OUT 95
71 BI	USBC_ATC0_D2R_P<1>	C22	ATCPHY0_RX0_P			ATCPHY2_RX0_P	C20	USBC_ATC2_D2R_P<1>	BI 95
71 BI	USBC_ATC0_D2R_N<1>	D22	ATCPHY0_RX0_N			ATCPHY2_RX0_N	D20	USBC_ATC2_D2R_N<1>	BI 95
71 OUT	USBC_ATC0_R2D_C_P<2>	F20	ATCPHY0_TX1_P			ATCPHY2_TX1_P	F18	USBC_ATC2_R2D_C_P<2>	OUT 95
71 OUT	USBC_ATC0_R2D_C_N<2>	G20	ATCPHY0_TX1_N			ATCPHY2_TX1_N	G18	USBC_ATC2_R2D_C_N<2>	OUT 95
71 BI	USBC_ATC0_D2R_P<2>	B21	ATCPHY0_RX1_P			ATCPHY2_RX1_P	B19	USBC_ATC2_D2R_P<2>	BI 95
71 BI	USBC_ATC0_D2R_N<2>	C21	ATCPHY0_RX1_N			ATCPHY2_RX1_N	C19	USBC_ATC2_D2R_N<2>	BI 95
147 89 BI	EUSB_ATC0_P	B10	USB_C0_EDP			USB_C2_EDP	B9	EUSB_ATC2_P	BI 89 147
147 89 BI	EUSB_ATC0_N	C10	USB_C0_EDM			USB_C2_EDM	C9	EUSB_ATC2_N	BI 89 147
89 OUT	CIO_ATC0_LSTX	M6	USB_C0_LSTX			USB_C2_LSTX	L3	CIO_ATC2_LSTX	OUT 89
89 IN	CIO_ATC0_LSRX	L6	USB_C0_LSRX			USB_C2_LSRX	L2	CIO_ATC2_LSRX	IN 89
73 BI	USBC_ATC0_AUX_P	L22	ATCPHY0_AUX_P			ATCPHY2_AUX_P	L20	USBC_ATC2_AUX_P	BI 82
73 BI	USBC_ATC0_AUX_N	L21	ATCPHY0_AUX_N			ATCPHY2_AUX_N	L19	USBC_ATC2_AUX_N	BI 82
146 NC_USB_C0_HPD		C62	USB_C0_HPD			USB_C2_HPD	R64	NC_USB_C2_HPD	146
72 OUT	USBC_ATC1_R2D_C_P<1>	F22	ATCPHY1_TX0_P	USB-C PORT 1	USB-C PORT 3	ATCPHY3_TX0_P	F24	DP_DP2HDMI_DATA_P<2>	OUT 146
72 OUT	USBC_ATC1_R2D_C_N<1>	G22	ATCPHY1_TX0_N			ATCPHY3_TX0_N	G24	DP_DP2HDMI_DATA_N<2>	OUT 146
72 BI	USBC_ATC1_D2R_P<1>	B23	ATCPHY1_RX0_P			ATCPHY3_RX0_P	B25	DP_DP2HDMI_DATA_P<3>	BI 146
72 BI	USBC_ATC1_D2R_N<1>	C23	ATCPHY1_RX0_N			ATCPHY3_RX0_N	C25	DP_DP2HDMI_DATA_N<3>	BI 146
72 OUT	USBC_ATC1_R2D_C_P<2>	G23	ATCPHY1_TX1_P			ATCPHY3_TX1_P	G25	DP_DP2HDMI_DATA_P<1>	OUT 146
72 OUT	USBC_ATC1_R2D_C_N<2>	H23	ATCPHY1_TX1_N			ATCPHY3_TX1_N	H25	DP_DP2HDMI_DATA_N<1>	OUT 146
72 BI	USBC_ATC1_D2R_P<2>	C24	ATCPHY1_RX1_P			ATCPHY3_RX1_P	C26	DP_DP2HDMI_DATA_P<0>	BI 146
72 BI	USBC_ATC1_D2R_N<2>	D24	ATCPHY1_RX1_N			ATCPHY3_RX1_N	D26	DP_DP2HDMI_DATA_N<0>	BI 146
147 89 BI	EUSB_ATC1_P	B11	USB_C1_EDP			USB_C3_EDP	B12	NC_EUSB_ATC3P	BI 146
147 89 BI	EUSB_ATC1_N	C11	USB_C1_EDM			USB_C3_EDM	C12	NC_EUSB_ATC3N	BI 146
89 OUT	CIO_ATC1_LSTX	N3	USB_C1_LSTX			USB_C3_LSTX	N6	NC_CIO_ATC3_LSTX_1V2	OUT 148
89 IN	CIO_ATC1_LSRX	N2	USB_C1_LSRX			USB_C3_LSRX	N7	NC_CIO_ATC3_LSRX_1V2	IN 148
73 BI	USBC_ATC1_AUX_P	L23	ATCPHY1_AUX_P			ATCPHY3_AUX_P	L25	DP_DP2HDMI_AUX_P	BI 146
73 BI	USBC_ATC1_AUX_N	L24	ATCPHY1_AUX_N			ATCPHY3_AUX_N	L26	DP_DP2HDMI_AUX_N	BI 146
146 NC_USB_C1_HPD		BF40	USB_C1_HPD			USB_C3_HPD (IPD)	BE40	DPRX_INT_HPD	IN 148
9 SOC_ATCPHY0_RCAL_P		B15	ATCPHY0_RCAL_P	RCAL RESREF		ATCPHY2_RCAL_P	B14	SOC_ATCPHY2_RCAL_P	9
9 SOC_ATCPHY0_RCAL_N		C15	ATCPHY0_RCAL_N			ATCPHY2_RCAL_N	C14	SOC_ATCPHY2_RCAL_N	9
9 SOC_ATCPHY1_RCAL_P		B16	ATCPHY1_RCAL_P			ATCPHY3_RCAL_P	B17	SOC_ATCPHY3_RCAL_P	9
9 SOC_ATCPHY1_RCAL_N		C16	ATCPHY1_RCAL_N			ATCPHY3_RCAL_N	C17	SOC_ATCPHY3_RCAL_N	9
9 SOC_USB_C0_RESREF		E15	USB_C0_RESREF			USB_C2_RESREF	F16	SOC_USB_C2_RESREF	9
9 SOC_USB_C1_RESREF		E16	USB_C1_RESREF			USB_C3_RESREF	E17	SOC_USB_C3_RESREF	9
				DBG USB		DBG_USB_EDP	B8	EUSB_DBG_P	OUT 77
						DBG_USB_EDM	C8	EUSB_DBG_N	OUT 77
9 SOC_DBG_USB_RESREF		F15	DBG_USB_RESREF			EUSB_VBUS_DETECT	BD44	EUSB_VBUS_DETECT	9

PP1V2_AWAKE 4 5 8 145

R1412 0 1 2 0% 1/20W TK 0201 EUSB_VBUS_DETECT 9

118S00334

R1400	200	1%	1/20W	TK	0201-1	SOC_DBG_USB_RESREF	9
R1403	200	1%	1/20W	TK	0201-1	SOC_USB_C3_RESREF	9
R1404	200	1%	1/20W	TK	0201-1	SOC_USB_C2_RESREF	9
R1405	200	1%	1/20W	TK	0201-1	SOC_USB_C1_RESREF	9
R1406	200	1%	1/20W	TK	0201-1	SOC_USB_C0_RESREF	9

NO_XNET_CONNECTION=1

9 SOC_ATCPHY0_RCAL_P — R1407 200 1% 1/20W TK 0201-1 — C1407 10PF 5% 25V C0G 0201 — 9 SOC_ATCPHY0_RCAL_N

NO_XNET_CONNECTION=1

9 SOC_ATCPHY1_RCAL_P — R1408 200 1% 1/20W TK 0201-1 — C1408 10PF 5% 25V C0G 0201 — 9 SOC_ATCPHY1_RCAL_N

NO_XNET_CONNECTION=1

9 SOC_ATCPHY2_RCAL_P — R1409 200 1% 1/20W TK 0201-1 — C1409 10PF 5% 25V C0G 0201 — 9 SOC_ATCPHY2_RCAL_N

NO_XNET_CONNECTION=1

9 SOC_ATCPHY3_RCAL_P — R1410 200 1% 1/20W TK 0201-1 — C1410 10PF 5% 25V C0G 0201 — 9 SOC_ATCPHY3_RCAL_N

BOM_COST_GROUP=SOC

PAGE TITLE: SOC: CIO, USB

Apple Inc.

DRAWING NUMBER: 051-08156 | SIZE: D
REVISION: 3.0.0
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DEV-RHO-SGA
BGA
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OMIT_TABLE

136	TP_AOP_FUNC0	BH18	AOP_FUNC[0]	AOP FUNC	NUB_CLK_OUT0	T6	SOC_DOMAIN_NGPIO_AOP1_0
136	TP_AOP_FUNC1	BG16	AOP_FUNC[1]		NUB_DOCK_ATTENTION	T7	TPT_SOC_DOCK_ATTENTION
136 93 IN	HDMI_CEC_AOP_RX	BG17	AOP_FUNC[2]		NUB_DOCK_CONNECT	L4	SOC_DOCK_CONNECT IN 10 135 140
136 93 OUT	HDMI_CEC_AOP_TX	BG25	AOP_FUNC[3]		NUB GPIO NUB_GPIO[0]	N8	NC_NUB_GPIO0 147
93 OUT	SPI_DP2HDMI_HOLD_L	BF17	AOP_FUNC[4]		NUB_GPIO[1]	BF21	CODEC_RESET_L OUT 122 134
136 93 IN	HDMI_HPD_AOP	BE15	AOP_FUNC[5]		NUB_GPIO[2]	U2	SOC_SW_DBG OUT 137
136 66 OUT	SPI_GYRO_CS_L	BH17	AOP_FUNC[6]		NUB_GPIO[3]	T8	TP_AOP_LEAP_MADI_IN 136
66 IN	GYRO_INT	BH16	AOP_FUNC[7]		NUB_GPIO[4]	M8	TP_AOP_LEAP_MADI_OUT 136
66 IN	GYRO_MOTION_INT	BF24	AOP_FUNC[8]		NUB_GPIO[5]	T5	SMC_FIXTURE_MODE_L IN 10 14 134 135
149	NC_AOP_FUNC9	BH10	AOP_FUNC[9]		NUB_GPIO[6]	AN2	NC_NUB_GPIO6 OUT 147
149	SE_NFC_GPIO3	BH15	AOP_FUNC[10]		NUB_GPIO[7]	L8	LOM_PMU_RESET_EN OUT 136
149	NC_AOP_FUNC11	BE16	AOP_FUNC[11]		NUB_GPIO[8]	BD21	TP_NUB_GPIO8 136
149	NC_AOP_FUNC12	BD17	AOP_FUNC[12]		NUB_GPIO[9]	T4	NC_NUB_GPIO9 149
14 OUT	SPI_LAS_CS_L	U8	AOP_FUNC[13]		NUB_GPIO[10]	R5	NC_NUB_GPIO10 149
135 115 OUT	ALS_INT_L	AU2	AOP_FUNC[14]		NUB_GPIO[11]	AN3	IPD_SYS_AWAKE OUT 130
					NUB_GPIO[12]	T3	NC_NUB_GPIO12 149
58 OUT	I2C_AOP_ALS_SCL	BE19	AOP_I2CM0_SCL	AOP I2C			
58 BI	I2C_AOP_ALS_SDA	BE18	AOP_I2CM0_SDA				
149	NC_AOP_I2CM1_SCL	BH26	AOP_I2CM1_SCL		NUB SPMI NUB_SPMI0_SCLK	P8	SPMI_NUB_MPMU_CLK_R OUT 11
149	NC_AOP_I2CM1_SDA	BH25	AOP_I2CM1_SDA		NUB_SPMI0_SDATA	R8	SPMI_NUB_MPMU_DATA_R BI 11
149	NC_AOP_I2CM2_SCL	BD18	AOP_I2CM2_SCL		NUB_SPMI1_SCLK	U3	SPMI_NUB_SPMU_P1V8VDDH_CLK_R OUT 11
149	NC_AOP_I2CM2_SDA	BD19	AOP_I2CM2_SDA		NUB_SPMI1_SDATA	U4	SPMI_NUB_SPMU_P1V8VDDH_DATA_R BI 11
136	TP_AOP_PDM_IN_CLK1	AT4	AOP_PDM_IN_CLK1	AOP PDM	NUB SWD NUB_SWD_TCK_OUT0	P2	SWD_NUB_PMU_SWCLK_R OUT 11
149	NC_AOP_I2S0_MCK	AT5	AOP_PDM_IN_CLK2		NUB_SWD_TMS0	P3	SWD_NUB_PMU_SWDIO_R BI 11
149	NC_AOP_I2S0_LRCK	AV5	AOP_PDM_IN_CLK3		NUB_SWD_TCK_OUT1	BG21	SWD_NUB_CLVR_SWCLK_R OUT 11
149	NC_AOP_I2S0_DOUT	AU5	AOP_PDM_IN_CLK4		NUB_SWD_TMS1	BH21	SWD_NUB_CLVR_SWDIO_R BI 11
149	NC_AOP_I2S0_DIN	AR5	AOP_PDM_IN_CLK5		NUB_SWD_TCK_OUT2	R3	SWD_NUB_IPD_SWCLK OUT 130
149	NC_AOP_I2S0_BCLK	AR4	AOP_PDM_IN_CLK6		NUB_SWD_TMS2	R2	NC_NUB_SWD_TMS2 149
13 OUT	PDM_DMIC_CLK7_R	U6	AOP_PDM_IN_CLK7		NUB_SWD_TCK_OUT7	BH20	SWD_NUB_ATCRTMR0_SWCLK_R BI 11
13 OUT	PDM_DMIC_CLK8_R	BD22	AOP_PDM_IN_CLK8		NUB_SWD_TMS7	BG20	SWD_NUB_ATCRTMR0_SWDIO_R OUT 11
136 134 126 IN	PDM_DMIC_DATA1	U7	AOP_PDM_IN_DATA1 (IPD)		NUB_SWD_TCK_OUT8	BE21	SWD_NUB_ATCRTMR1_SWCLK_R BI 11
136 134 126 IN	PDM_DMIC_DATA4	BD23	AOP_PDM_IN_DATA4 (IPD)		NUB_SWD_TMS8	BE22	SWD_NUB_ATCRTMR1_SWDIO_R OUT 11
14 OUT	SPI_AOP_GYRO_MOSI_R	AU3	AOP_SPI0_MOSI	AOP SPI	NUB_SWD_TMS3	P6	SWD_NUB_IPD_SWDIO BI 130
66 IN	SPI_AOP_GYRO_MISO	AV3	AOP_SPI0_MISO (IPD)				
SPI_AOP_GYRO_CLK_R 14 OUT	SPI_AOP_GYRO_SCLK_R	AT3	AOP_SPI0_SCLK		NUB JTAG JTAG_TCK	AR6	SWD_SOC_SWCLK_R BI 11
13 OUT	SPI_AOP_SENSOR_MOSI_R	AR2	AOP_SPI1_MOSI		JTAG_TMS	AT6	SWD_SOC_SWDIO_R OUT 11
SPI_AOP_SENSORS 13 IN	SPI_AOP_SENSOR_MISO	AP3	AOP_SPI1_MISO (IPD)		JTAG_TDI	AR7	SOC_JTAG_TDI 134 150
13 OUT	SPI_AOP_SENSOR_SCLK_R	AR3	AOP_SPI1_SCLK		JTAG_TDO	AR8	SOC_JTAG_TDO 134 150
147	NC_AOP_SPI1_SSIN	AP2	AOP_SPI1_SSIN		JTAG_TRSTN	AT7	TPT_JTAG_SOC_TRST_L 134
					JTAG_SEL	AT8	SOC_JTAG_SEL IN 10 134
SPMI_AOP_WBLT 148 13 OUT	SPMI_WLBT_CLK_R	AN5	AOP_SPMI0_SCLK	AOP SPMI	JTAG_SLV_TCK	BH22	NC_JTAG_SLV_TCK 149
148 13 BI	SPMI_WLBT_DATA_R	AN4	AOP_SPMI0_SDATA		JTAG_SLV_TMS	AV7	NC_JTAG_SLV_TMS 149
148 13 OUT	SPMI_SE_CLK_R	AP6	AOP_SPMI1_SCLK		JTAG_SLV_TDI	AN8	NC_JTAG_SLV_TDI 149
SPMI_AOP_SE 148 13 BI	SPMI_SE_DATA_R	AP5	AOP_SPMI1_SDATA		JTAG_SLV_TDO	AV8	NC_JTAG_SLV_TDO 149
					JTAG_SLV_TRSTN	AU6	NC_JTAG_SLV_TRSTN 149
147	NC_AOP_UART2_RXD	BD16	AOP_UART2_TXD	AOP UART			
147	NC_AOP_UART2_TXD	BD15	AOP_UART2_RXD				
134 45 IN	PMU_CLK32K_SOC	AW8	RT_CLK32768	AON Clock Resets WDOG	SMC I2C SMC_I2C0_SCL	BH11	I2C_SMC_PWR_SCL OUT 57 135
		AV6	CFSB_AON		SMC_I2C0_SDA	BH12	I2C_SMC_PWR_SDA BI 57 135
137 135 134 73 44 5 IN	PMU_ACTIVE_READY	D2	CFSB_XTAL		SMC_I2C1_SCL	BH14	I2C_SMC_UPC_SCL OUT 32 57 135 136
135 134 44 12 IN	PMU_RESET_L	AW2	COLD_RESETN		SMC_I2C1_SDA	BH13	I2C_SMC_UPC_SDA BI 32 57 135 136
136	TP_AON_SLEEP1_RESET_L	AP8	AON_SLEEP1_RESETN		SMC_I2C2_SCL	BH7	I2C_SMC_NAND_SCL OUT 57 136
44 10 OUT	SOC_WDOG_L	AW3	WDOG_L (IPU)		SMC_I2C2_SDA	BH6	I2C_SMC_NAND_SDA BI 57 136
					SMC_I2C3_SCL	BH24	I2C_SMC_IPD_SCL OUT 130
136 57 IN	UPC_SMC_I2C_INT_L	BH5	SMC_GPIO0	SMC GPIO	SMC_I2C3_SDA	BG24	I2C_SMC_IPD_SDA BI 130
149	SOC_DOMAIN_MGPIO_AOP1	BG4	SMC_GPIO1		SMC_I2C4_SCL	BG10	I2C_SMC_SNS0_SCL OUT 58
149	NC_SMC_GPIO2	AW4	SMC_GPIO2		SMC_I2C4_SDA	BG9	I2C_SMC_SNS0_SDA BI 58
149	NC_SMC_GPIO3	AV2	SMC_GPIO3		SMC_I2C5_SCL	BG6	NC_I2C_SMC_SNS1_SCL OUT 148
149	NC_SMC_GPIO4	BG23	SMC_GPIO4		SMC_I2C5_SDA	BG7	NC_I2C_SMC_SNS1_SDA BI 148
149	NC_SMC_GPIO5	AV4	SMC_GPIO5		SMC_I2C6_SCL	BF23	NC_SMC_I2CM6_SCL 149
147	NC_SMC_GPIO6	AW6	SMC_GPIO6		SMC_I2C6_SDA	BE23	NC_SMC_I2CM6_SDA 149
147 IN	NC_SMC_GPIO7	BH4	SMC_GPIO7				
147	NC_SMC_GPIO8	AW7	SMC_GPIO8				
148 135 29 IN	CHGR_INT_L	BH23	SMC_GPIO9		SMC FPWM SMC_FPWM0	BG13	SMC_FAN_0_PWM OUT 67
					SMC_FPWM1	BG12	SMC_FAN_0_TACH IN 67
135 74 OUT	UART_SMC_DEBUGPRT_R2D	BH8	SMC_UART0_TXD (IPU)	SMC UART	SMC_FPWM2	BE24	SMC_FAN_1_PWM OUT 67
135 74 IN	UART_SMC_DEBUGPRT_D2R	BH9	SMC_UART0_RXD		SMC_FPWM3	BD24	SMC_FAN_1_TACH IN 67
121 IN	DMIC_DISABLE_L	BH19	MIC_DISABLE_L	MIC			
121 IN	DMIC_DISABLE_WARN_L	BD25	MIC_DISABLE_WARN_L				

NEED PULL-UP ON
MIC_DISABLE_*
EITHER SECDIS OR PROJECT SPECIFIC

PP1V2_S2 5 144

R1600	10K	1 2	5%	1/20W	TK	0201	SOC_WDOG_L 10 44
R1601	47K	1 2	5%	1/20W	TK	0201	SOC_DOCK_CONNECT 10 135 140
R1602	10K	1 2	5%	1/20W	TK	0201	SOC_JTAG_SEL 10 134
R1603	47K	1 2	5%	1/20W	TK	0201	SMC_FIXTURE_MODE_L 10 14 134 135

NOSTUFF

ARCH IO V9:

SWD_NUB_IPD_SWCLK_R

SWD_NUB_ATCRTMR01_SWCLK

SWD_NUB_ATCRTMR23_SWCLK

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: AOP, SMC, NUB

Apple Inc.

DRAWING NUMBER 051-08156
SIZE D
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IN PROGRESS

SPMI PMU SERIES RESISTORS

TODO: check resistor values with SI sims

5 IN	SPMI_CLVR0_CLK_R	PLACE_NEAR=U0600.AR61:25MM	R1914	33	5% 1/20W TK 0201	SPMI_CLVR0_CLK	OUT	51
5 BI	SPMI_CLVR0_DATA_R	PLACE_NEAR=U0600.AR62:25MM	R1915	33	5% 1/20W TK 0201	SPMI_CLVR0_DATA	BI	51
5 IN	SPMI_CLVR1_CLK_R	PLACE_NEAR=U0600.BH33:25MM	R1916	33	5% 1/20W TK 0201	SPMI_CLVR1_CLK	OUT	52
5 BI	SPMI_CLVR1_DATA_R	PLACE_NEAR=U0600.BH32:25MM	R1917	33	5% 1/20W TK 0201	SPMI_CLVR1_DATA	BI	52
5 IN	SPMI_CLVR2_CLK_R	PLACE_NEAR=U0600.BG33:25MM	R1950	33	5% 1/20W TK 0201	SPMI_CLVR2_CLK	OUT	53
5 BI	SPMI_CLVR2_DATA_R	PLACE_NEAR=U0600.BG32:25MM	R1951	33	5% 1/20W TK 0201	SPMI_CLVR2_DATA	BI	53
10 IN	SPMI_NUB_MPMU_CLK_R	PLACE_NEAR=U0600.P8:25MM	R1928	33	5% 1/20W TK 0201	SPMI_NUB_MPMU_CLK	OUT	44 136
11 10 BI	SPMI_NUB_MPMU_DATA_R	PLACE_NEAR=U0600.R8:25MM	R1929	33	5% 1/20W TK 0201	SPMI_NUB_MPMU_DATA	BI	44 136
10 IN	SPMI_NUB_SPMU_P1V8VDDH_CLK_R	PLACE_NEAR=U0600.U3:25MM	R1930	20	5% 1/20W TK 0201	SPMI_NUB_SPMU_P1V8VDDH_CLK		
		PLACE_NEAR=U7700.F9:25MM	R1924	49.9	1% 1/20W TK 0201	SPMI_NUB_SPMU_CLK	OUT	40 136
		PLACE_NEAR=U9300.2:25MM	R1925	49.9	1% 1/20W TK 0201	SPMI_NUB_P1V8VDDH_CLK	OUT	48
10 BI	SPMI_NUB_SPMU_P1V8VDDH_DATA_R	PLACE_NEAR=U0600.U4:25MM	R1931	20	5% 1/20W TK 0201	SPMI_NUB_SPMU_P1V8VDDH_DATA		
		PLACE_NEAR=U7700.G10:25MM	R1926	49.9	1% 1/20W TK 0201	SPMI_NUB_SPMU_DATA	BI	40 136
		PLACE_NEAR=U9300.1:25MM	R1927	49.9	1% 1/20W TK 0201	SPMI_NUB_P1V8VDDH_DATA	BI	48

SWD SERIES RESISTORS

10 IN	SWD_NUB_PMU_SWCLK_R	PLACE_NEAR=U0600.P2:25MM	R1942	15 136	5% 1/20W TK 0201	SWD_NUB_PMU_SWCLK					
			R1910	49.9	1% 1/20W TK 0201	PLACE_NEAR=U8100.F11:25MM	SWD_NUB_MPMU_SWCLK	OUT	44
			R1911	49.9	1% 1/20W TK 0201	PLACE_NEAR=U7700.F10:25MM	SWD_NUB_SPMU_SWCLK	OUT	40
10 BI	SWD_NUB_PMU_SWDIO_R	PLACE_NEAR=U0600.P3:25MM	R1943	15 136	5% 1/20W TK 0201	SWD_NUB_PMU_SWDIO					
			R1912	49.9	1% 1/20W TK 0201	PLACE_NEAR=U8100.F11:25MM	SWD_NUB_MPMU_SWDIO	BI	44
			R1913	49.9	1% 1/20W TK 0201	PLACE_NEAR=U7700.F10:25MM	SWD_NUB_SPMU_SWDIO	BI	40
5 IN	SWD_CLVR_SWCLK_R	PLACE_NEAR=U0600.BE36:25MM	R1936	15	5% 1/20W TK 0201	SWD_CLVR_SWCLK					
			R1920	49.9	1% 1/20W TK 0201	PLACE_NEAR=UA100.L1:25MM	SWD_CLVR0_SWCLK	OUT	51
			R1921	49.9	1% 1/20W TK 0201	PLACE_NEAR=UA200.L1:25MM	SWD_CLVR1_SWCLK	OUT	52
6 BI	SWD_CLVR_SWDIO_R	PLACE_NEAR=U0600.BF36:25MM	R1937	15	5% 1/20W TK 0201	SWD_CLVR_SWDIO					
			R1922	49.9	1% 1/20W TK 0201	PLACE_NEAR=UA100.K1:25MM	SWD_CLVR0_SWDIO	BI	51
			R1923	49.9	1% 1/20W TK 0201	PLACE_NEAR=UA200.K1:25MM	SWD_CLVR1_SWDIO	BI	52
10 IN	SWD_NUB_CLVR_SWCLK_R	PLACE_NEAR=U0600.BG21:25MM	R1960	33	5% 1/20W TK 0201	SWD_CLVR2_SWCLK	OUT	53
10 BI	SWD_NUB_CLVR_SWDIO_R	PLACE_NEAR=U0600.BH21:25MM	R1961	33	5% 1/20W TK 0201	SWD_CLVR2_SWDIO	BI	53
5 IN	SWD_NAND0_SWCLK_R	PLACE_NEAR=U0600.N65:25MM	R1932	15 134	5% 1/20W TK 0201	SWD_NAND0_SWCLK					
			R1985	49.9	1% 1/20W TK 0201	SWD_NAND0_S5E0_S5E1_SWCLK	OUT	146
			R1986	49.9	1% 1/20W TK 0201	SWD_NAND0_S5E2_S5E3_SWCLK	OUT	146
5 BI	SWD_NAND0_SWDIO_R	PLACE_NEAR=U0600.N64:25MM	R1933	15 134	5% 1/20W TK 0201	SWD_NAND0_SWDIO					
			R1987	15	5% 1/20W TK 0201	SWD_NAND0_S5E0_S5E1_SWDIO	BI	146
			R1988	15	5% 1/20W TK 0201	SWD_NAND0_S5E2_S5E3_SWDIO	BI	146
5 IN	SWD_NAND1_SWCLK_R	PLACE_NEAR=U0600.AV62:25MM	R1934	15 134	5% 1/20W TK 0201	SWD_NAND1_SWCLK					
			R1989	49.9	1% 1/20W TK 0201	SWD_NAND1_S5E0_S5E1_SWCLK	OUT	146
			R1990	49.9	1% 1/20W TK 0201	SWD_NAND1_S5E2_S5E3_SWCLK	OUT	146
5 BI	SWD_NAND1_SWDIO_R	PLACE_NEAR=U0600.AV63:20MM	R1935	15 134	5% 1/20W TK 0201	SWD_NAND1_SWDIO					
			R1991	15	5% 1/20W TK 0201	SWD_NAND1_S5E0_S5E1_SWDIO	BI	146
			R1992	15	5% 1/20W TK 0201	SWD_NAND1_S5E2_S5E3_SWDIO	BI	146
10	SWD_NUB_ATCRTMR0_SWDIO_R		R1971	49.9	1% 1/20W TK 0201	SWD_NUB_ATCRTMR0_SWDIO		148
10	SWD_NUB_ATCRTMR0_SWCLK_R		R1972	49.9	1% 1/20W TK 0201	SWD_NUB_ATCRTMR0_SWCLK		148
10	SWD_NUB_ATCRTMR1_SWDIO_R		R1973	49.9	1% 1/20W TK 0201	SWD_NUB_ATCRTMR1_SWDIO		148
10	SWD_NUB_ATCRTMR1_SWCLK_R		R1974	49.9	1% 1/20W TK 0201	SWD_NUB_ATCRTMR1_SWCLK		148
10 OUT	SWD_SOC_SWCLK_R	PLACE_NEAR=U0600.AR6:25MM	R1938	0	0% 1/20W TK 0201	SWD_SOC_SWCLK	IN	74 134 135
10 BI	SWD_SOC_SWDIO_R	PLACE_NEAR=U0600.AT6:25MM	R1939	0	0% 1/20W TK 0201	SWD_SOC_SWDIO	BI	74 134 135
8 IN	SWD_UPC_SWCLK_R	PLACE_NEAR=U0600.R66:25MM	R1946	49.9	1% 1/20W TK 0201	SWD_UPC_SWCLK0	OUT	89
			R1993	49.9	1% 1/20W TK 0201	SWD_UPC_SWCLK1	OUT	32 89
9 BI	SWD_UPC_SWDIO0_R	PLACE_NEAR=U0600.V67:25MM	R1947	0	1% 1/20W TK 0201	SWD_UPC_SWDIO0	BI	89
8 BI	SWD_UPC_SWDIO1_R	PLACE_NEAR=U0600.C64:25MM	R1948	0	0% 1/20W TK 0201	SWD_UPC_SWDIO1	BI	89
8 BI	SWD_UPC_SWDIO2_R	PLACE_NEAR=U0600.R67:25MM	R1949	0	0% 1/20W TK 0201	SWD_UPC_SWDIO2	BI	32
146 8 BI	SWD_UPC_SWDIO3_R	PLACE_NEAR=U0600.BH38:25MM	R1956	0	0% 1/20W TK 0201	SWD_UPC_SWDIO3	BI	89

VDD/VSS SENSE BREAKOUT PADS

All SOC/DRAM VSNS traces to be 50ohm SE-impedance

Non-CLVR SENSE points are only for debug/characterization access

Non-CLVR diff SENSE use resistor pads. These will never be STUFF'd:

22 IN	VSNS_PVDD2H0_SENSE0_P	NOSTUFF	R19A0	10K 5% 1/20W TK 0201	VSNS_PVDD2H1_SENSE1_P
25 IN	VSNS_PVDD2H0_SENSE0_N				VSNS_PVDD2H1_SENSE1_N
22 IN	VSNS_PVDD2H0_SENSE2_P	NOSTUFF	R19A1	10K 5% 1/20W TK 0201	VSNS_PVDD2H1_SENSE3_P
25 IN	VSNS_PVDD2H0_SENSE2_N				VSNS_PVDD2H1_SENSE3_N

23 IN	VSNS_PVDD2H1_SENSE1_P	NOSTUFF	R19A2	10K 5% 1/20W TK 0201	
25 IN	VSNS_PVDD2H1_SENSE1_N				
23 IN	VSNS_PVDD2H1_SENSE3_P	NOSTUFF	R19A3	10K 5% 1/20W TK 0201	
25 IN	VSNS_PVDD2H1_SENSE3_N				

CLVR rail SENSE points are used in Factory in place of fixture probe access on PP* net, so they require HWTE TPs:

15 IN	VSNS_PVDDPCPU0_SENSE_P PLACE_NEAR=TP19A1.1:2MM	TP19A0 1 A TP-P4
25 IN	VSNS_PVDDPCPU0_SENSE_N	TP19A1 1 A TP-P4

P/N pairs do not require diff impedance control, But should be routed as a pair for noise immunity

IN	VSNS_PVDDDCS_SENSE PLACE_NEAR=PP19A3.1:5MM	PP19A0 1 PP P3MM SM
18 IN	VSNS_PVDDO0_SENSE PLACE_NEAR=PP19A3.1:5MM	PP19A1 1 PP P3MM SM
IN	VSNS_PVDDAMPH0_SENSE PLACE_NEAR=PP19A3.1:5MM	PP19A2 1 PP P3MM SM
25 IN	VSNS_PVSSDDR_SENSE	PP19A3 1 PP P3MM SM

Place VSSDDR PP near these related PP's
Constrain trace skew <15mm for the group

15 IN	VSNS_PVDDECPU_SENSE	PP19A4 1 PP P3MM SM
16 IN	VSNS_PVDDSOC_SENSE	PP19A5 1 PP P3MM SM
16 IN	VSNS_PVDDDISP_SENSE	PP19A6 1 PP P3MM SM
IN	VSNS_PVDDSRAM_SENSE	PP19A7 1 PP P3MM SM
15 IN	VSNS_PVDDPCPU0_ABSMIN	PP19A8 1 PP P3MM SM
15 IN	VSNS_PVDDPCPU1_ABSMIN	PP19A9 1 PP P3MM SM
25 IN	VSNS_PVSS_SENSE	PP19AA 1 PP P3MM SM

Place VSS PP near these related PP's, if possible

15 IN	VSNS_PVDDGPU0_SENSE	TP19A2 1 A TP-P4
19 IN	VSNS_PVDDAFRCS_SENSE	TP19A3 1 A TP-P4
19 IN	VSNS_PVDDANE_SENSE	TP19A4 1 A TP-P4
20 IN	VSNS_PVDDFABRIC_SENSE	TP19A5 1 A TP-P4

HWTE access to CLVR outputs

TP19A* SENSE TPs can be used in place out output nets. Below are the CLVR outputs that don't have a SENSE TP
Place XWs under CLVRs, to breakout to HWTE-accessible test vias
TP_PPVDD nets require special spacing constraints to all nets except GND

143 IN	PPVDD_PCPU1_AWAKESW	XW19B0
	TP_PPVDD_PCPU1_AWAKESW	SHORT-20L-0.1MM-SM NO_XNET_CONNECTION=1
143 IN	PPVDD_GPU_SRAM0_AWAKESW	XW19C1
	TP_PPVDD_GPU_SRAM0_AWAKESW	SHORT-20L-0.1MM-SM NO_XNET_CONNECTION=1
143 IN	PPVDD_ANE_SRAM_AWAKESW	XW19D1
	TP_PPVDD_ANE_SRAM_AWAKESW	SHORT-20L-0.1MM-SM NO_XNET_CONNECTION=1
143 IN	PPVDD_PCPU_SRAM1_AWAKESW	XW19B1
	TP_PPVDD_PCPU_SRAM1_AWAKESW	SHORT-20L-0.1MM-SM NO_XNET_CONNECTION=1
143 IN	PPVDD_GPU1_AWAKESW	XW19C2
	TP_PPVDD_GPU1_AWAKESW	SHORT-20L-0.1MM-SM NO_XNET_CONNECTION=1
143 IN	PPVDD_PCPU_SRAM0_AWAKESW	XW19B3
	TP_PPVDD_PCPU_SRAM0_AWAKESW	SHORT-20L-0.1MM-SM NO_XNET_CONNECTION=1
143 IN	PPVDD_GPU_SRAM1_AWAKESW	XW19C3
	TP_PPVDD_GPU_SRAM1_AWAKESW	SHORT-20L-0.1MM-SM NO_XNET_CONNECTION=1

NAND PCIE CLK BRANCH RESISTORS

8 IN	PCIE_CLK100M_NAND0_0_1_P	MAKE_BASE=TRUE	PCIE_CLK100M_NAND0_0_1_P OUT 103 113
			PCIE_CLK100M_NAND0_0_1_P OUT 104
8 IN	PCIE_CLK100M_NAND0_0_1_N	MAKE_BASE=TRUE	PCIE_CLK100M_NAND0_0_1_N OUT 103 113
			PCIE_CLK100M_NAND0_0_1_N OUT 104
8 IN	PCIE_CLK100M_NAND0_2_3_P	MAKE_BASE=TRUE	PCIE_CLK100M_NAND0_2_3_P OUT 105 113
			PCIE_CLK100M_NAND0_2_3_P OUT 106
8 IN	PCIE_CLK100M_NAND0_2_3_N	MAKE_BASE=TRUE	PCIE_CLK100M_NAND0_2_3_N OUT 105 113
			PCIE_CLK100M_NAND0_2_3_N OUT 106
8 IN	PCIE_CLK100M_NAND1_0_1_P	MAKE_BASE=TRUE	PCIE_CLK100M_NAND1_0_1_P OUT 108 113
			PCIE_CLK100M_NAND1_0_1_P OUT 109
8 IN	PCIE_CLK100M_NAND1_0_1_N	MAKE_BASE=TRUE	PCIE_CLK100M_NAND1_0_1_N OUT 108 113
			PCIE_CLK100M_NAND1_0_1_N OUT 109
8 IN	PCIE_CLK100M_NAND1_2_3_P	MAKE_BASE=TRUE	PCIE_CLK100M_NAND1_2_3_P OUT 110 113
			PCIE_CLK100M_NAND1_2_3_P OUT 111
8 IN	PCIE_CLK100M_NAND1_2_3_N	MAKE_BASE=TRUE	PCIE_CLK100M_NAND1_2_3_N OUT 110 113
			PCIE_CLK100M_NAND1_2_3_N OUT 111

136 5 OUT	PMU_UVWARN_ILIMIT_L	R198B	909	1% 1/20W TK 0201	P3V8AON_ILIMIT_L IN 36
		R1980	430	1% 1/20W TK 0201	PMU_VDDMAIN_UVWARN_L IN 44 136
		R1981	0	0% 1/20W TK 0201	PMU_VDDHI_UVWARN_L IN 44 136

SPMI_NUB DAMPING FILTERS

11 10 SPMI_NUB_MPMU_DATA_R

C1902 1 10PF 5% 25V C0G 0201 2

BOM_COST_GROUP=SOC

PAGE TITLE

SOC: SHARED SUPPORT

Apple Inc.

DRAWING NUMBER 051-08156 | SIZE D

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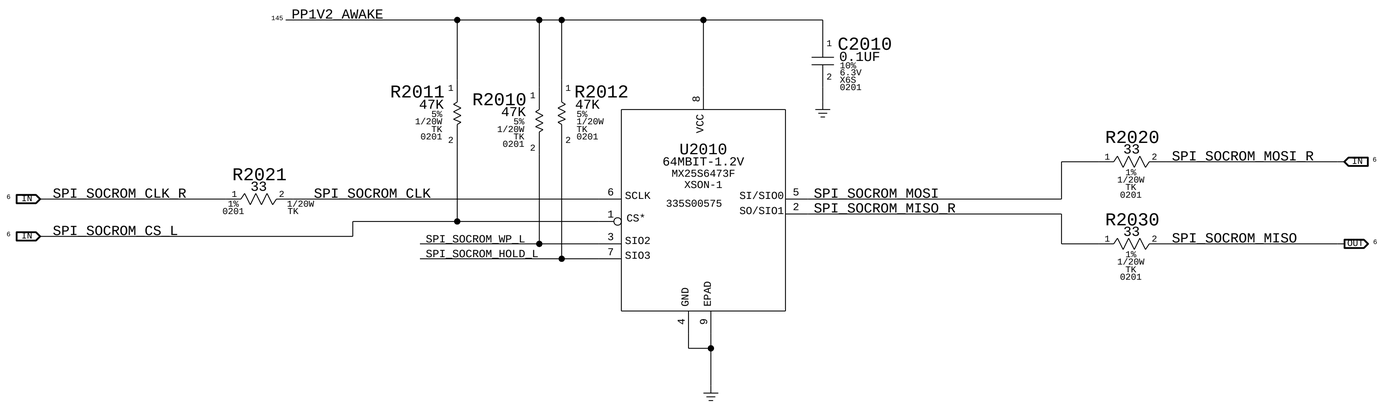
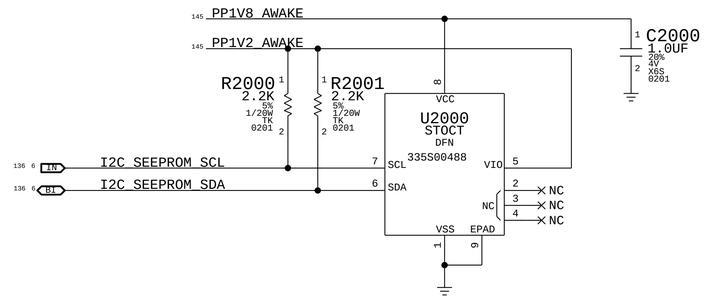
SPI NOR (1.2V 64MBIT)



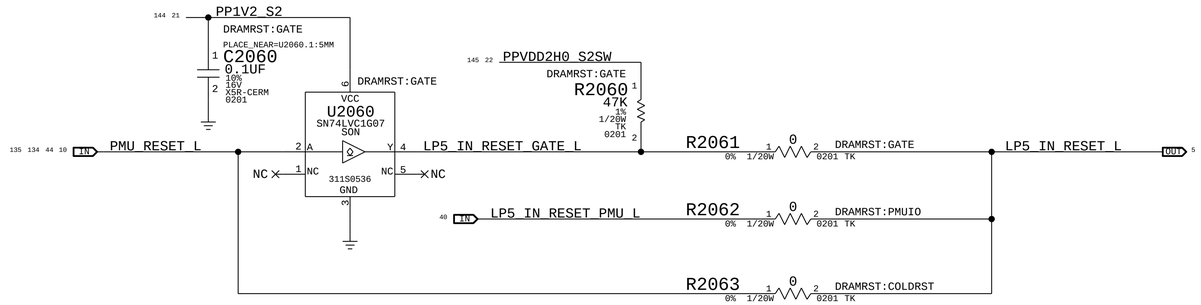
SEP EEPROM (16KBIT)

(Write: 0xA2, Read 0xA3)

APN:335S00488



rdar://83318583 (Add new LP5_IN_RESET_L signal options (discrete gate and SPMU GPIO))



BOM_COST_GROUP=SOC

PAGE TITLE
SOC: SPI NOR, SEP ROM, LP5 RESET

Apple Inc.

DRAWING NUMBER 051-08156 SIZE D
REVISION 3.0.0
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SGA SPMI SE SOURCE TERMINATIONS

R2100 33 5% 1/20W TK 0201
148 10 IN SPMI_SE_CLK_R 1 2 SPMI_SE_CLK OUT 26

R2101 33 5% 1/20W TK 0201
148 10 BI SPMI_SE_DATA_R 1 2 SPMI_SE_DATA BI 26

SGA SPI BKLT SOURCE TERMINATIONS

117S00113
R2172 20 5% 1/20W TK 0201
7 IN SPI_DISP_BKLT_MOSI_R 1 2 SPI_DISP_BKLT_MOSI OUT 119 135
PLACE_NEAR=U0600.BH34:15MM

117S00113
R2173 20 5% 1/20W TK 0201
7 IN SPI_DISP_BKLT_CLK_R 1 2 SPI_DISP_BKLT_CLK OUT 119 135
PLACE_NEAR=U0600.BH34:15MM

LUXE SPMI SOURCE TERMINATIONS

117S00113
R2174 20 5% 1/20W TK 0201
135 7 IN SPMI_DISP_BKLT_CLK_R 1 2 SPMI_DISP_BKLT_CLK OUT 118
PLACE_NEAR=U0600.AU61:15MM

117S00113
R2175 20 5% 1/20W TK 0201
135 7 BI SPMI_DISP_BKLT_DATA_R 1 2 SPMI_DISP_BKLT_DATA BI 118
PLACE_NEAR=U0600.AT61:15MM

NAND CLKREQ SERIES RESISTORS

R2176 0 0% 1/20W TK 0201
134 8 IN NAND0_CLKREQ0_L 1 2 NAND0_CLKREQ0_R_L OUT 103

R2177 0 0% 1/20W TK 0201
134 8 IN NAND0_CLKREQ1_L 1 2 NAND0_CLKREQ1_R_L OUT 104

R2178 0 0% 1/20W TK 0201
134 8 IN NAND0_CLKREQ2_L 1 2 NAND0_CLKREQ2_R_L OUT 105

R2179 0 0% 1/20W TK 0201
134 8 IN NAND0_CLKREQ3_L 1 2 NAND0_CLKREQ3_R_L OUT 106

R2180 0 0% 1/20W TK 0201
134 8 IN NAND1_CLKREQ0_L 1 2 NAND1_CLKREQ0_R_L OUT 108

R2181 0 0% 1/20W TK 0201
134 8 IN NAND1_CLKREQ1_L 1 2 NAND1_CLKREQ1_R_L OUT 109

R2182 0 0% 1/20W TK 0201
134 8 IN NAND1_CLKREQ2_L 1 2 NAND1_CLKREQ2_R_L OUT 110

R2183 0 0% 1/20W TK 0201
134 8 IN NAND1_CLKREQ3_L 1 2 NAND1_CLKREQ3_R_L OUT 111

SSD 24M CLOCK TERMINATIONS

R2184 15 5% 1/20W TK 0201
8 IN NAND0_CLK24M_R 1 2 NAND0_CLK24M_0123_R

R2185 49.9 1% 1/20W TK 0201
NAND0_CLK24M_0123_R 1 2 NAND0_CLK24M_01 MAKE_BASE=TRUE
NAND0_CLK24M_01 OUT 103
NAND0_CLK24M_01 OUT 104

R2186 49.9 1% 1/20W TK 0201
NAND0_CLK24M_0123_R 1 2 NAND0_CLK24M_23 MAKE_BASE=TRUE
NAND0_CLK24M_23 OUT 105
NAND0_CLK24M_23 OUT 106

R2187 15 5% 1/20W TK 0201
8 IN NAND1_CLK24M_R 1 2 NAND1_CLK24M_0123_R

R2188 49.9 1% 1/20W TK 0201
NAND1_CLK24M_0123_R 1 2 NAND1_CLK24M_01 MAKE_BASE=TRUE
NAND1_CLK24M_01 OUT 108
NAND1_CLK24M_01 OUT 109

R2189 49.9 1% 1/20W TK 0201
NAND1_CLK24M_0123_R 1 2 NAND1_CLK24M_23 MAKE_BASE=TRUE
NAND1_CLK24M_23 OUT 110
NAND1_CLK24M_23 OUT 111

SGA SPI SENSOR SOURCE TERMINATIONS

117S00113
R2120 20 5% 1/20W TK 0201
10 IN SPI_AOP_SENSOR_MOSI_R 1 2 SPI_AOP_SENSOR_MOSI OUT 14
PLACE_NEAR=U0600.AR2:18MM

117S00113
R2121 20 5% 1/20W TK 0201
10 IN SPI_AOP_SENSOR_SCLK_R 1 2 SPI_AOP_SENSOR_SCLK OUT 14
PLACE_NEAR=U0600.AR3:18MM

117S00113
R2122 20 5% 1/20W TK 0201
10 OUT SPI_AOP_SENSOR_MISO 1 2 SPI_AOP_SENSOR_MISO_R IN 14
PLACE_NEAR=U2240.4:15MM

SGA SPI IPD SOURCE TERMINATIONS

117S00113
R2123 20 5% 1/20W TK 0201
6 IN SPI_IPD_MOSI_R 1 2 SPI_IPD_MOSI OUT 130 139
PLACE_NEAR=U0600.N5:15MM

117S00113
R2124 20 5% 1/20W TK 0201
6 IN SPI_IPD_CLK_R 1 2 SPI_IPD_CLK OUT 130 139
PLACE_NEAR=U0600.N4:15MM

SGA SPI TOUCHID SOURCE TERMINATIONS

117S00113
R2125 20 5% 1/20W TK 0201
6 IN SPI_TOUCHID_MOSI_R 1 2 SPI_TOUCHID_MOSI OUT 132
PLACE_NEAR=U0600.BG60:16MM

117S00113
R2126 20 5% 1/20W TK 0201
6 IN SPI_TOUCHID_CLK_R 1 2 SPI_TOUCHID_CLK OUT 132
PLACE_NEAR=U0600.BG58:16MM

SGA SPI TCON SOURCE TERMINATIONS

R2127 33 5% 1/20W TK 0201
6 IN SPI_TCON_MOSI_R 1 2 SPI_TCON_MOSI OUT 116 135
PLACE_NEAR=U0600.BE53:15MM

R2128 33 5% 1/20W TK 0201
6 IN SPI_TCON_CLK_R 1 2 SPI_TCON_CLK OUT 116 135
PLACE_NEAR=U0600.BE52:15MM

DMIC CLK SOURCE TERMINATIONS

R2158 33 5% 1/20W TK 0201
10 IN PDM_DMIC_CLK7_R 1 2 PDM_DMIC_CLK7 OUT 126 134 136
PLACE_NEAR=U0600.U6:25MM

R2159 33 5% 1/20W TK 0201
10 IN PDM_DMIC_CLK8_R 1 2 PDM_DMIC_CLK8 OUT 126 134 136
PLACE_NEAR=U0600.BD22:25MM

R2102 0 0% 1/20W TK 0201
148 IN SPI_TCON_CS_R_L 1 2 SPI_TCON_CS_L OUT 116 135
PLACE_NEAR=U0600.BE54:25MM

SGA TDM SOURCE TERMINATIONS

117S00113
R2160 20 5% 1/20W TK 0201
6 IN TDM_SPKRAMP_L_BCLK_R 1 2 TDM_SPKRAMP_L_BCLK MAKE_BASE=TRUE
PLACE_NEAR=U0600.BH54:18MM
TDM_SPKRAMP_L_BCLK 123 134
TDM_SPKRAMP_L_BCLK 123
TDM_SPKRAMP_L_BCLK 123

117S00113
R2161 20 5% 1/20W TK 0201
6 IN TDM_SPKRAMP_L_R2D_R 1 2 TDM_SPKRAMP_L_R2D MAKE_BASE=TRUE
PLACE_NEAR=U0600.BG53:17MM
TDM_SPKRAMP_L_R2D 123 134
TDM_SPKRAMP_L_R2D 123
TDM_SPKRAMP_L_R2D 123

117S00113
R2162 20 5% 1/20W TK 0201
6 IN TDM_SPKRAMP_L_FSYNC_R 1 2 TDM_SPKRAMP_L_FSYNC MAKE_BASE=TRUE
PLACE_NEAR=U0600.BG54:17MM
TDM_SPKRAMP_L_FSYNC 123 134
TDM_SPKRAMP_L_FSYNC 123
TDM_SPKRAMP_L_FSYNC 123

6 OUT TDM_SPKRAMP_L_D2R MAKE_BASE=TRUE
TDM_SPKRAMP_L_D2R 123 134
TDM_SPKRAMP_L_D2R 123
TDM_SPKRAMP_L_D2R 123

117S00113
R2163 20 5% 1/20W TK 0201
6 IN TDM_SPKRAMP_R_BCLK_R 1 2 TDM_SPKRAMP_R_BCLK MAKE_BASE=TRUE
PLACE_NEAR=U0600.BE51:18MM
TDM_SPKRAMP_R_BCLK 124 134
TDM_SPKRAMP_R_BCLK 124
TDM_SPKRAMP_R_BCLK 124

117S00113
R2164 20 5% 1/20W TK 0201
6 IN TDM_SPKRAMP_R_R2D_R 1 2 TDM_SPKRAMP_R_R2D MAKE_BASE=TRUE
PLACE_NEAR=U0600.BD49:17MM
TDM_SPKRAMP_R_R2D 124 134
TDM_SPKRAMP_R_R2D 124
TDM_SPKRAMP_R_R2D 124

117S00113
R2165 20 5% 1/20W TK 0201
6 IN TDM_SPKRAMP_R_FSYNC_R 1 2 TDM_SPKRAMP_R_FSYNC MAKE_BASE=TRUE
PLACE_NEAR=U0600.BF51:18MM
TDM_SPKRAMP_R_FSYNC 124 134
TDM_SPKRAMP_R_FSYNC 124
TDM_SPKRAMP_R_FSYNC 124

6 OUT TDM_SPKRAMP_R_D2R MAKE_BASE=TRUE
TDM_SPKRAMP_R_D2R 124 134
TDM_SPKRAMP_R_D2R 124
TDM_SPKRAMP_R_D2R 124

117S00113
R2166 20 5% 1/20W TK 0201
6 IN TDM_CODEC_BCLK_R 1 2 TDM_CODEC_BCLK OUT 122 134
PLACE_NEAR=U0600.BH51:17MM

117S00113
R2167 20 5% 1/20W TK 0201
6 IN TDM_CODEC_R2D_R 1 2 TDM_CODEC_R2D OUT 122 134
PLACE_NEAR=U0600.BH52:15MM

117S00113
R2168 20 5% 1/20W TK 0201
6 IN TDM_CODEC_FSYNC_R 1 2 TDM_CODEC_FSYNC OUT 122 134
PLACE_NEAR=U0600.BG51:18MM

R2169 33 5% 1/20W TK 0201
148 10 IN SPMI_WLBT_CLK_R 1 2 SPMI_WLBT_CLK OUT 101

R2170 33 5% 1/20W TK 0201
148 10 IN SPMI_WLBT_DATA_R 1 2 SPMI_WLBT_DATA OUT 101

BOM_COST_GROUP=SOC

PAGE TITLE
PROJECT SUPPORT (1/2)

Apple Inc.

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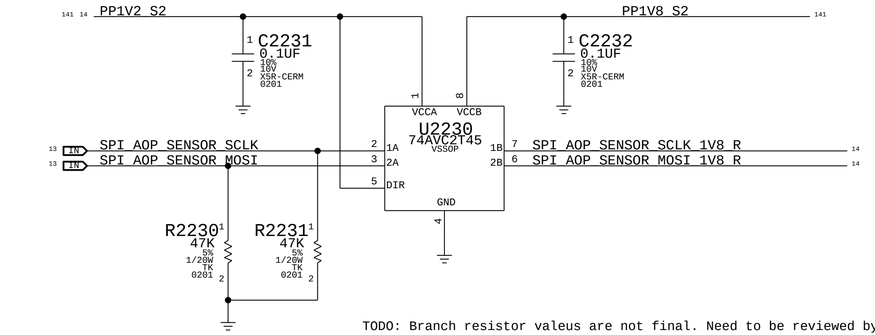
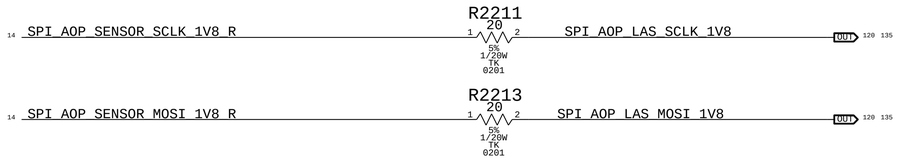
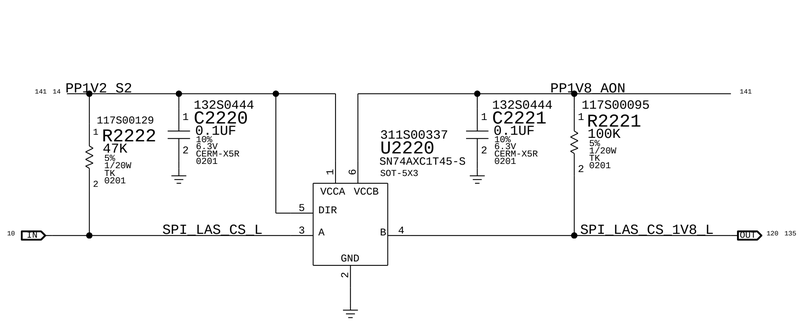
SPI AOP Sensor LS and Branch Resistors

TODO: Reference designators need to be updated once layout has imported latest netlist

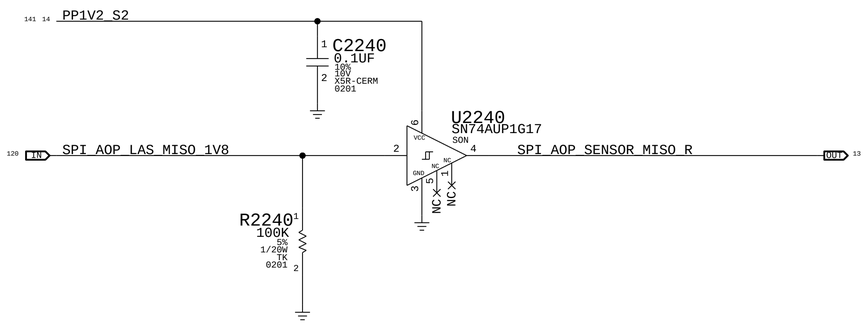


TODO: Branch resistor valeus are not final. Need to be reviewed by SI once routed

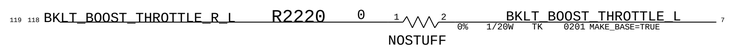




SPI LEVEL TRANSLATION

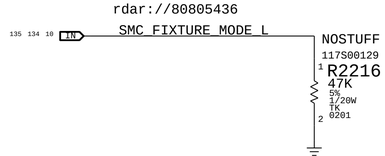


DISPLAY BACKLIGHT



rdar://86287477
(J414x P1x missing PD for AOP_SPI0_MOSI and AOP_SPI0_SCLK)

rdar://80805436



BOM_COST_GROUP=SOC

PAGE TITLE: PROJECT SUPPORT (2/2)

Apple Inc.

DRAWING NUMBER: 051-08156
SIZE: D
REVISION: 3.0.0
BRANCH: evt-1
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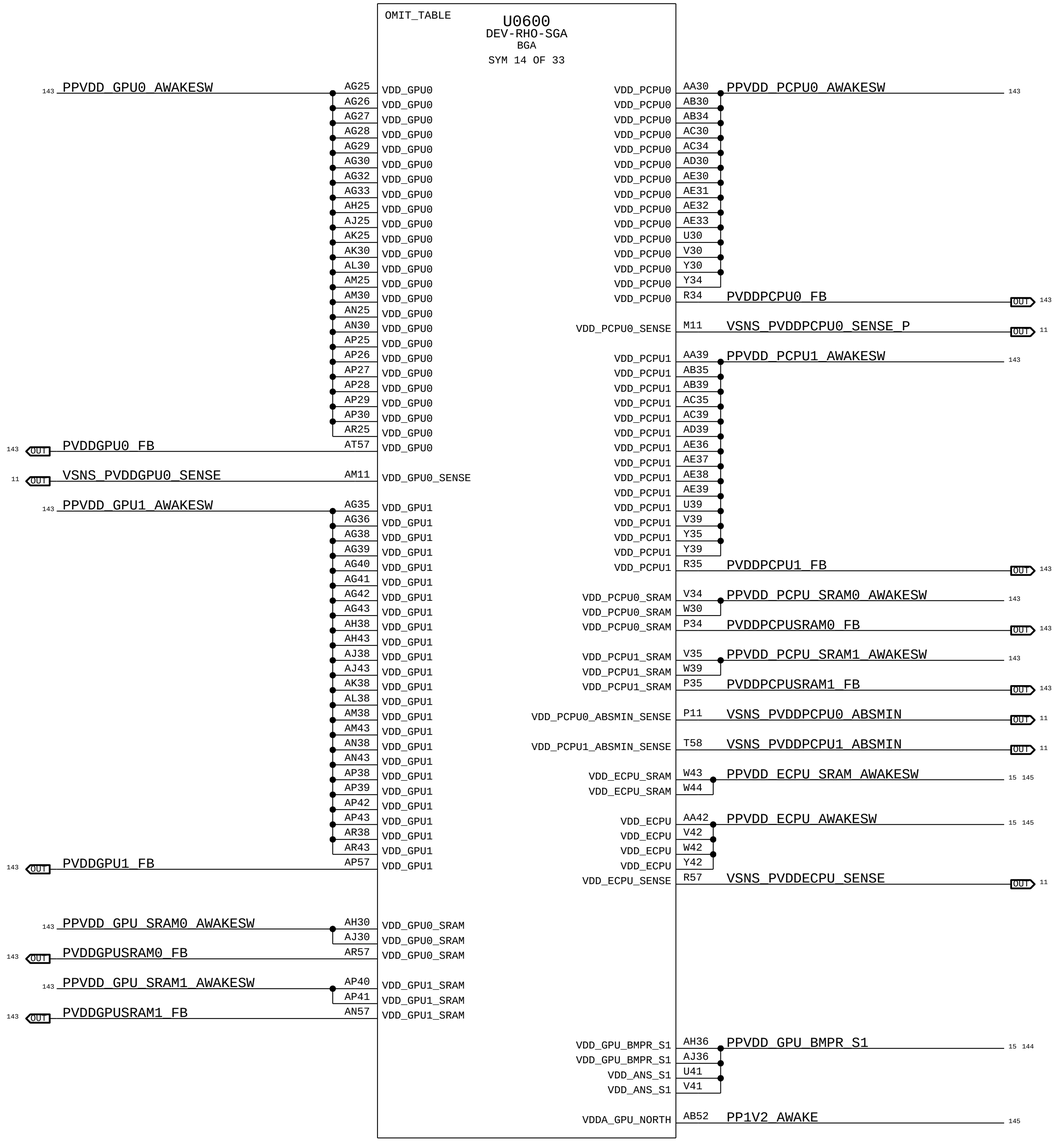

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (CPU, GPU)

Apple Inc.

DRAWING NUMBER 051-08156
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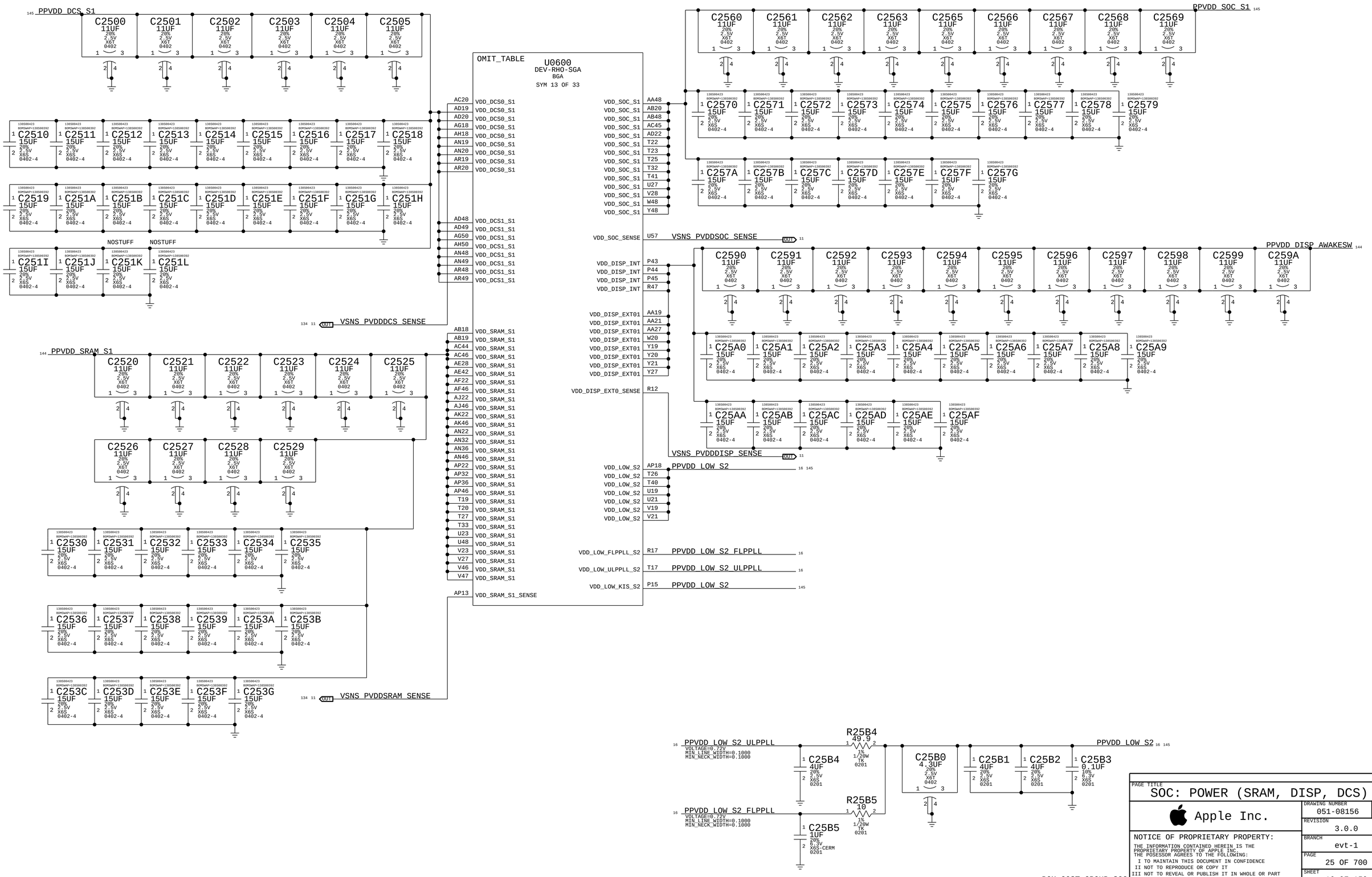
PPVDD_DCS_S1
C2500 11UF 20% 2.5V X6T 0402
C2501 11UF 20% 2.5V X6T 0402
C2502 11UF 20% 2.5V X6T 0402
C2503 11UF 20% 2.5V X6T 0402
C2504 11UF 20% 2.5V X6T 0402
C2505 11UF 20% 2.5V X6T 0402
C2510 15UF 20% 2.5V X6S 0402-4
C2511 15UF 20% 2.5V X6S 0402-4
C2512 15UF 20% 2.5V X6S 0402-4
C2513 15UF 20% 2.5V X6S 0402-4
C2514 15UF 20% 2.5V X6S 0402-4
C2515 15UF 20% 2.5V X6S 0402-4
C2516 15UF 20% 2.5V X6S 0402-4
C2517 15UF 20% 2.5V X6S 0402-4
C2518 15UF 20% 2.5V X6S 0402-4
C2519 15UF 20% 2.5V X6S 0402-4
C251A 15UF 20% 2.5V X6S 0402-4
C251B 15UF 20% 2.5V X6S 0402-4
C251C 15UF 20% 2.5V X6S 0402-4
C251D 15UF 20% 2.5V X6S 0402-4
C251E 15UF 20% 2.5V X6S 0402-4
C251F 15UF 20% 2.5V X6S 0402-4
C251G 15UF 20% 2.5V X6S 0402-4
C251H 15UF 20% 2.5V X6S 0402-4
NOSTUFF
NOSTUFF
C251I 15UF 20% 2.5V X6S 0402-4
C251J 15UF 20% 2.5V X6S 0402-4
C251K 15UF 20% 2.5V X6S 0402-4
C251L 15UF 20% 2.5V X6S 0402-4
OMIT_TABLE
U0600
DEV-RHO-SGA
BGA
SYM 13 OF 33
AC20 VDD_DCS0_S1
AD19 VDD_DCS0_S1
AD20 VDD_DCS0_S1
AG18 VDD_DCS0_S1
AH18 VDD_DCS0_S1
AN19 VDD_DCS0_S1
AN20 VDD_DCS0_S1
AR19 VDD_DCS0_S1
AR20 VDD_DCS0_S1
AD48 VDD_DCS1_S1
AD49 VDD_DCS1_S1
AG50 VDD_DCS1_S1
AH50 VDD_DCS1_S1
AN48 VDD_DCS1_S1
AN49 VDD_DCS1_S1
AR48 VDD_DCS1_S1
AR49 VDD_DCS1_S1
VSNS_PVDDDCS_SENSE
PPVDD_SRAM_S1
C2520 11UF 20% 2.5V X6T 0402
C2521 11UF 20% 2.5V X6T 0402
C2522 11UF 20% 2.5V X6T 0402
C2523 11UF 20% 2.5V X6T 0402
C2524 11UF 20% 2.5V X6T 0402
C2525 11UF 20% 2.5V X6T 0402
C2526 11UF 20% 2.5V X6T 0402
C2527 11UF 20% 2.5V X6T 0402
C2528 11UF 20% 2.5V X6T 0402
C2529 11UF 20% 2.5V X6T 0402
AB18 VDD_SRAM_S1
AB19 VDD_SRAM_S1
AC44 VDD_SRAM_S1
AC46 VDD_SRAM_S1
AE28 VDD_SRAM_S1
AE42 VDD_SRAM_S1
AF22 VDD_SRAM_S1
AF46 VDD_SRAM_S1
AJ22 VDD_SRAM_S1
AJ46 VDD_SRAM_S1
AK22 VDD_SRAM_S1
AK46 VDD_SRAM_S1
AN22 VDD_SRAM_S1
AN32 VDD_SRAM_S1
AN36 VDD_SRAM_S1
AN46 VDD_SRAM_S1
AP22 VDD_SRAM_S1
AP32 VDD_SRAM_S1
AP36 VDD_SRAM_S1
AP46 VDD_SRAM_S1
T19 VDD_SRAM_S1
T20 VDD_SRAM_S1
T27 VDD_SRAM_S1
T33 VDD_SRAM_S1
U23 VDD_SRAM_S1
U48 VDD_SRAM_S1
V23 VDD_SRAM_S1
V27 VDD_SRAM_S1
V46 VDD_SRAM_S1
V47 VDD_SRAM_S1
AP13 VDD_SRAM_S1_SENSE
VSNS_PVDDSRAM_SENSE
C2530 15UF 20% 2.5V X6S 0402-4
C2531 15UF 20% 2.5V X6S 0402-4
C2532 15UF 20% 2.5V X6S 0402-4
C2533 15UF 20% 2.5V X6S 0402-4
C2534 15UF 20% 2.5V X6S 0402-4
C2535 15UF 20% 2.5V X6S 0402-4
C2536 15UF 20% 2.5V X6S 0402-4
C2537 15UF 20% 2.5V X6S 0402-4
C2538 15UF 20% 2.5V X6S 0402-4
C2539 15UF 20% 2.5V X6S 0402-4
C253A 15UF 20% 2.5V X6S 0402-4
C253B 15UF 20% 2.5V X6S 0402-4
C253C 15UF 20% 2.5V X6S 0402-4
C253D 15UF 20% 2.5V X6S 0402-4
C253E 15UF 20% 2.5V X6S 0402-4
C253F 15UF 20% 2.5V X6S 0402-4
C253G 15UF 20% 2.5V X6S 0402-4
VDD_SOC_S1 AA48
VDD_SOC_S1 AB20
VDD_SOC_S1 AB48
VDD_SOC_S1 AC45
VDD_SOC_S1 AD22
VDD_SOC_S1 T22
VDD_SOC_S1 T23
VDD_SOC_S1 T25
VDD_SOC_S1 T32
VDD_SOC_S1 T41
VDD_SOC_S1 U27
VDD_SOC_S1 V28
VDD_SOC_S1 W48
VDD_SOC_S1 Y48
VDD_SOC_SENSE U57 VSNS_PVDDSOC_SENSE
VDD_DISP_INT P43
VDD_DISP_INT P44
VDD_DISP_INT P45
VDD_DISP_INT R47
VDD_DISP_EXT01 AA19
VDD_DISP_EXT01 AA21
VDD_DISP_EXT01 AA27
VDD_DISP_EXT01 W20
VDD_DISP_EXT01 Y19
VDD_DISP_EXT01 Y20
VDD_DISP_EXT01 Y21
VDD_DISP_EXT01 Y27
VDD_DISP_EXT0_SENSE R12
VSNS_PVDDDISP_SENSE
VDD_LOW_S2 AP18 PPVDD_LOW_S2
VDD_LOW_S2 T26
VDD_LOW_S2 T40
VDD_LOW_S2 U19
VDD_LOW_S2 U21
VDD_LOW_S2 V19
VDD_LOW_S2 V21
VDD_LOW_FLPPLL_S2 R17 PPVDD_LOW_S2_FLPPLL
VDD_LOW_ULPPLL_S2 T17 PPVDD_LOW_S2_ULPPLL
VDD_LOW_KIS_S2 P15 PPVDD_LOW_S2
PPVDD_SOC_S1
C2560 11UF 20% 2.5V X6T 0402
C2561 11UF 20% 2.5V X6T 0402
C2562 11UF 20% 2.5V X6T 0402
C2563 11UF 20% 2.5V X6T 0402
C2565 11UF 20% 2.5V X6T 0402
C2566 11UF 20% 2.5V X6T 0402
C2567 11UF 20% 2.5V X6T 0402
C2568 11UF 20% 2.5V X6T 0402
C2569 11UF 20% 2.5V X6T 0402
C2570 15UF 20% 2.5V X6S 0402-4
C2571 15UF 20% 2.5V X6S 0402-4
C2572 15UF 20% 2.5V X6S 0402-4
C2573 15UF 20% 2.5V X6S 0402-4
C2574 15UF 20% 2.5V X6S 0402-4
C2575 15UF 20% 2.5V X6S 0402-4
C2576 15UF 20% 2.5V X6S 0402-4
C2577 15UF 20% 2.5V X6S 0402-4
C2578 15UF 20% 2.5V X6S 0402-4
C2579 15UF 20% 2.5V X6S 0402-4
C257A 15UF 20% 2.5V X6S 0402-4
C257B 15UF 20% 2.5V X6S 0402-4
C257C 15UF 20% 2.5V X6S 0402-4
C257D 15UF 20% 2.5V X6S 0402-4
C257E 15UF 20% 2.5V X6S 0402-4
C257F 15UF 20% 2.5V X6S 0402-4
C257G 15UF 20% 2.5V X6S 0402-4
PPVDD_DISP_AWAKESW
C2590 11UF 20% 2.5V X6T 0402
C2591 11UF 20% 2.5V X6T 0402
C2592 11UF 20% 2.5V X6T 0402
C2593 11UF 20% 2.5V X6T 0402
C2594 11UF 20% 2.5V X6T 0402
C2595 11UF 20% 2.5V X6T 0402
C2596 11UF 20% 2.5V X6T 0402
C2597 11UF 20% 2.5V X6T 0402
C2598 11UF 20% 2.5V X6T 0402
C2599 11UF 20% 2.5V X6T 0402
C259A 11UF 20% 2.5V X6T 0402
C25A0 15UF 20% 2.5V X6S 0402-4
C25A1 15UF 20% 2.5V X6S 0402-4
C25A2 15UF 20% 2.5V X6S 0402-4
C25A3 15UF 20% 2.5V X6S 0402-4
C25A4 15UF 20% 2.5V X6S 0402-4
C25A5 15UF 20% 2.5V X6S 0402-4
C25A6 15UF 20% 2.5V X6S 0402-4
C25A7 15UF 20% 2.5V X6S 0402-4
C25A8 15UF 20% 2.5V X6S 0402-4
C25A9 15UF 20% 2.5V X6S 0402-4
C25AA 15UF 20% 2.5V X6S 0402-4
C25AB 15UF 20% 2.5V X6S 0402-4
C25AC 15UF 20% 2.5V X6S 0402-4
C25AD 15UF 20% 2.5V X6S 0402-4
C25AE 15UF 20% 2.5V X6S 0402-4
C25AF 15UF 20% 2.5V X6S 0402-4
PPVDD_LOW_S2_ULPPLL
VOLTAGE=0.72V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
R25B4 49.9 1% 1/20W TK 0201
C25B4 4UF 20% 2.5V X6S 0201
C25B0 4.3UF 20% 2.5V X6T 0402
C25B1 4UF 20% 2.5V X6S 0201
C25B2 4UF 20% 2.5V X6S 0201
C25B3 0.1UF 10% 6.3V X6S 0201
PPVDD_LOW_S2
PPVDD_LOW_S2_FLPPLL
VOLTAGE=0.72V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
R25B5 10 1% 1/20W TK 0201
C25B5 1UF 20% 6.3V X6S-CERM 0201
BOM_COST_GROUP=SOC
PAGE TITLE
SOC: POWER (SRAM, DISP, DCS)
Apple Inc.
DRAWING NUMBER 051-08156
SIZE D
REVISION 3.0.0
BRANCH evt-1
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SHEET 16 OF 159
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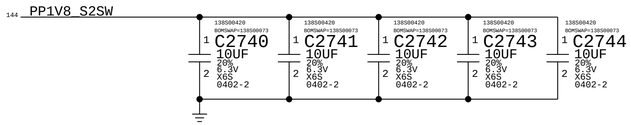

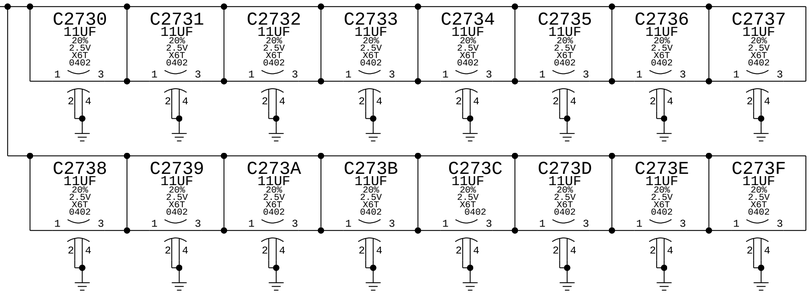

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (VDD1)

Apple Inc.

DRAWING NUMBER 051-08156
SIZE D
REVISION 3.0.0
BRANCH evt-1
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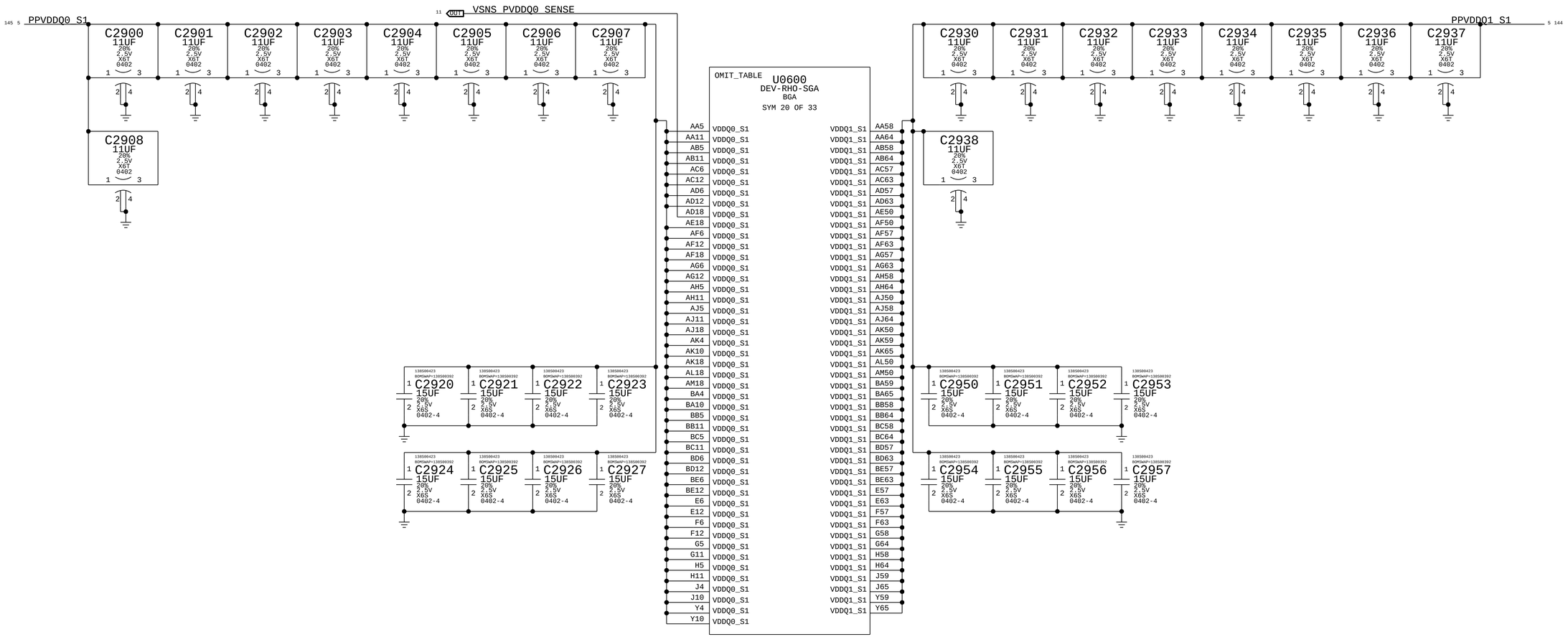
SHEET 17 OF 159



BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (VDDQ)

Apple Inc.

DRAWING NUMBER 051-08156
SIZE D
REVISION 3.0.0
BRANCH evt-1
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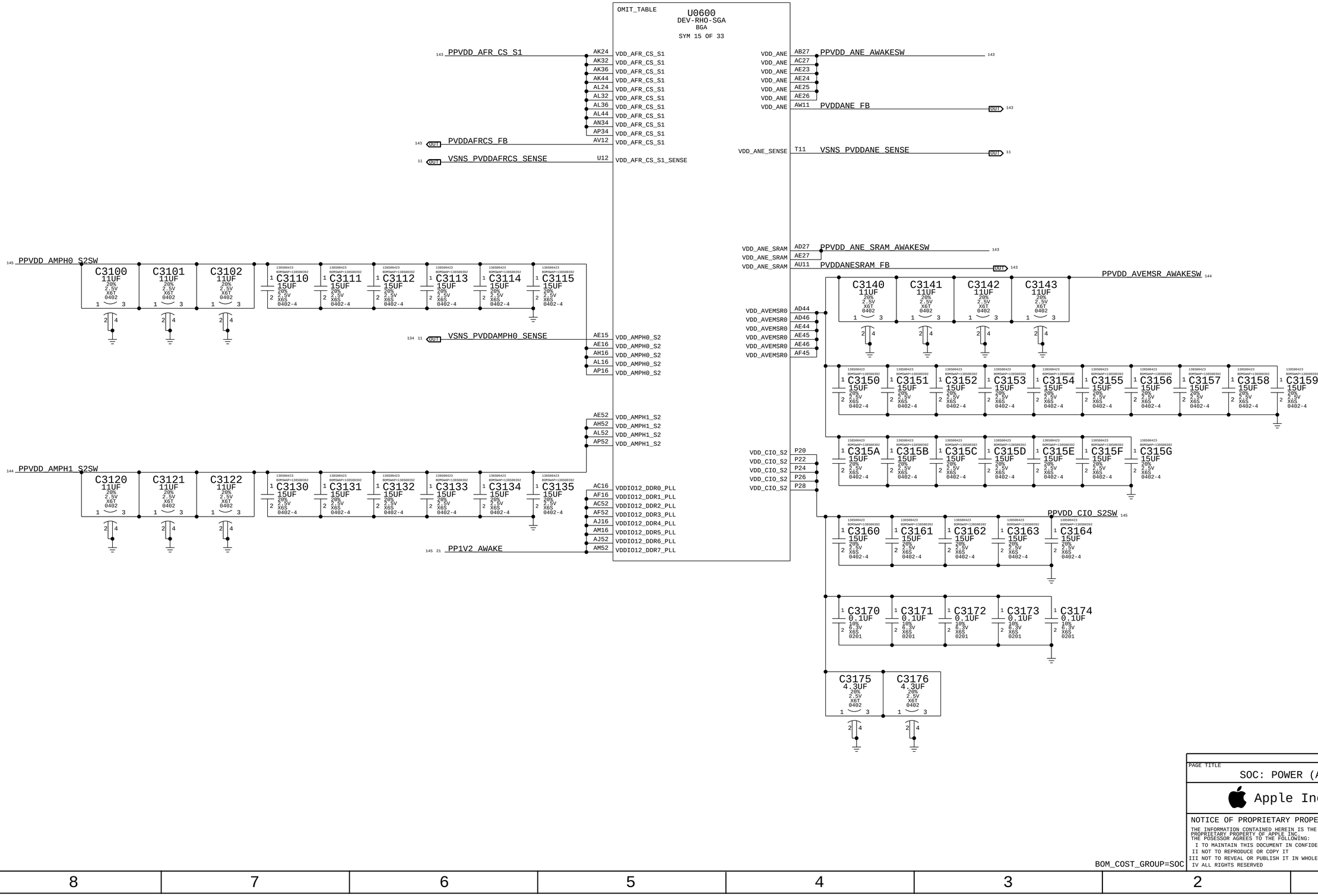

PAGE TITLE
SOC: POWER (AFR, ANE, CIO)

Apple Inc.

DRAWING NUMBER 051-08156
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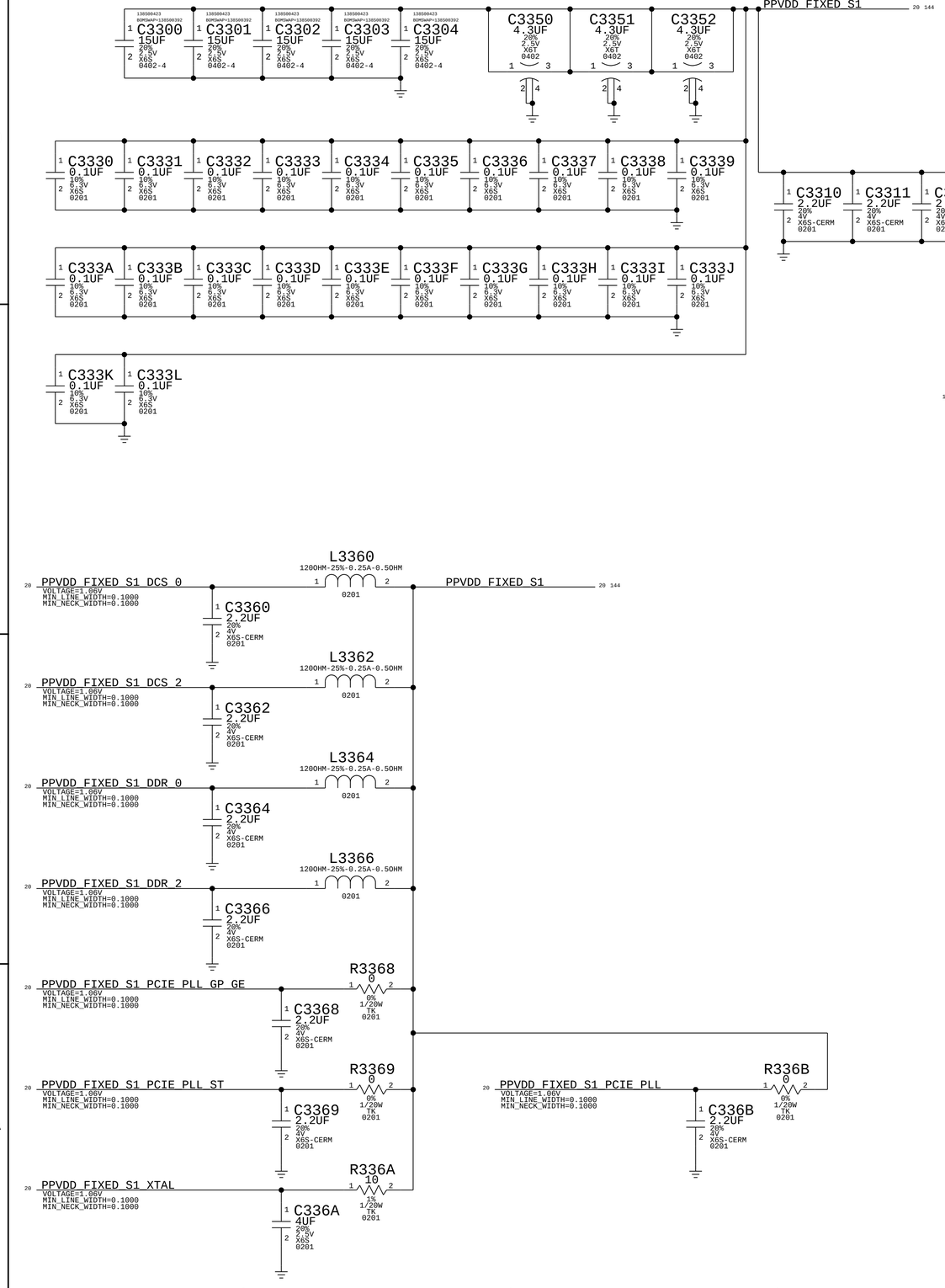
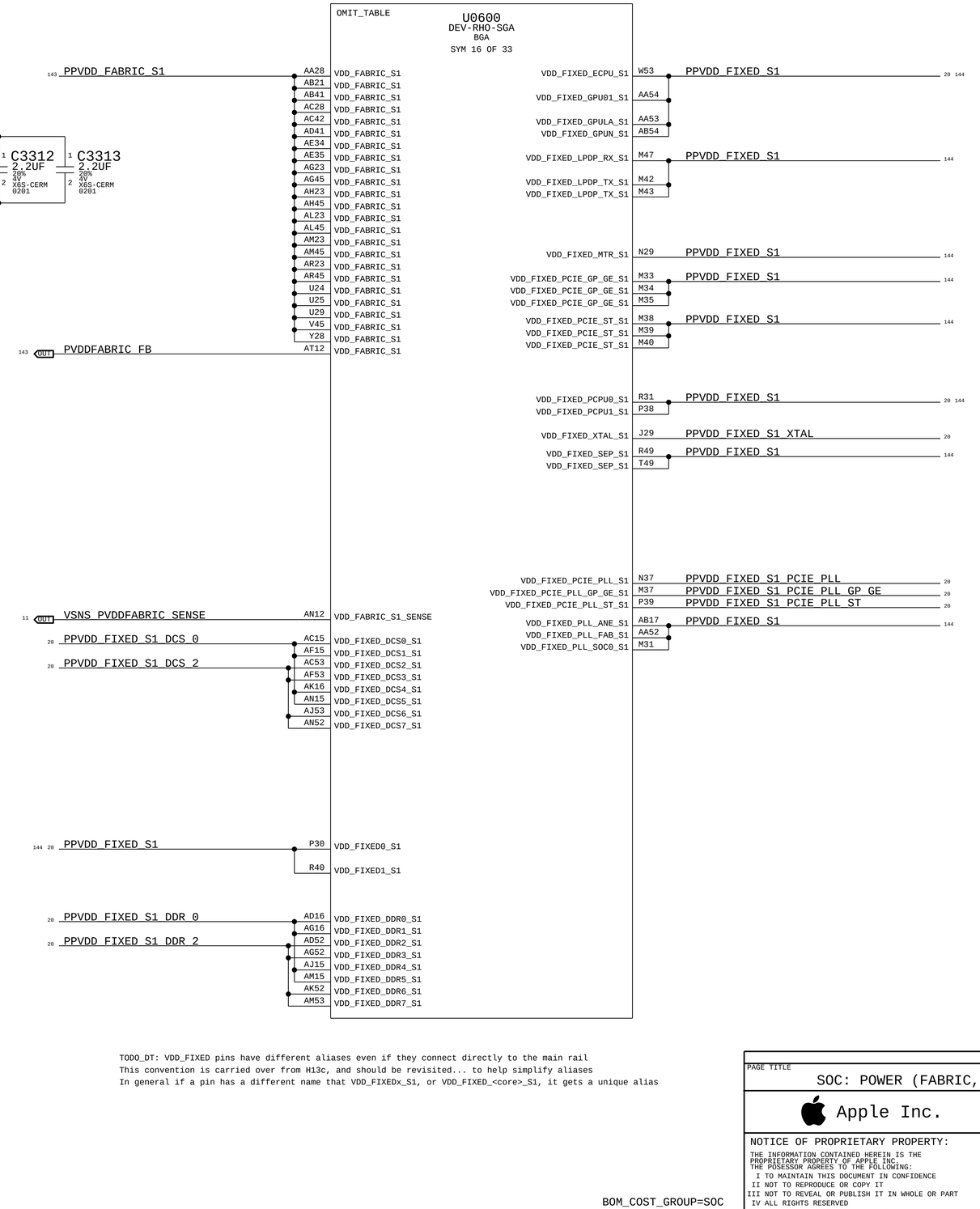
REVISION 3.0.0
BRANCH evt-1
PAGE 31 OF 700
SHEET 19 OF 159





TODO_DT: VDD_FIXED pins have different aliases even if they connect directly to the main rail
This convention is carried over from H13c, and should be revisited... to help simplify aliases
In general if a pin has a different name that VDD_FIXEDx_S1, or VDD_FIXED_<core>_S1, it gets a unique alias

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (FABRIC, FIXED)

Apple Inc.

DRAWING NUMBER 051-08156 | SIZE D
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BRANCH evt-1
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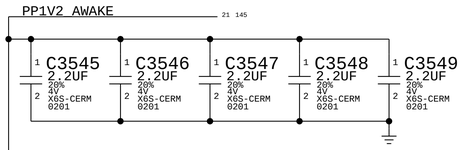
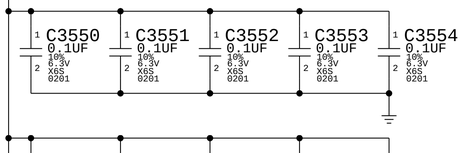
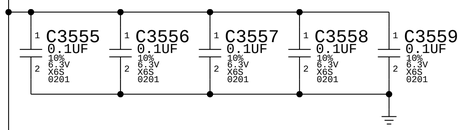
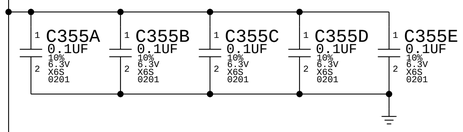
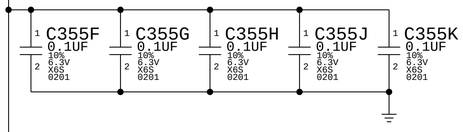
SHEET 20 OF 159

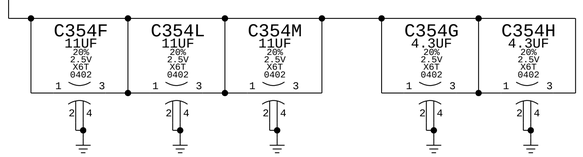


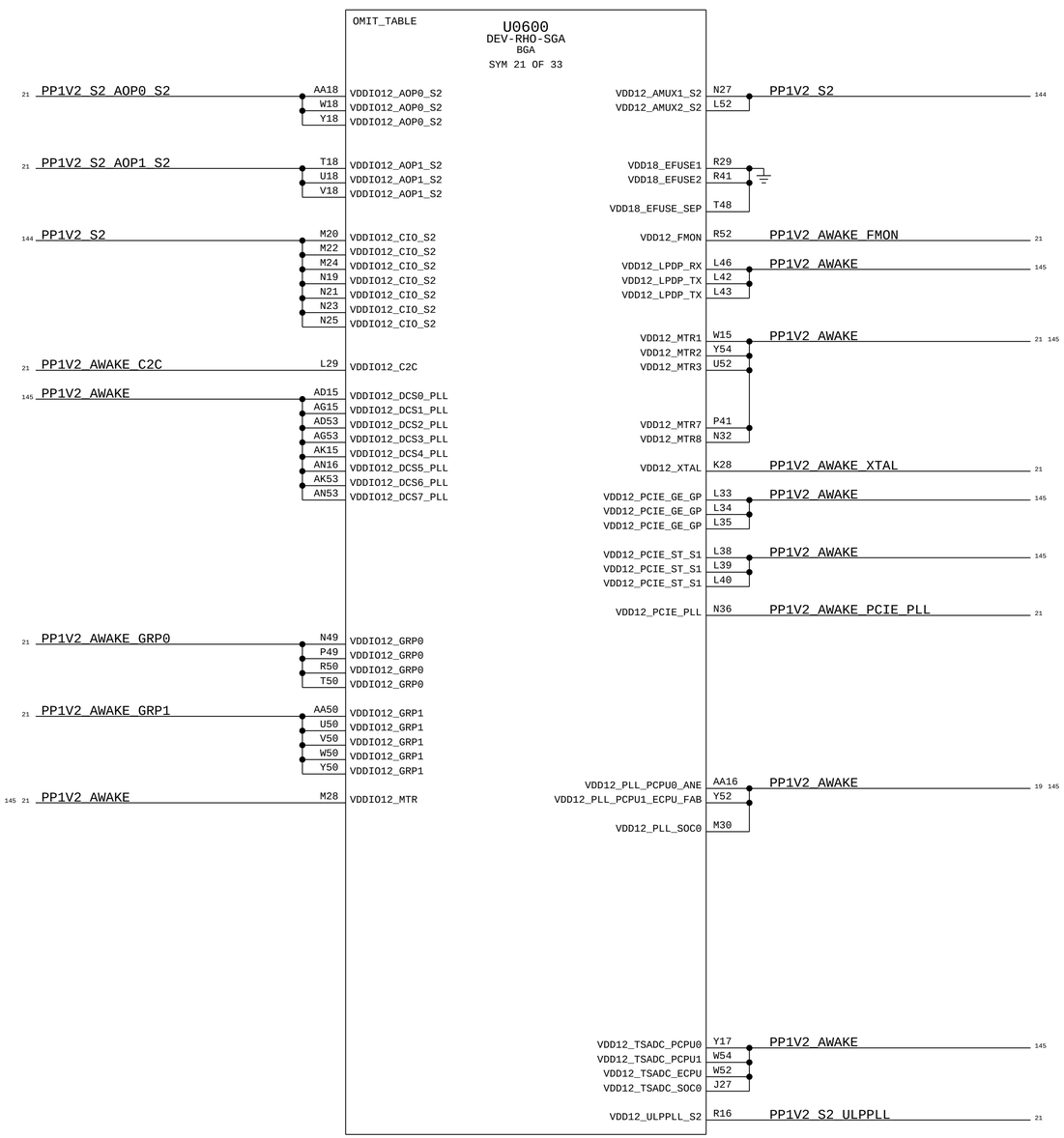


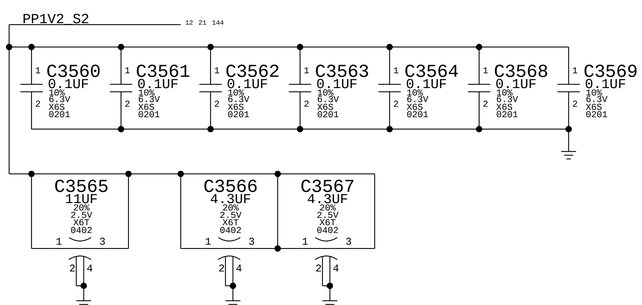


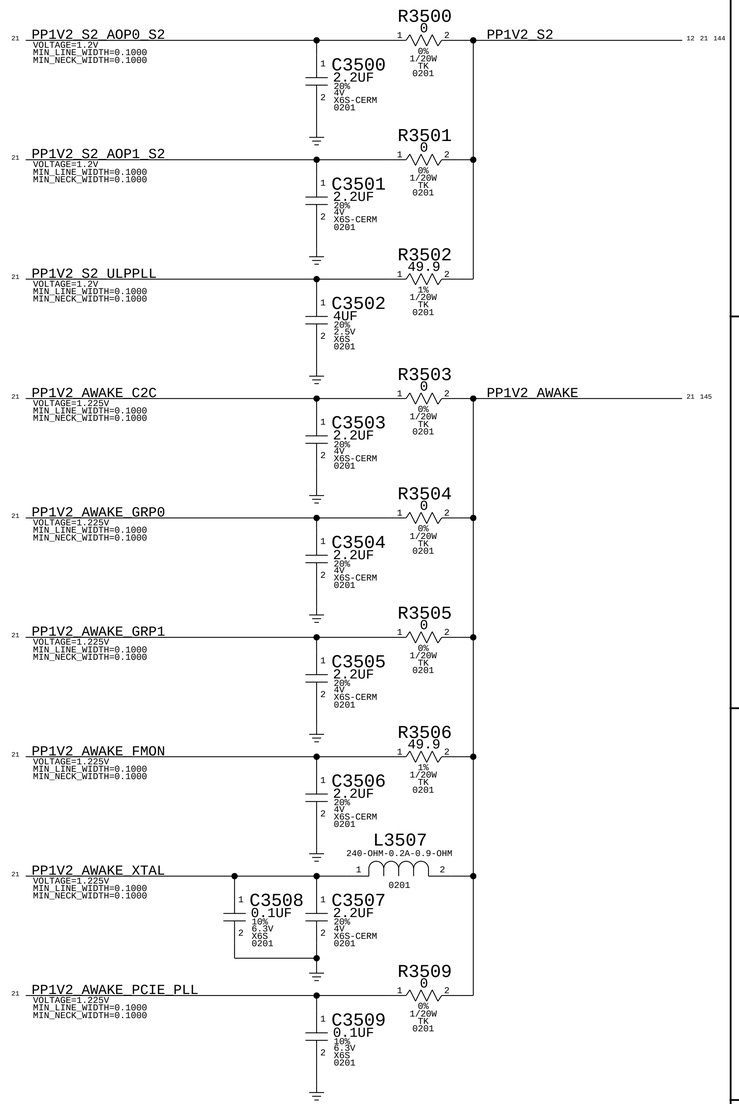












BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (VDDIO)

Apple Inc.

DRAWING NUMBER 051-08156
SIZE D
REVISION 3.0.0
BRANCH evt-1
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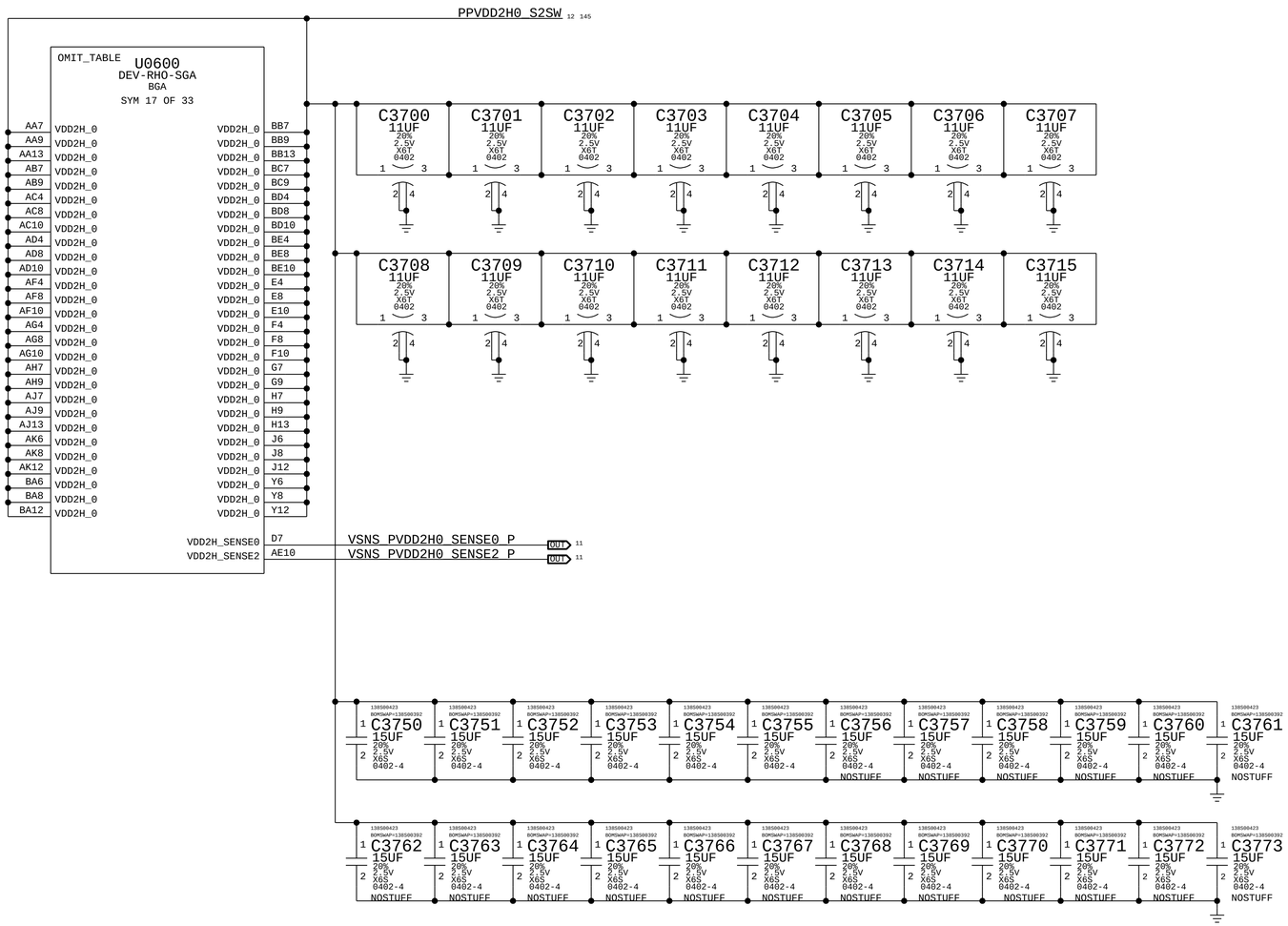

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (VDD2H0)

Apple Inc.

DRAWING NUMBER 051-08156
SIZE D
REVISION 3.0.0
BRANCH evt-1
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PPVDD2H1_S2SW 144

U0600
DEV-RHO-SGA
BGA
SYM 18 OF 33
OMIT_TABLE

AA56	VDD2H_1	BB56	VDD2H_1
AA60	VDD2H_1	BB60	VDD2H_1
AA62	VDD2H_1	BB62	VDD2H_1
AB60	VDD2H_1	BC60	VDD2H_1
AB62	VDD2H_1	BC62	VDD2H_1
AC59	VDD2H_1	BD59	VDD2H_1
AC61	VDD2H_1	BD61	VDD2H_1
AC65	VDD2H_1	BD65	VDD2H_1
AD59	VDD2H_1	BE59	VDD2H_1
AD61	VDD2H_1	BE61	VDD2H_1
AD65	VDD2H_1	BE65	VDD2H_1
AF59	VDD2H_1	E59	VDD2H_1
AF61	VDD2H_1	E61	VDD2H_1
AF65	VDD2H_1	E65	VDD2H_1
AG59	VDD2H_1	F59	VDD2H_1
AG61	VDD2H_1	F61	VDD2H_1
AG65	VDD2H_1	F65	VDD2H_1
AH60	VDD2H_1	G60	VDD2H_1
AH62	VDD2H_1	G62	VDD2H_1
AJ60	VDD2H_1	H56	VDD2H_1
AJ62	VDD2H_1	H60	VDD2H_1
AK57	VDD2H_1	H62	VDD2H_1
AK61	VDD2H_1	J57	VDD2H_1
AK63	VDD2H_1	J61	VDD2H_1
BA57	VDD2H_1	J63	VDD2H_1
BA61	VDD2H_1	Y57	VDD2H_1
BA63	VDD2H_1	Y61	VDD2H_1
		Y63	VDD2H_1
	VDD2H_SENSE1	D64	VSNS_PVDD2H1_SENSE1_P OUT 11
	VDD2H_SENSE3	AE63	VSNS_PVDD2H1_SENSE3_P OUT 11

C3900 C3901 C3902 C3903 C3904 C3905 C3906 C3907
11UF 20% 2.5V X6T 0402 1 3 2 4

C3908 C3909 C3910 C3911 C3912 C3913 C3914 C3915
11UF 20% 2.5V X6T 0402 1 3 2 4

C3950 C3951 C3952 C3953 C3954 C3955 C3956 C3957 C3958 C3959 C3960 C3961
15UF 20% 2.5V X6S 0402-4 1 2 NOSTUFF

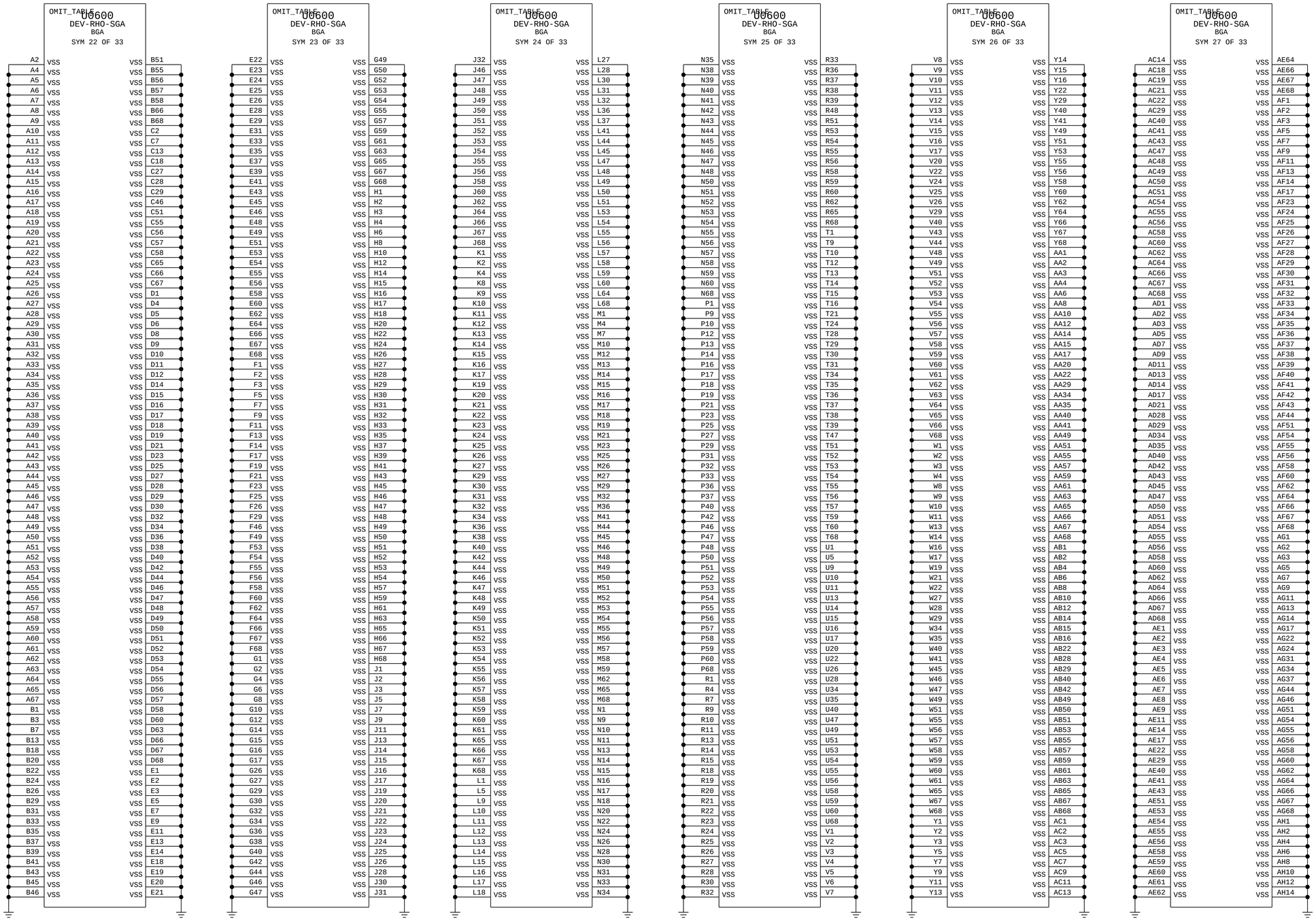
C3962 C3963 C3964 C3965 C3966 C3967 C3968 C3969 C3970 C3971 C3972 C3973
15UF 20% 2.5V X6S 0402-4 1 2 NOSTUFF

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (VDD2H1)

Apple Inc.

DRAWING NUMBER 051-08156
SIZE D
REVISION 3.0.0
BRANCH evt-1
PAGE 39 OF 700
SHEET 23 OF 159

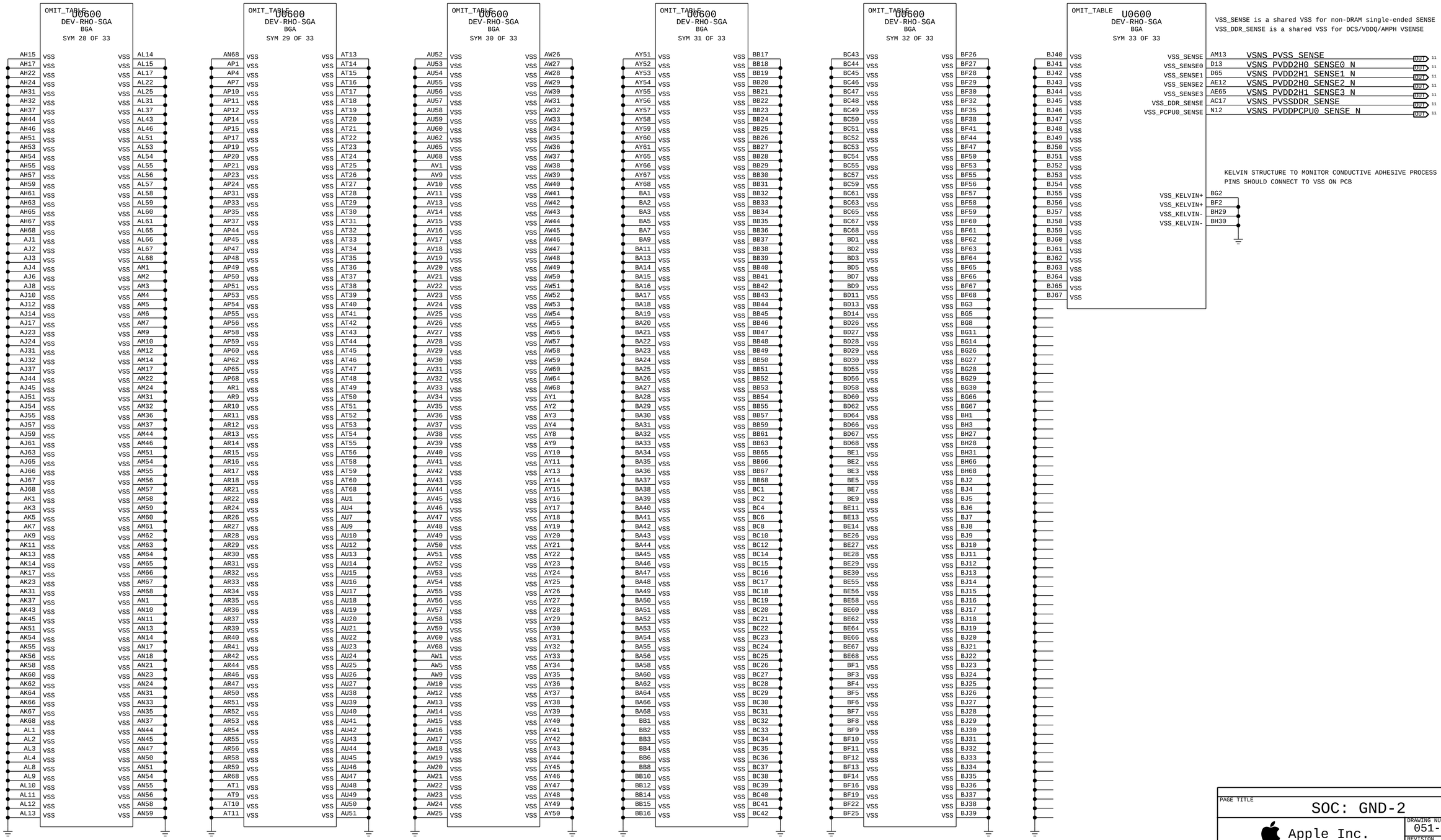


BOM_COST_GROUP=SOC

PAGE TITLE
SOC: GND-1

Apple Inc.

DRAWING NUMBER 051-08156
SIZE D
REVISION 3.0.0
BRANCH evt-1
PAGE 41 OF 700
SHEET 24 OF 159



BOM_COST_GROUP=SOC

PAGE TITLE: SOC: GND-2

Apple Inc.

DRAWING NUMBER: 051-08156 | SIZE: D
REVISION: 3.0.0
BRANCH: evt-1
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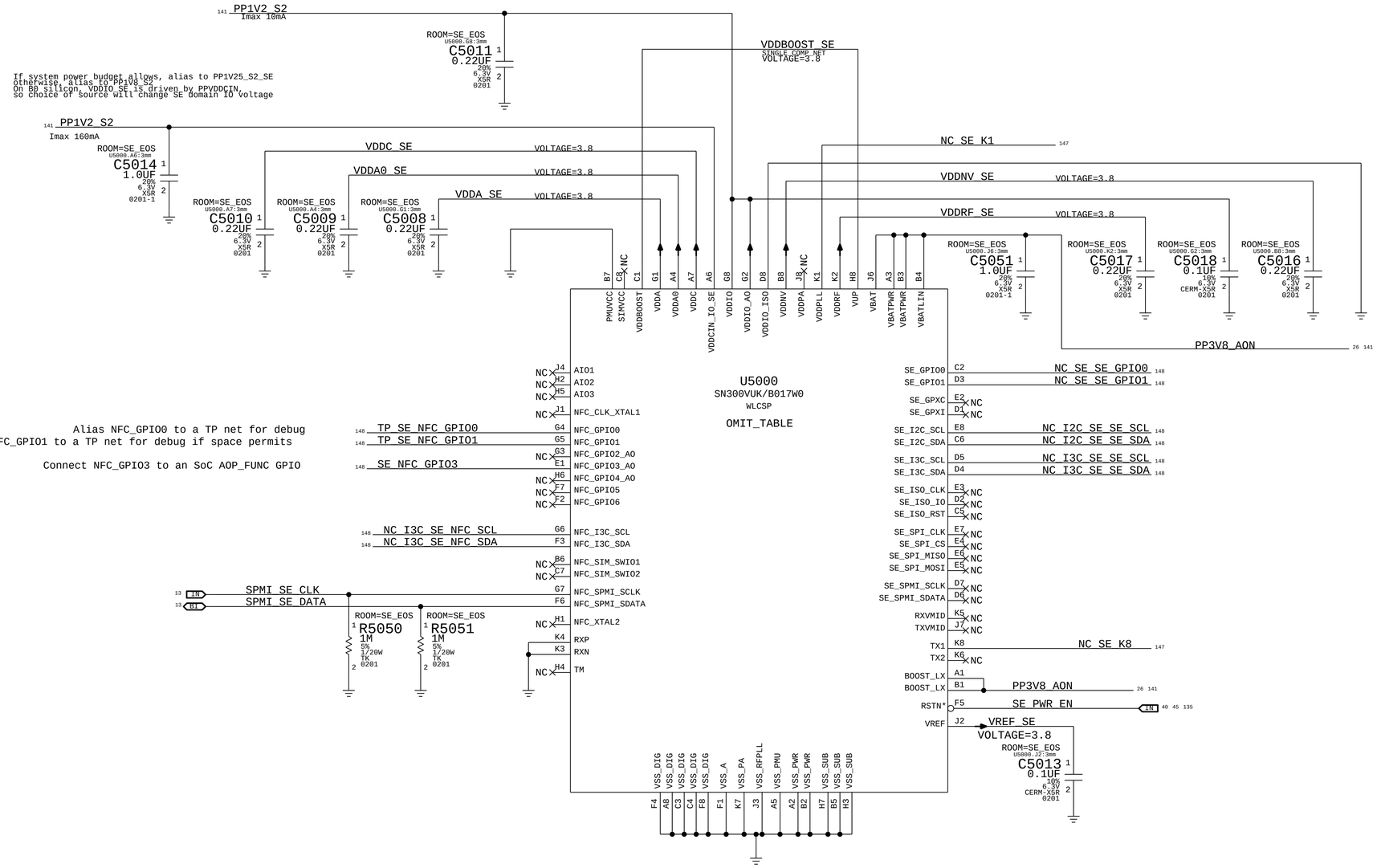
Eos - Secure Element



SE and NFC GPIO, I2C, and I3C are not used on the architectural roadmap as of 9/15/21 and should be NC'd on all form factor designs, with the exception of NFC_GPI01/2/3 per inline notes

Support for Eos A1 Silicon has been removed from the reference design following V0.1.0

<rdar://problem/59254645> [SN300V] Data Sheet
<rdar://problem/71610778> [SN300V] Wired Mode SE Only Reference Design Material

BOM_COST_GROUP=SECURE ELEMENT

PAGE TITLE: Secure Element

Apple Inc.

DRAWING NUMBER: 051-08156
SIZE: D
REVISION: 3.0.0
BRANCH: evt-1
PAGE: 50 OF 700
SHEET: 26 OF 159

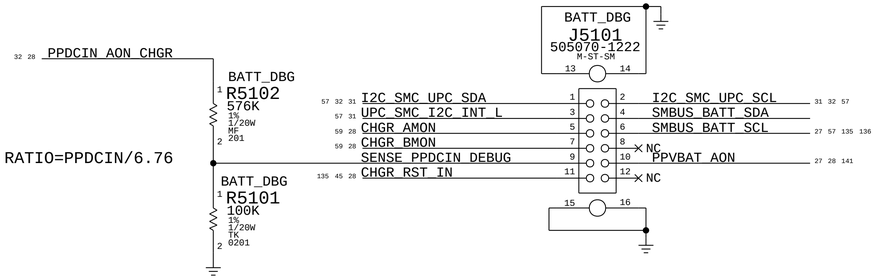
Battery Sub-System Debug Connector

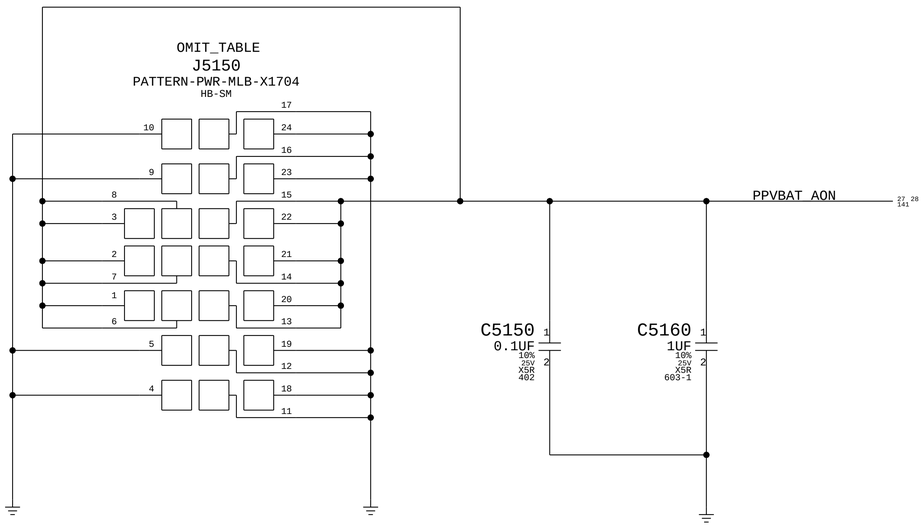
ARKANOID CONN

BMU POWER FLEX HOTBAR'd TO THE MLB:

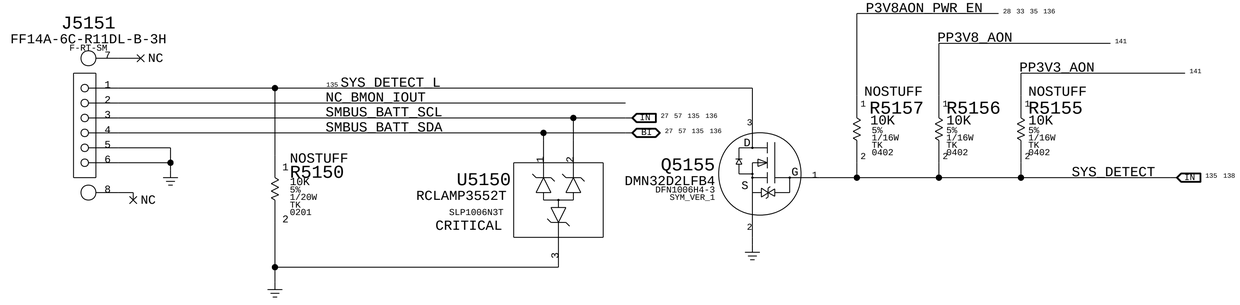
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-04146	1	PCBA,FLEX,BMU-POWER,X1703	J5150	CRITICAL	

ARKANOID	MLB Connector / Signals		Saleae
J0301 - 1	6	SMBUS_BATT_SCL (= I2C_SMC_PWR_SCL)	0
J0301 - 3	4	SMBUS_BATT_SDA (= I2C_SMC_PWR_SDA)	1
J0301 - 5	2	I2C_SMC_UPC_SCL	2
J0301 - 7	1	I2C_SMC_UPC_SDA	3
J0302 - 1	3	UPC_SMC_I2C_INT_L	4
J0302 - 3	5	CHGR_AMON	5
J0302 - 5	7	CHGR_BMON	6
J0302 - 7	9	1 / 6.76 * PPDCIN_AON	7
J0303 - 1	11	CHGR_RST_IN	8
J0303 - 3	12	—	9
J0303 - 5	10	PPVBAT_AON	10
J0303 - 7	8	—	11





APN:518S0818



BOM_COST_GROUP=BATTERY

PAGE TITLE: BATTERY CONN

Apple Inc.

DRAWING NUMBER	051-08156
SIZE	D
REVISION	3.0.0
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BOM_COST_GROUP=BATTERY

PAGE TITLE
PBUS SUPPLY & BATTERY CHARGER

Apple Inc.

DRAWING NUMBER	051-08156
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REVISION	3.0.0
BRANCH	evt-1
PAGE	52 OF 700
SHEET	28 OF 159

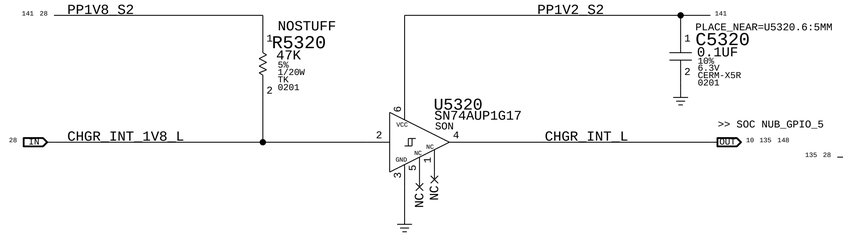
*** OK2PLACE ***

CHGR I2C Level Translation

SMBUS_CHGR_1V8_[SCL/SDA]: Level translation circuit to be placed in project specific I2C page.

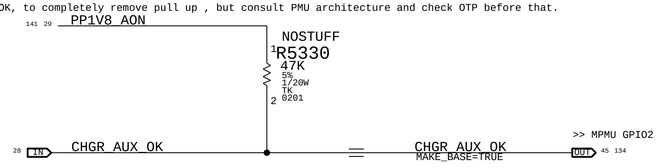
CHGR_INT_L Level Translation

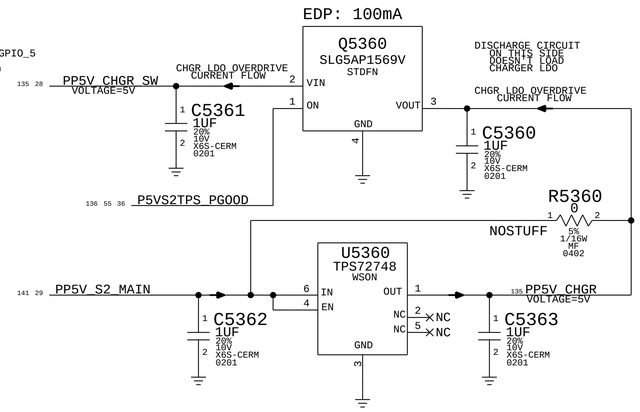
Stuff R5320 in case, glitch during power sequencing is a concern.

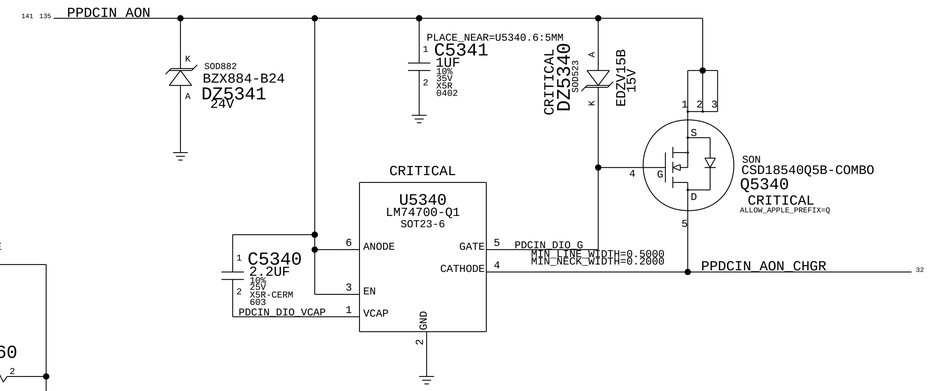


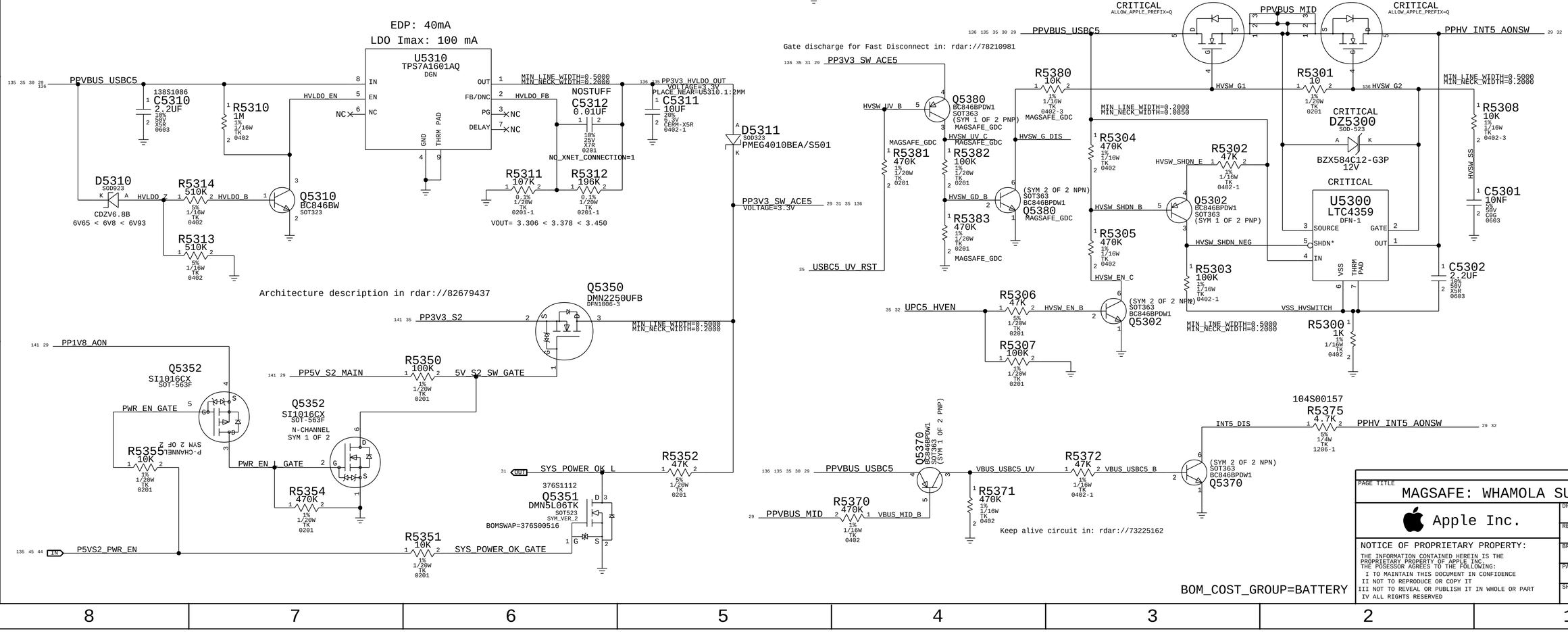
CHGR_AUX_OK Pull Up

Pull up to MPMU LDO9, or rely on MPMU internal pull up.
OK, to completely remove pull up , but consult PMU architecture and check OTP before that.









Architecture description in rdar://82679437

Gate discharge for Fast Disconnect in: rdar://78210981

BOM_COST_GROUP=BATTERY

PAGE TITLE: MAGSAFE: WHAMOLA SUPPORT

Apple Inc.

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BRANCH	evt-1
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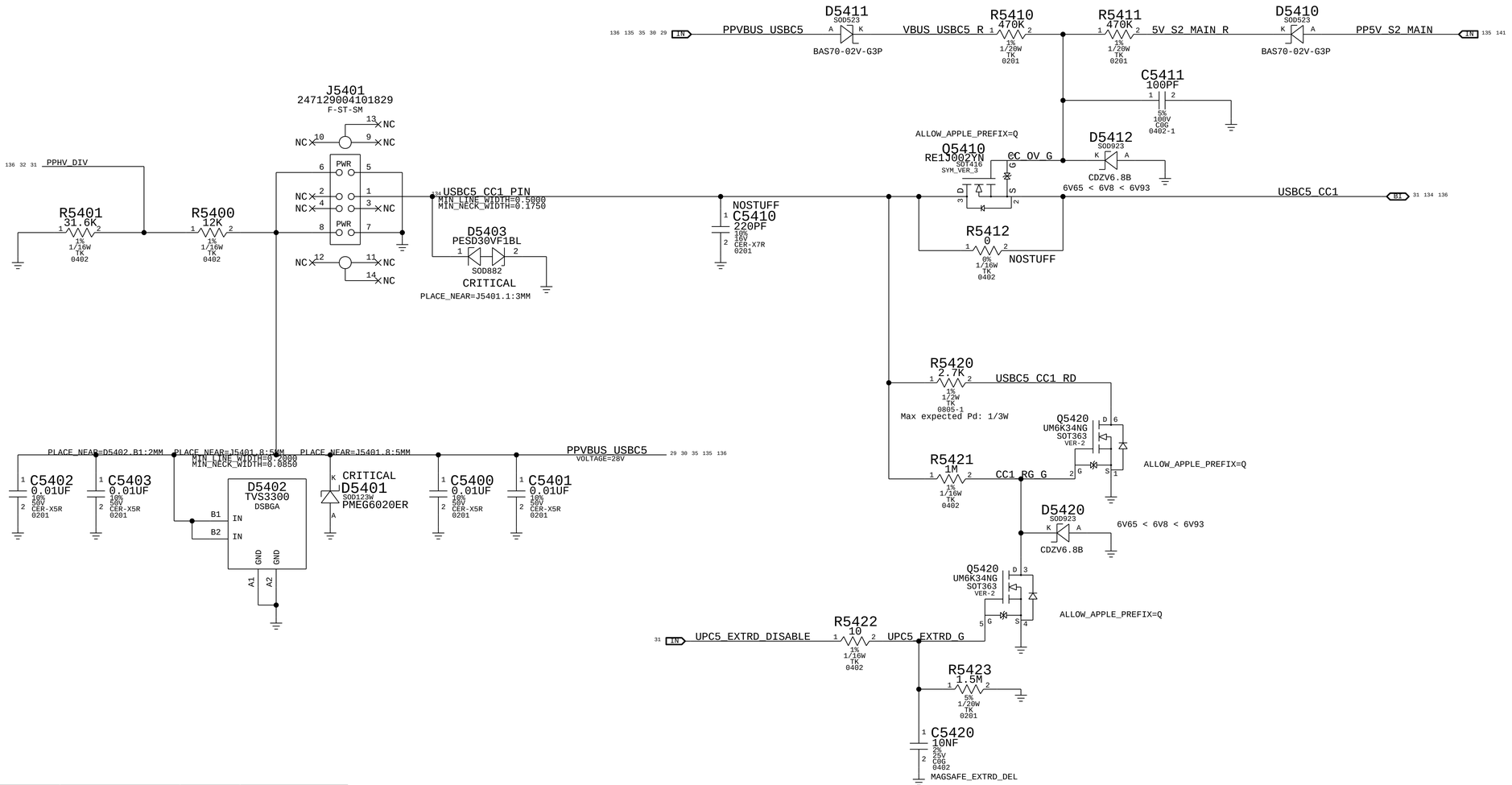
SHEET	29 OF 159

** OK2PLACE **

MAGSAFE MLB connector, CC OV and External RD



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0516	1	UVLO set RH=750K	R5215	CRITICAL	SUONA_UVLO
118S0236	1	UVLO set RL=255K	R5216	CRITICAL	SUONA_UVLO
118S00393	1	UVLO set RH=787K	R5215	CRITICAL	WHAMOLA_UVLO
118S00358	1	UVLO set RL=158K	R5216	CRITICAL	WHAMOLA_UVLO
353S02781	1	IC,RAA489900,PMIC,WHAMOLA,OTP-4,WCSP40	U5200	CRITICAL	WHAMOLA:1A
353S02937	1	IC,RAA489900,PMIC,WHAMOLA,OTP-5,WCSP40	U5200	CRITICAL	WHAMOLA:1_4A

BOM_COST_GROUP=MAGSAFE

PAGE TITLE: MAGSAFE: CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-08156 SIZE: D
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BRANCH: evt-1
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** OK2PLACE **


Configured as UPC5 (the 6th slot)
POR, ACE_WILL_BE_OTPED:YES -> I2C_ADDR=Float, I2CM_SCL_CNFG=HIGH, SDA=LOW
P0, ACE_WILL_BE_OTPED:NO -> I2C_ADDR=84.5k, I2CM_SCL_CNFG=HIGH, SDA=HIGH
PP3V3_UPC5_LDO
R5507 10K 5% 1/20W TK 0201 UPC5_GPIO2
R5509 1M 5% 1/20W TK 0201 I2C_UPC5_SCL CKPLUS_WAIVE=I2C_PULLUP
R5504 1M 5% 1/20W TK 0201 I2C_UPC5_SDA CKPLUS_WAIVE=I2C_PULLUP
ACE_WILL_BE_OTPED:NO
R5508 1M 5% 1/20W TK 0201
ACE_WILL_BE_OTPED:YES
R5510 84.5K 1% 1/20W TK 0201 UPC5_I2C_ADDR
ACE_WILL_BE_OTPED:NO
R5505 1M 5% 1/20W TK 0201 UART_UPC5
R5506 100K 5% 1/20W TK 0201 UPC5_MRESET
R5502 0 0% 1/20W TK 0201 UPC5_HRESET
CRITICAL R5503 15K 0.1% 1/20W TK 0201
GND_I2C_ADDR PRIMARY ONLY
PPHV_DIV
NOSTUFF C5504 1UF 10% 35V X5R 0402
PD_ACE5_VCONN
PD_ACE5_VCONN
CAP FOR PP_5V0 ON VR PAGE
PP_5V0 PP_CABLE PP_HV VBUS
U5500 CD3218B12ACE2 FCBGA
OMIT_TABLE CRITICAL
UPC5_HRESET B13 HRESET
UPC5_MRESET A14 MRESET
NC_UPC5_RESET_L B17 RESET*
UPC5_SER_DBG A2 B1 GPIO0
SYS_POWER_OK_L D1 GPIO1
UPC5_GPIO2 F1 GPIO2
UPC5_EXTRD_DISABLE C2 GPIO3
UPC5_HVEN_SENSE E2 GPIO4
UPC5_HVEN_ACE B3 GPIO5
UPC5_GPIO6 C4 GPIO6
UPC5_GPIO7 D3 GPIO7
UPC5_GPIO8 E4 GPIO8
UPC5_GPIO9 F3 GPIO9
UPC5_GPIO10 F7 GPIO10
GND A18 BUSPOWER
UPC5_I2C_ADDR M19 I2C_ADDR IPU-BOOT
UPC5_R_OSC M21 R_OSC
I2C_UPC5_SDA A16 I2CM_SDA_CNFG
I2C_UPC5_SCL B15 I2CM_SCL_CNFG
I2C_UPC_SDA B5 I2C_SDA1
I2C_UPC_SCL A4 I2C_SCL1
UPC_I2C_INT_L D7 I2C_IRQ1*
I2C_SMC_UPC_SDA B7 I2C_SDA2
I2C_SMC_UPC_SCL A6 I2C_SCL2
UPC_SMC_I2C_INT_L C8 I2C_IRQ2*
SPI_UPC5_R_CLK B9 SPI_CLK
SPI_UPC5_R_MOSI B11 SPI_MOSI
SPI_UPC5_R_MISO A10 SPI_MISO
SPI_UPC5_R_CS_L A8 SPI_SSZ
SWD_UPC_SWDIO2 E20 SWD_DATA IPU
SWD_UPC_SWCLK1 E16 SWD_CLK IPU
UART_UPC5 B19 UART_RX
UART_UPC5 A20 UART_TX
PD_UPC5_USB_RP H19 USB_RP1_P
PD_UPC5_USB_RP H21 USB_RP1_N
PD_UPC5_USB_RP G20 USB_RP2_P
PD_UPC5_USB_RP G22 USB_RP2_N
PD_UPC5_USB_RP F19 USB_RP3_P
PD_UPC5_USB_RP F21 USB_RP3_N
PD_UPC5_PORT_MUX J12 AUX_P
PD_UPC5_PORT_MUX H11 AUX_N
PD_UPC5_HPD C12 HPD
PD_UPC5_DBG_R G12 DEBUG0
PD_UPC5_DBG_R F11 DEBUG1
PD_UPC5_DBG_R E8 DEBUG2
PD_UPC5_DBG_R E12 DEBUG3
PD_UPC5_DBG_R G16 DEBUG4
PD_UPC5_DBG_R F15 DEBUG5
PD_UPC5_DBG_R D15 DEBUG6
PD_UPC5_DBG_R D19 DEBUG7
DIGITAL CORE I/O & CONTROL
POWER
TYPE-C
PORT_MUX
GND
VIN_3V3 C20
VDDIO A12
VDDIO_CFG D11 GND
LDO_3V3 C22 D21
VIN_LV L20 UPC5_LV
VOUT_LV L18
VRET C16
SS L22 UPC5_SS
LDO_CORE E22 PP1V5_UPC5_LDO_CORE
VBUS_OPT D5 NC_PPVBUS_USBC5_OPT FLOATING?
PP_HV_OPT F5 PPHV_DIV HOOKED TO PPHV_DIV
C_CC1 M15 N16 USBC5_CC1
C_CC2 M17 N18 USBC5_CC2
RPD_G1 L14 GND
RPD_G2 L16 GND
C_USB_TP K19 USBC5_WPD
C_USB_TN K21 USBC5_WPD
C_USB_BP J20 USBC5_WPD
C_USB_BN J22 USBC5_WPD
C_SBU1 J16 USBC5_WPD
C_SBU2 H15 USBC5_WPD
GND_OPT C18
GND_OPT E18
GND_OPT D17
GND_OPT G18
GND A22 H9 N20 B21 K15 N22
TP_PPVBUS_USBC5
R5500 1K 1% 1/16W TK 0402
NOSTUFF C5501 1UF 10% 35V X5R 0402
PP3V3_SW_ACE5
C5500 10UF 20% 6.3V CERM 0402
PP1V2_S2
C5502 1.0UF 20% 6.3V X5R 0201-1
MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.0850
VOLTAGE=3.3V
PP3V3_UPC5_LDO
C5508 10UF 20% 6.3V CERM 0402
R5501 1K 1% 1/16W TK 0402
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.0850
C5505 10UF 20% 6.3V CERM 0402
R5512 0 0% 1/16W TK 0402
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
NOSTUFF C5514 220PF 5% 50V C0G 0201-1
C5513 220PF 5% 50V C0G 0201-1
USBC5_WPD
USBC5_WPD MAKE_BASE=TRUE
R5511 10K 1% 1/16W TK 0402-3

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02994	1	IC,ACE2,B3,USB PWR SW,ROM3,BGA123	U5500	CRITICAL	

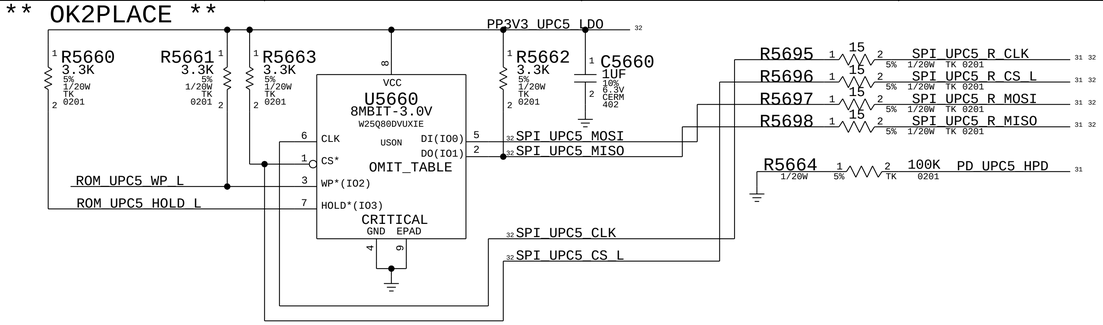
BOM_COST_GROUP=MAGSAFE

PAGE TITLE
MAGSAFE: PORT CONTROLLER

Apple Inc.

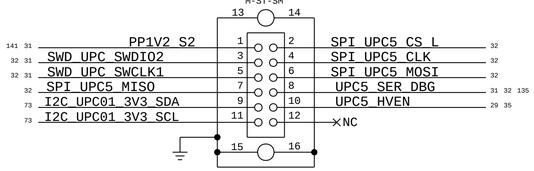
DRAWING NUMBER 051-08156 SIZE D
REVISION 3.0.0
BRANCH evt-1

** OK2PLACE **



AARDVARKANOID CONN

J5602 USBC_DBG 505070-1222 M-ST-SM



Either a Testpoint or Arkanoid connector must be present for GPI00 (EVEN IN PRODUCTION)

POWER ALIASES

NC_PPVBUS_USBC5_OPT = NC_PPVBUS_USBC5_OPT MAKE_BASE=TRUE

PPDCIN_AON_CHGR

CRITICAL 0603-1 F5601 6A-32V

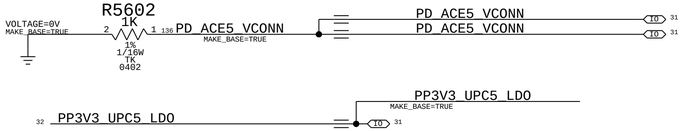
FUSES FOR UPC

PPHV_INT5_AONSW = PPHV_INT5_AONSW MAKE_BASE=TRUE VOLTAGE=28V

PLACE_NEAR=Q5301:5MM

PPHV_DIV = PPHV_DIV MAKE_BASE=TRUE

NC_UPC5_RESET_L = NC_UPC5_RESET_L MAKE_BASE=TRUE NO_TEST=1



WE DO NOT NEED HIGHER VOLTAGE RATING FOR THIS FUSE CHECKED WITH MFGR

ACE5 IS SPI ROM ONLY

SPI_UPC5_R_CLK = SPI_UPC5_R_CLK MAKE_BASE=TRUE (IN)
SPI_UPC5_R_CS_L = SPI_UPC5_R_CS_L MAKE_BASE=TRUE (IN)
SPI_UPC5_R_MOSI = SPI_UPC5_R_MOSI MAKE_BASE=TRUE (IN)
SPI_UPC5_R_MISO = SPI_UPC5_R_MISO MAKE_BASE=TRUE (OUT)

CONNECTION TO CHARGER

PPDCIN_AON_CHGR = PPDCIN_AON_CHGR

PPDCIN_AON_CHGR MAKE_BASE=TRUE VOLTAGE=28V

CCONNECTION TO SoC

I2C_SMC_UPC_SCL = I2C_SMC_UPC_SCL MAKE_BASE=TRUE (IN)
I2C_SMC_UPC_SDA = I2C_SMC_UPC_SDA MAKE_BASE=TRUE (IO)
CKPLUS_WAIVE=I2C_PULLUP

I2C_UPC_SCL = I2C_UPC_SCL MAKE_BASE=TRUE (IN)
I2C_UPC_SDA = I2C_UPC_SDA MAKE_BASE=TRUE (IO)
UPC_I2C_INT_L = UPC_I2C_INT_L MAKE_BASE=TRUE (OUT)
CKPLUS_WAIVE=I2C_PULLUP

SWD TO SoC

SWD_UPC_SWCLK1 = SWD_UPC_SWCLK1 MAKE_BASE=TRUE

SWD_UPC_SWDIO2 = SWD_UPC_SWDIO2 MAKE_BASE=TRUE

Unused ports and GPIOs

NOSTUFF

R5632 100K 5% 1/20W TK 0201 UPC5_SER_DBG
R5671 100K UPC5_GPIO6
R5672 100K UPC5_GPIO8
R5673 100K UPC5_GPIO7
R5674 100K UPC5_GPIO9
R5675 100K UPC5_GPIO10
R5620 100K PD_UPC5_DBG_R = PD_UPC5_DBG_R MAKE_BASE=TRUE
R5628 100K PD_UPC5_USB_RP = PD_UPC5_USB_RP MAKE_BASE=TRUE (BI)

PD_UPC5_PORT_MUX = PD_UPC5_PORT_MUX

PD_UPC5_PORT_MUX R5600 100K 5% 1/20W TK 0201

UART

UART_UPC5 = UART_UPC5 MAKE_BASE=TRUE

GND = GND MAKE_BASE=TRUE

GND (OUT) = GND MAKE_BASE=TRUE

ACE RPD STRAPPING

GND (BI) MAKE_BASE=TRUE

GND (BI) MAKE_BASE=TRUE

BOM_COST_GROUP=MAGSAFE

PAGE TITLE: MAGSAFE: CONTROLLER SUPPORT

Apple Inc.

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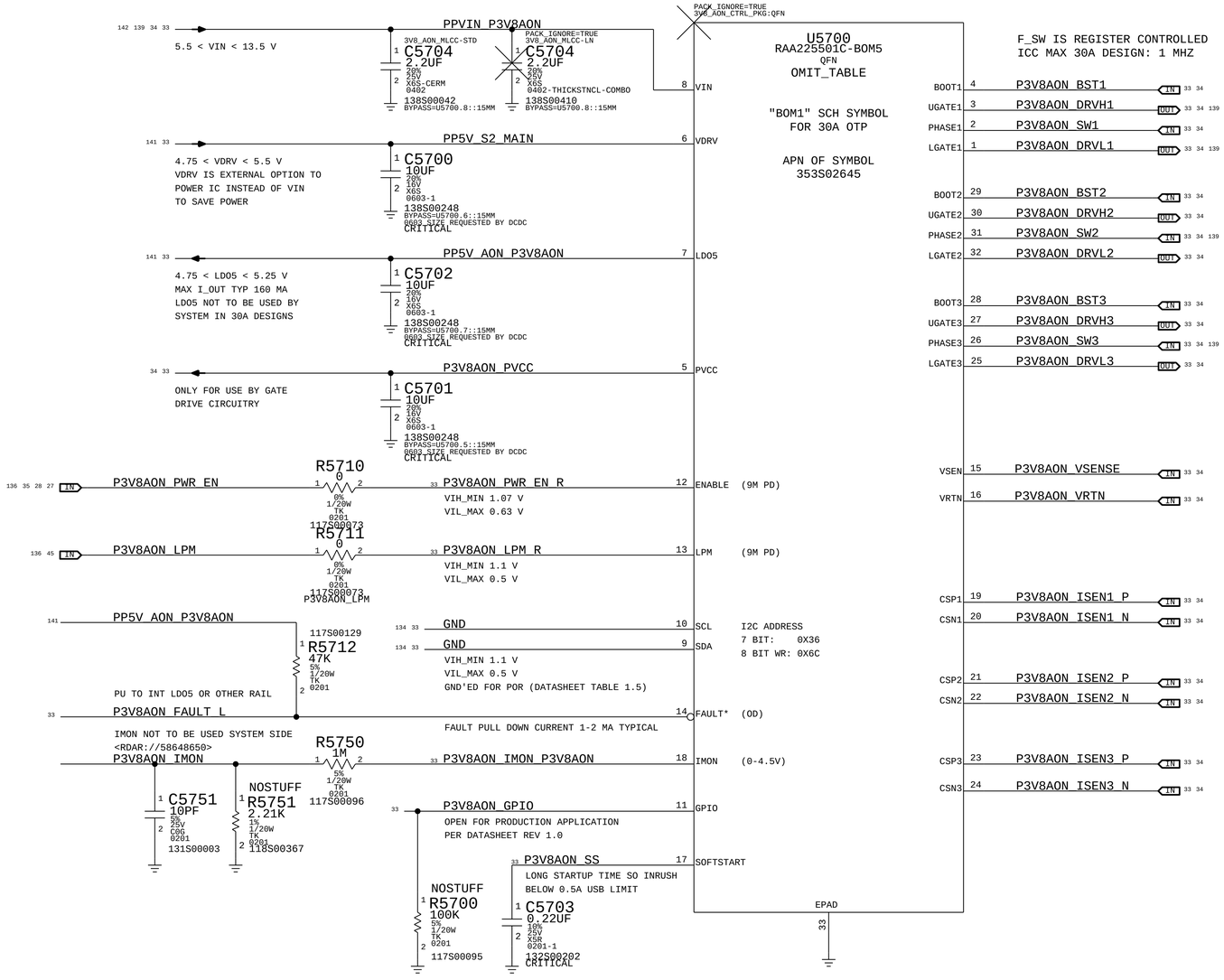
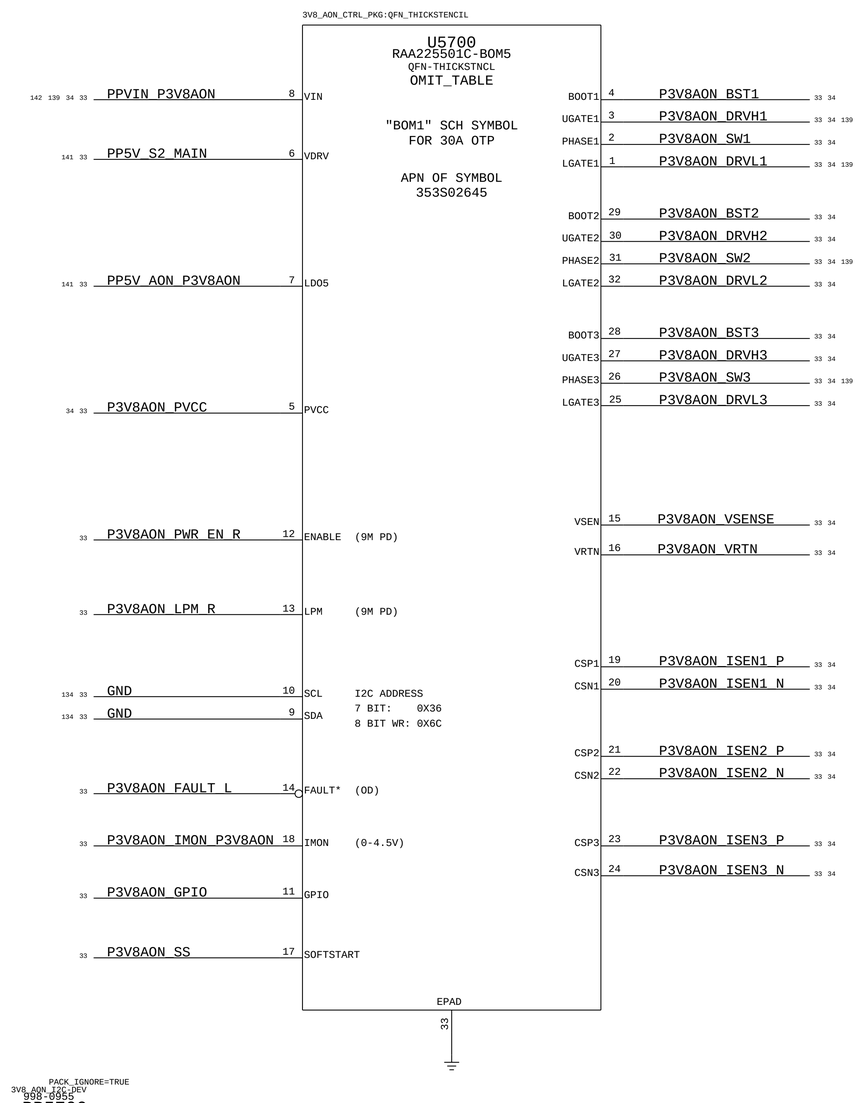
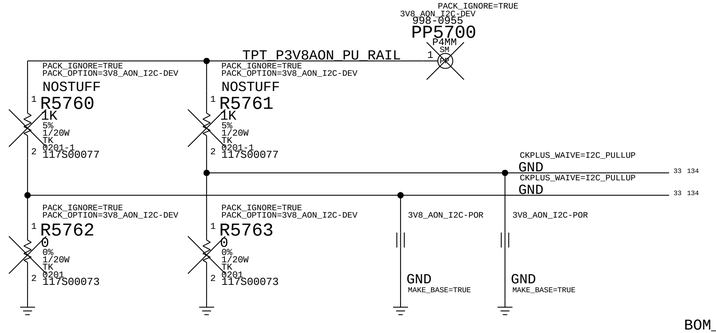
3V8 AON CONTROLLER
30A ICC MAX







30A OTP CHANGES DOCUMENTED IN <RDAR://61519509>

BOM5 IS A CONTINUATION OF BOM1 SINCE BOM1 IS FROZEN FOR TGA PROGRAMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
353S02326	1	IC,RAA225501,3-PH VOLT REG,TQFN32	U5700	CRITICAL	P3V8AON_IC:A0	
353S02472	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B0,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B0	
353S02544	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B1,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B1	
353S02560	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B2,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B2	
353S02576	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B3,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B3	
353S02592	1	IC,RAA225501B,ICE,BOM1,A2,OTP-R0B0,QFN32	U5700	CRITICAL	P3V8AON_IC:A2_R0B0	<- 30A BOM1 OTP TGA PROGRAMS ARE GOING TO RAMP WITH
353S02645	1	IC,RAA225501C,ICE,BOM5,A2,OTP-R170,QFN32	U5700	CRITICAL	P3V8AON_IC:A2_R170	<- NEW BOM5 OTP FOR FUTURE PROGRAMS

BOM_COST_GROUP=SOC POWER

PAGE TITLE
POWER: 3V8 AON (1/2)

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ICCMAX = 30 A

BOM_COST_GROUP=SOC POWER

PAGE TITLE	POWER: 3V8 AON (2/2)
	Apple Inc.
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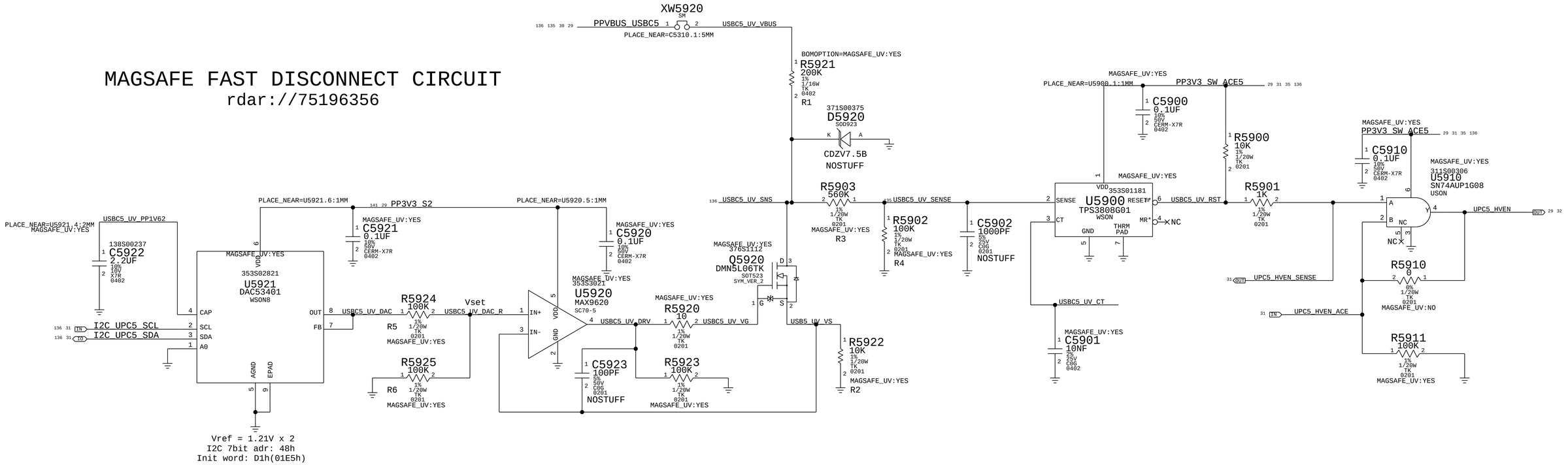
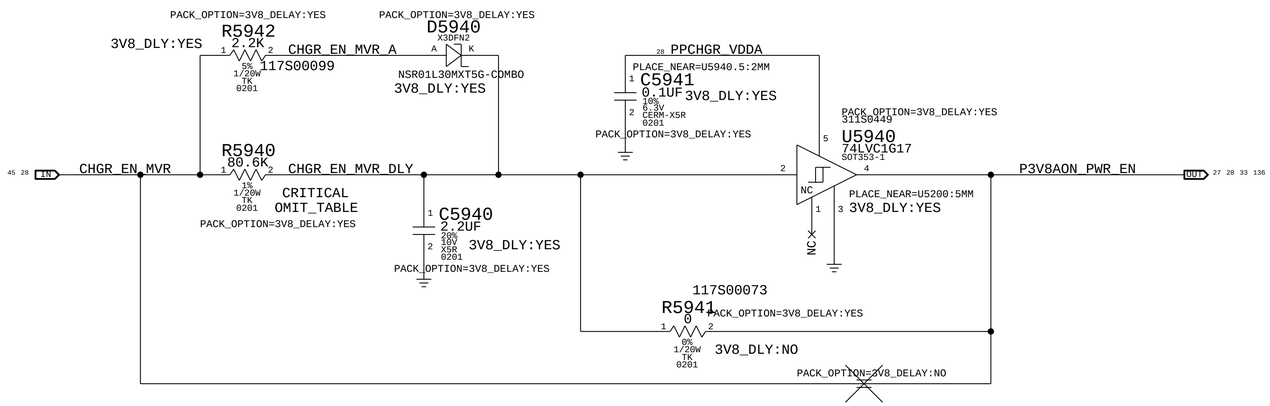
MAGSAFE FAST DISCONNECT CIRCUIT

rdar://75196356



DELAY FOR 3.8V VR ENABLE

R5340 and C5340 updated per rdar://62686034



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S00505	1	RES,TK,80.6KOHM,1%,1/20W,0201	R5940	CRITICAL	3V8_DLY:YES
117S0201	1	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	R5940	CRITICAL	3V8_DLY:NO

BOM_COST_GROUP=MAGSAFE

PAGE TITLE: MAGSAFE: VBUS UV

Apple Inc.

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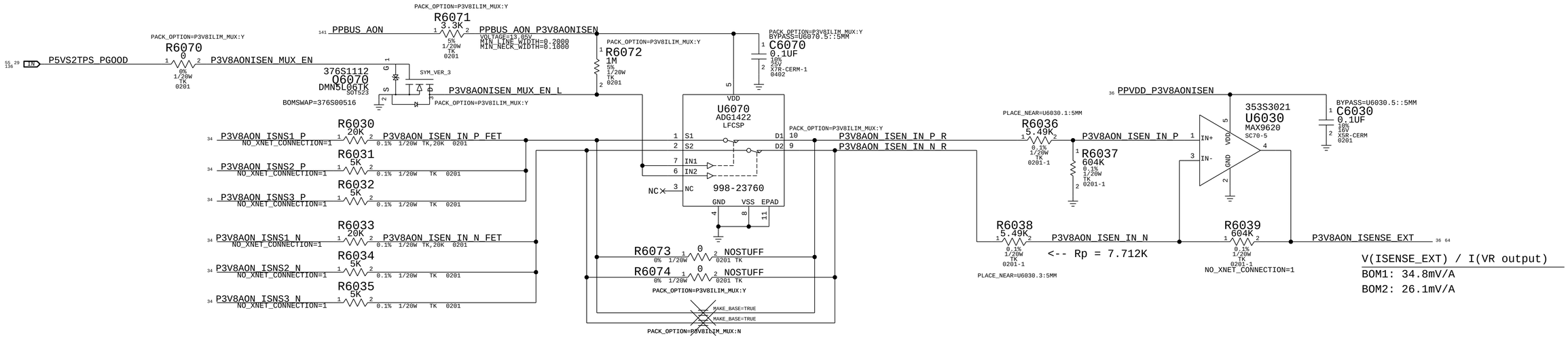
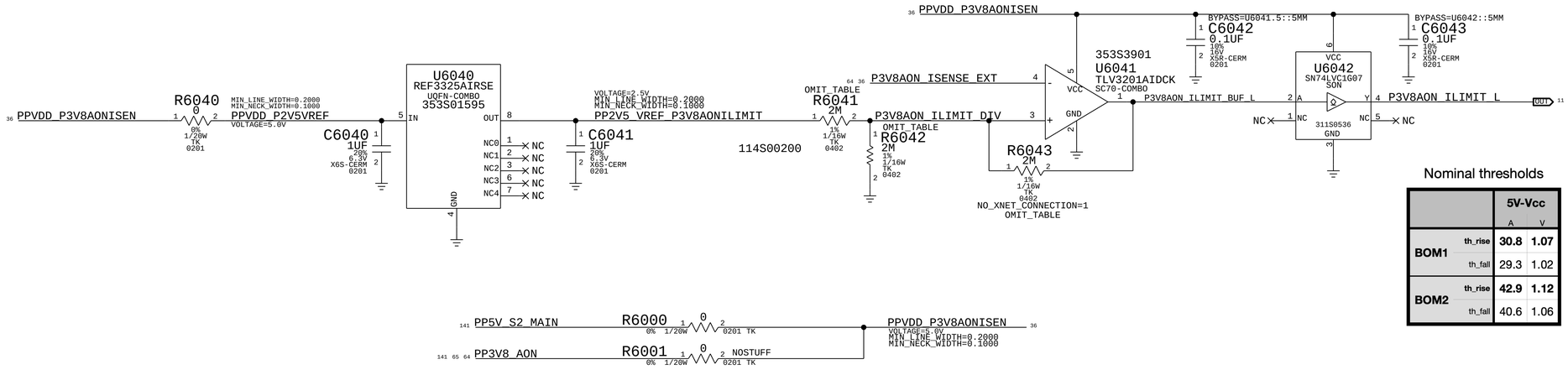
P3V8 LOW SIDE ISENSE AND ILIMIT (SUMMING AMP FOR 3 PHASES)

rdar://problem/69466996 Iceman Throttle Design Data

10A MAX ON PHASE 1, MAX TOTAL CURRENT SENSE @ PMU= 43.11A



PHASE 1 VSENSE GAIN: 8.75
PHASE 2/3 VSENSE GAIN: 35
4:1 WEIGHT FOR PHASE 1 RTREE



Nominal thresholds

		5V-Vcc	
		A	V
BOM1	th_rise	**30.8**	**1.07**
	th_fall	29.3	1.02
BOM2	th_rise	**42.9**	**1.12**
	th_fall	40.6	1.06

Call one of these BOM GROUPs in the main BOM:

BOM GROUP	BOM OPTIONS
P3V8ILIM:BOM1_5V	P3V8ILIM_RT:22K,P3V8ILIM_RB:15K4,P3V8ILIM_RF:866K
P3V8ILIM:BOM2_5V	P3V8ILIM_RT:20K,P3V8ILIM_RB:15K,P3V8ILIM_RF:715K

Don't Call these OPTIONs directly:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S00178	1	RES,0402,1%,1/16W,20K	R6041	P3V8ILIM_RT:20K
114S00277	1	RES,0402,1%,1/16W,22K	R6041	P3V8ILIM_RT:22K
114S00177	1	RES,0402,1%,1/16W,15K	R6042	P3V8ILIM_RB:15K
114S00201	1	RES,0402,1%,1/16W,15.4K	R6042	P3V8ILIM_RB:15K4
114S00179	1	RES,0402,1%,1/16W,715K	R6043	P3V8ILIM_RF:715K
114S00202	1	RES,0402,1%,1/16W,866K	R6043	P3V8ILIM_RF:866K

BOM_COST_GROUP=SOC POWER

PAGE TITLE: POWER: 3V8 AON OUTPUT THROTTLE

Apple Inc.

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Desense Caps for every rail

1 set for 1- and 2- phase BUCKs
2 set for 3- and 4- phase BUCKs

MPMU

144 43 41 PPVDD_SRAM_S1
0
C7600 12PF 25V NP0-C0G 5% 0201
C7601 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7602 1.8PF 25V C0G +/-0.1PF 201
C7603 12PF 25V NP0-C0G 5% 0201
C7604 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7605 1.8PF 25V C0G +/-0.1PF 201

144 43 41 PPVDD_GPU_BMPR_S1
1
C7620 12PF 25V NP0-C0G 5% 0201
C7621 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7622 1.8PF 25V C0G +/-0.1PF 201

144 43 41 PP1V8_S2SW
3
C7630 12PF 25V NP0-C0G 5% 0201
C7631 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7632 1.8PF 25V C0G +/-0.1PF 201

144 43 41 PPVDD2H1_S2SW
4
C7640 12PF 25V NP0-C0G 5% 0201
C7641 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7642 1.8PF 25V C0G +/-0.1PF 201
C7643 12PF 25V NP0-C0G 5% 0201
C7644 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7645 1.8PF 25V C0G +/-0.1PF 201

144 43 41 PPVDD_DISP_AWAKESW
5
C7650 12PF 25V NP0-C0G 5% 0201
C7651 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7652 1.8PF 25V C0G +/-0.1PF 201
C7653 12PF 25V NP0-C0G 5% 0201
C7654 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7655 1.8PF 25V C0G +/-0.1PF 201

144 43 41 PPVDD_AMPH1_S2SW
6
C7660 12PF 25V NP0-C0G 5% 0201
C7661 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7662 1.8PF 25V C0G +/-0.1PF 201

144 43 41 PPVDD_AVEMSR_AWAKESW
7
C7670 12PF 25V NP0-C0G 5% 0201
C7671 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7672 1.8PF 25V C0G +/-0.1PF 201
C7673 12PF 25V NP0-C0G 5% 0201
C7674 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7675 1.8PF 25V C0G +/-0.1PF 201

144 141 43 41 PP1V2_S2
8
C7680 12PF 25V NP0-C0G 5% 0201
C7681 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7682 1.8PF 25V C0G +/-0.1PF 201

144 43 41 PPVDD_FIXED_S1
9
C7690 12PF 25V NP0-C0G 5% 0201
C7691 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7692 1.8PF 25V C0G +/-0.1PF 201

144 43 41 PPVDDQ1_S1
10
C76A0 12PF 25V NP0-C0G 5% 0201
C76A1 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76A2 1.8PF 25V C0G +/-0.1PF 201
C76A3 12PF 25V NP0-C0G 5% 0201
C76A4 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76A5 1.8PF 25V C0G +/-0.1PF 201

144 42 PP1V2_S2_CLVR_VDDIO
SW0
C76M0 12PF 25V NP0-C0G 5% 0201
C76M1 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76M2 1.8PF 25V C0G +/-0.1PF 201

SPMU

145 41 39 PPVDD_DCS_S1
0
C76B0 12PF 25V NP0-C0G 5% 0201
C76B1 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76B2 1.8PF 25V C0G +/-0.1PF 201
C76B3 12PF 25V NP0-C0G 5% 0201
C76B4 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76B5 1.8PF 25V C0G +/-0.1PF 201

145 41 39 PPVDDQ0_S1
1
C76C0 12PF 25V NP0-C0G 5% 0201
C76C1 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76C2 1.8PF 25V C0G +/-0.1PF 201

145 41 39 PPVDD_ECPU_SRAM_AWAKESW
2
C76D0 12PF 25V NP0-C0G 5% 0201
C76D1 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76D2 1.8PF 25V C0G +/-0.1PF 201

145 141 41 39 PP1V8_S2
3
C76E0 12PF 25V NP0-C0G 5% 0201
C76E1 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76E2 1.8PF 25V C0G +/-0.1PF 201

145 41 39 PPVDD2H0_S2SW
4
C76F0 12PF 25V NP0-C0G 5% 0201
C76F1 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76F2 1.8PF 25V C0G +/-0.1PF 201
C76F3 12PF 25V NP0-C0G 5% 0201
C76F4 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76F5 1.8PF 25V C0G +/-0.1PF 201

145 41 39 PPVDD_SOC_S1
5
C76G0 12PF 25V NP0-C0G 5% 0201
C76G1 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76G2 1.8PF 25V C0G +/-0.1PF 201
C76G3 12PF 25V NP0-C0G 5% 0201
C76G4 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76G5 1.8PF 25V C0G +/-0.1PF 201

145 41 39 PPVDD_CIO_S2SW
6
C76H0 12PF 25V NP0-C0G 5% 0201
C76H1 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76H2 1.8PF 25V C0G +/-0.1PF 201

145 41 39 PPVDD_DISP2_AWAKESW
PACK_COMMENT=TBD
PACK_OPTION=PMU_DISP2:Y
7
C76I0 12PF 25V NP0-C0G 5% 0201
C76I1 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76I2 1.8PF 25V C0G +/-0.1PF 201
C76I3 12PF 25V NP0-C0G 5% 0201
C76I4 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76I5 1.8PF 25V C0G +/-0.1PF 201

145 141 41 39 PP1V2_AWAKE
8
C76J0 12PF 25V NP0-C0G 5% 0201
C76J1 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76J2 1.8PF 25V C0G +/-0.1PF 201

145 41 39 PPVDD_AMPH0_S2SW
9
C76K0 12PF 25V NP0-C0G 5% 0201
C76K1 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76K2 1.8PF 25V C0G +/-0.1PF 201

145 41 39 PPVDD_ECPU_AWAKESW
10
C76L0 12PF 25V NP0-C0G 5% 0201
C76L1 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76L2 1.8PF 25V C0G +/-0.1PF 201
C76L3 12PF 25V NP0-C0G 5% 0201
C76L4 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76L5 1.8PF 25V C0G +/-0.1PF 201

BOM_COST_GROUP=WIRELESS

PAGE TITLE
PMU OUTPUT DESENSE CAPS

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SPMU VIN/LDO/SW

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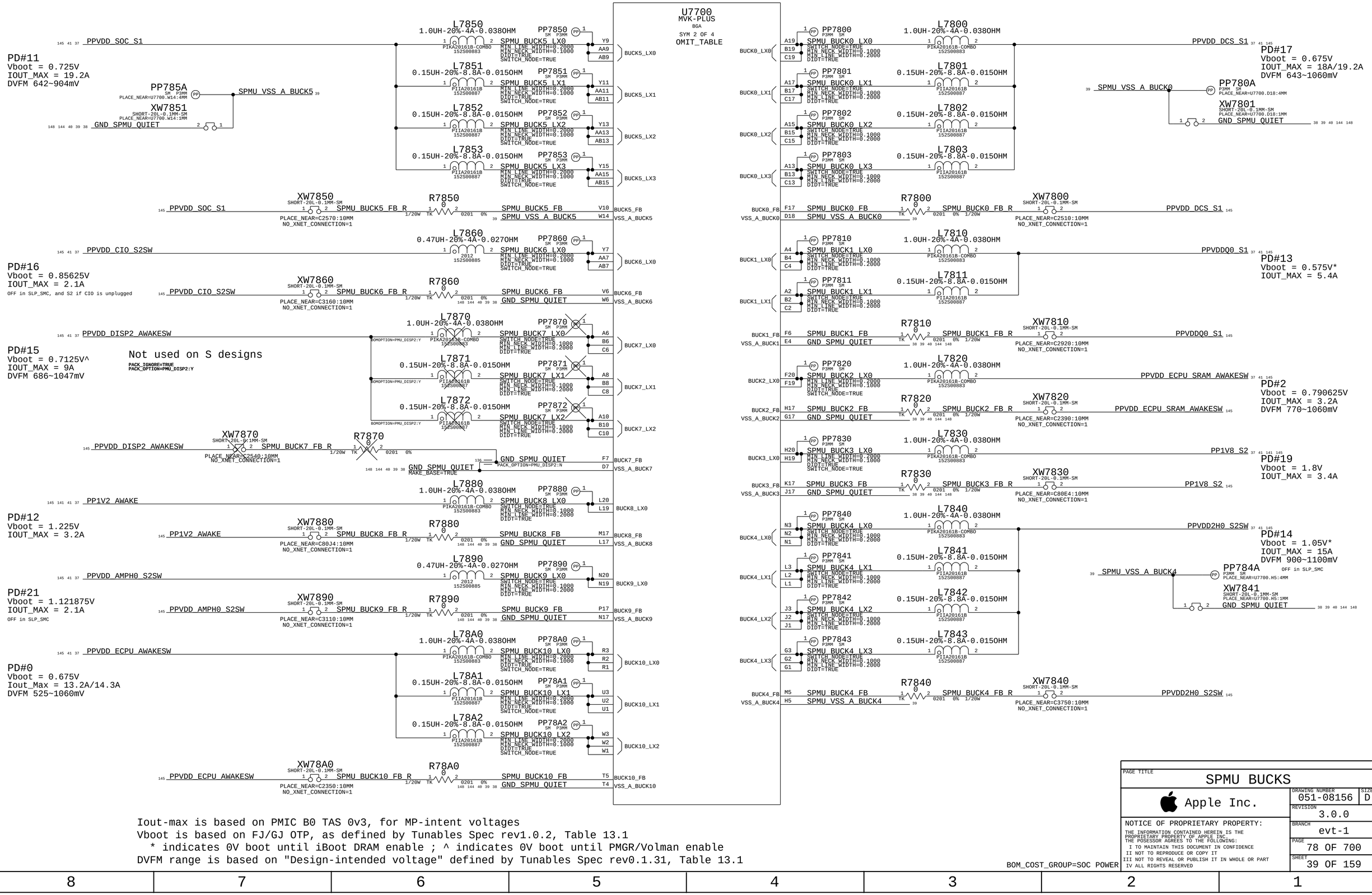

Iout-max is based on PMIC B0 TAS 0v3, for MP-intent voltages
Vboot is based on FJ/GJ OTP, as defined by Tunables Spec rev1.0.2, Table 13.1
  * indicates 0V boot until iBoot DRAM enable ; ^ indicates 0V boot until PMGR/Volman enable
DVFM range is based on "Design-intended voltage" defined by Tunables Spec rev0.1.31, Table 13.1

PAGE TITLE
SPMU BUCKS

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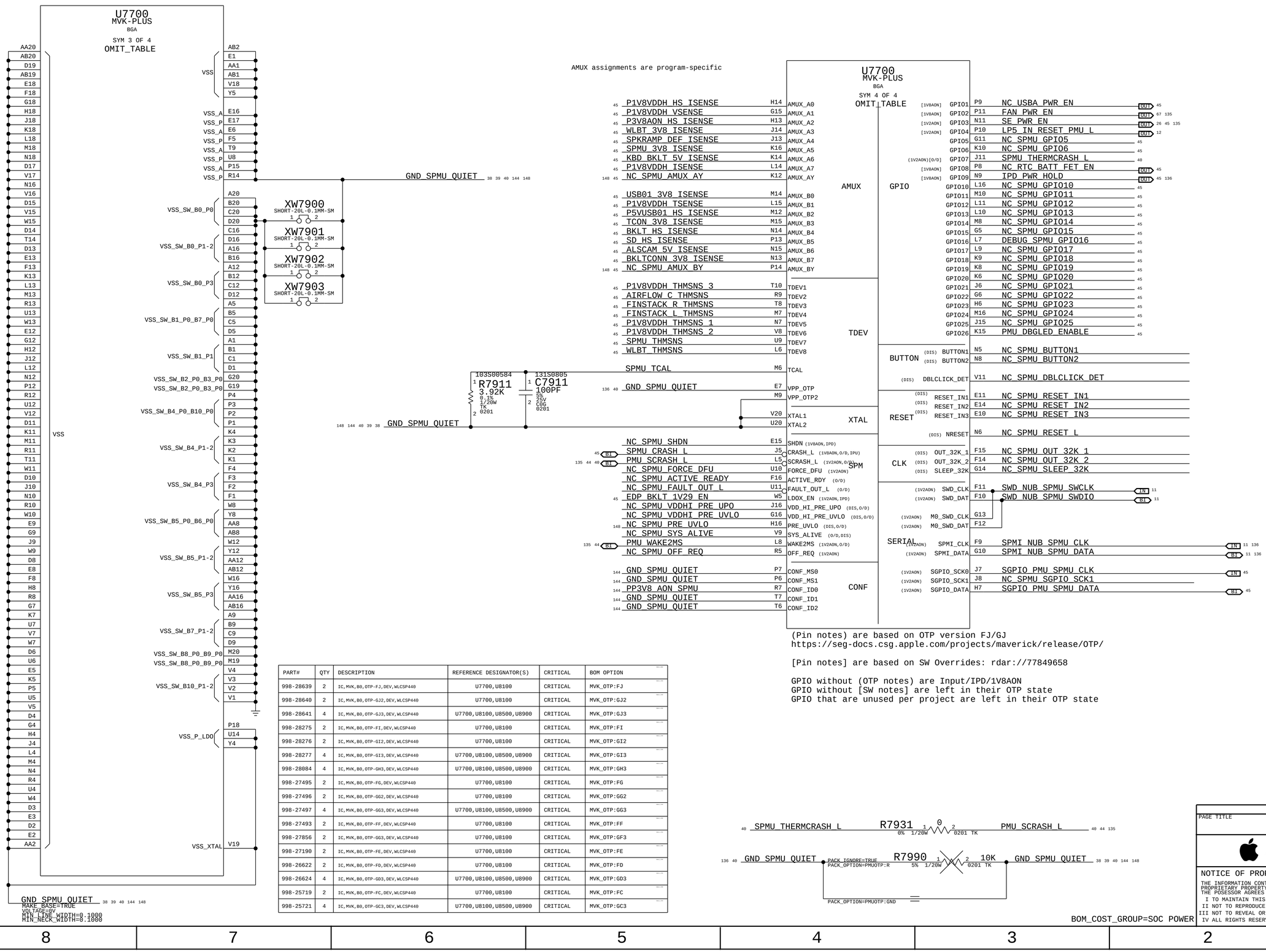

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-28639	2	IC,MVK,B0,OTP-FJ,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:FJ
998-28640	2	IC,MVK,B0,OTP-GJ2,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:GJ2
998-28641	4	IC,MVK,B0,OTP-GJ3,DEV,WLCSP440	U7700,U8100,U8500,U8900	CRITICAL	MVK_OTP:GJ3
998-28275	2	IC,MVK,B0,OTP-FI,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:FI
998-28276	2	IC,MVK,B0,OTP-GI2,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:GI2
998-28277	4	IC,MVK,B0,OTP-GI3,DEV,WLCSP440	U7700,U8100,U8500,U8900	CRITICAL	MVK_OTP:GI3
998-28084	4	IC,MVK,B0,OTP-GH3,DEV,WLCSP440	U7700,U8100,U8500,U8900	CRITICAL	MVK_OTP:GH3
998-27495	2	IC,MVK,B0,OTP-FG,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:FG
998-27496	2	IC,MVK,B0,OTP-GG2,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:GG2
998-27497	4	IC,MVK,B0,OTP-GG3,DEV,WLCSP440	U7700,U8100,U8500,U8900	CRITICAL	MVK_OTP:GG3
998-27493	2	IC,MVK,B0,OTP-FF,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:FF
998-27856	2	IC,MVK,B0,OTP-GG3,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:GF3
998-27190	2	IC,MVK,B0,OTP-FE,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:FE
998-26622	2	IC,MVK,B0,OTP-FD,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:FD
998-26624	4	IC,MVK,B0,OTP-GD3,DEV,WLCSP440	U7700,U8100,U8500,U8900	CRITICAL	MVK_OTP:GD3
998-25719	2	IC,MVK,B0,OTP-FC,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:FC
998-25721	4	IC,MVK,B0,OTP-GC3,DEV,WLCSP440	U7700,U8100,U8500,U8900	CRITICAL	MVK_OTP:GC3

PAGE TITLE
SPMU GPIO & GND

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144 43 37 **PPVDD_SRAM_S1**

C8003	C8002	C8001	C8000	0
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

144 43 37 **PPVDD_GPU_BMPR_S1**

C8013	C8012	C8011	C8010	1
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

<unused> 2

144 43 37 **PP1V8_S2SW**

C8033	C8032	C8031	C8030	3
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

144 43 37 **PPVDD2H1_S2SW**

C8043	C8042	C8041	C8040	4
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

144 43 37 **PPVDD_DISP_AWAKESW**

C8053	C8052	C8051	C8050	5
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

144 43 37 **PPVDD_AMPH1_S2SW**

C8063	C8062	C8061	C8060	6
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

144 43 37 **PPVDD_AVEMSR_AWAKESW**

C8073	C8072	C8071	C8070	7
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

144 141 43 37 **PP1V2_S2**

C8088	C8087	C8086	C8085	C8084	C8083	C8082	C8081	C8080	8
15UF 20% 2.5V X6S 0402-4	15UF 20% 2.5V X6S 0402-4	15UF 20% 2.5V X6S 0402-4	15UF 20% 2.5V X6S 0402-4	15UF 20% 2.5V X6S 0402-4	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	138S00041	138S00041	138S00041	138S00041	138S00041	

144 43 37 **PPVDD_FIXED_S1**

C8093	C8092	C8091	C8090	9
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

144 43 37 **PPVDDQ1_S1**

C80A3	C80A2	C80A1	C80A0	10
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

SPMU

145 39 37 **PPVDD_DCS_S1**

C80B3	C80B2	C80B1	C80B0	0
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

145 39 37 **PPVDDQ0_S1**

C80C3	C80C2	C80C1	C80C0	1
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

145 39 37 **PPVDD_ECPU_SRAM_AWAKESW**

C80D3	C80D2	C80D1	C80D0	2
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

145 141 39 37 **PP1V8_S2**

C80E9	C80E8	C80E7	C80E6	C80E5	C80E4	C80E3	C80E2	C80E1	C80E0	3
20UF 20% 2.5V X6S 0402-3	20UF 20% 2.5V X6S 0402-3	20UF 20% 2.5V X6S 0402-3	20UF 20% 2.5V X6S 0402-3	20UF 20% 2.5V X6S 0402-3	20UF 20% 2.5V X6S 0402-3	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00424 BOMSWAP=138S00035 NOSTUFF	138S00424 BOMSWAP=138S00035	138S00424 BOMSWAP=138S00035	138S00424 BOMSWAP=138S00035	138S00424 BOMSWAP=138S00035	138S00424 BOMSWAP=138S00035	138S00041	138S00041	138S00041	138S00041	

145 39 37 **PPVDD2H0_S2SW**

C80F3	C80F2	C80F1	C80F0	4
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

145 39 37 **PPVDD_SOC_S1**

C80G3	C80G2	C80G1	C80G0	5
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

145 39 37 **PPVDD_CIO_S2SW**

C80H3	C80H2	C80H1	C80H0	6
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

145 39 37 **PPVDD_DISP2_AWAKESW**

C80I3	C80I2	C80I1	C80I0	7
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041 BOMOPTION=PMU_DISP2:Y	138S00041 BOMOPTION=PMU_DISP2:Y	138S00041 BOMOPTION=PMU_DISP2:Y	138S00041 BOMOPTION=PMU_DISP2:Y	

PACK_IGNORE=TRUE
PACK_OPTION=PMU_DISP2:Y

145 141 39 37 **PP1V2_AWAKE**

C80J8	C80J7	C80J6	C80J5	C80J4	C80J3	C80J2	C80J1	C80J0	8
15UF 20% 2.5V X6S 0402-4	15UF 20% 2.5V X6S 0402-4	15UF 20% 2.5V X6S 0402-4	15UF 20% 2.5V X6S 0402-4	15UF 20% 2.5V X6S 0402-4	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00423 BOMSWAP=138S00392	138S00423 BOMSWAP=138S00392	138S00423 BOMSWAP=138S00392	138S00423 BOMSWAP=138S00392	138S00423 BOMSWAP=138S00392	138S00041	138S00041	138S00041	138S00041	

145 39 37 **PPVDD_AMPH0_S2SW**

C80K3	C80K2	C80K1	C80K0	9
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

145 39 37 **PPVDD_ECPU_AWAKESW**

C80L3	C80L2	C80L1	C80L0	10
2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	2.2UF 10% 10V X6S-CERM 0402	
138S00041	138S00041	138S00041	138S00041	

BOM_COST_GROUP=SOC POWER

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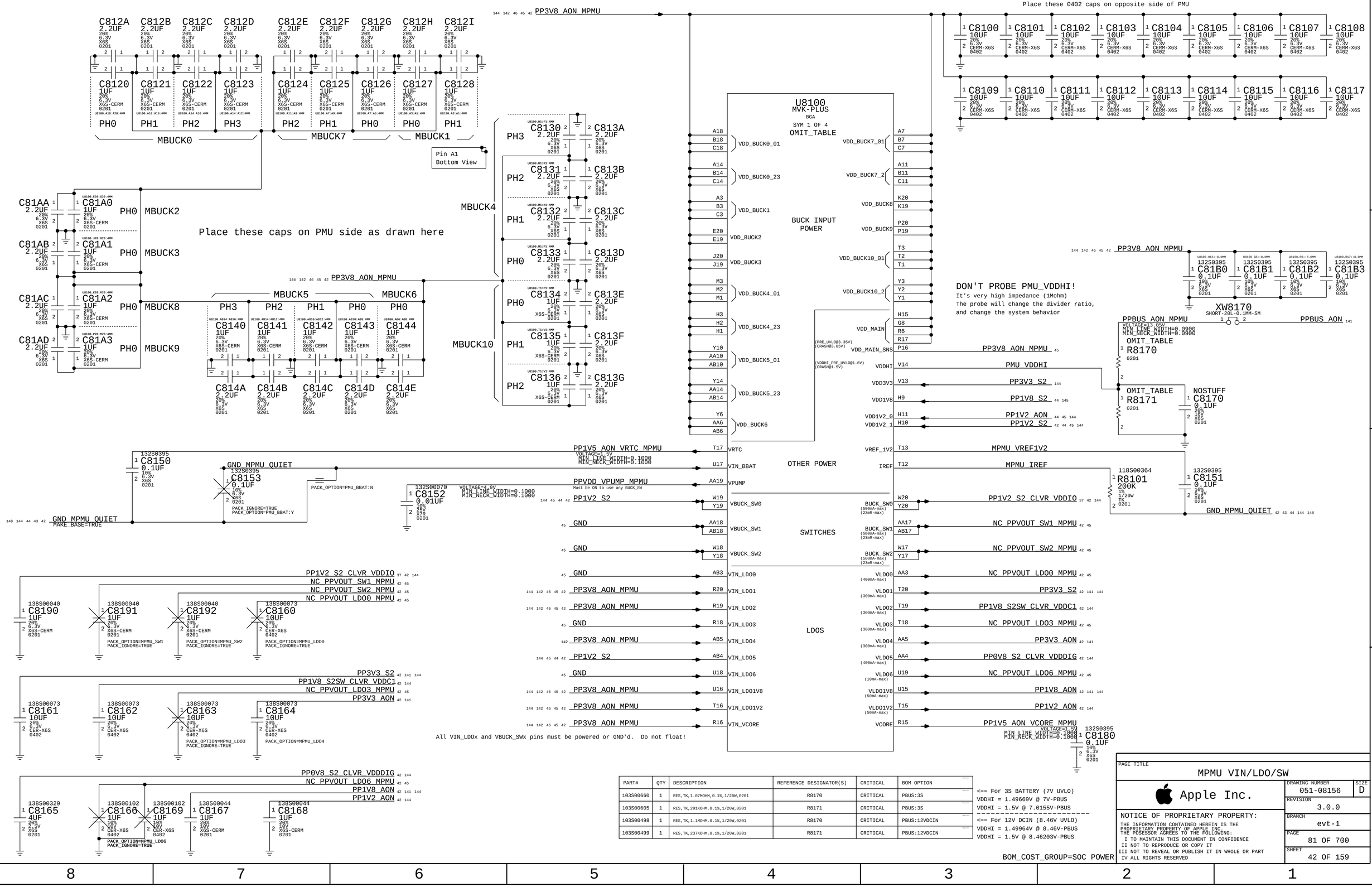

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
103S00660	1	RES,TK,1.07MOHM,0.1%,1/20W,0201	R8170	CRITICAL	PBUS:3S
103S00605	1	RES,TK,291KOHM,0.1%,1/20W,0201	R8171	CRITICAL	PBUS:3S
103S00498	1	RES,TK,1.1MOHM,0.1%,1/20W,0201	R8170	CRITICAL	PBUS:12VDCIN
103S00499	1	RES,TK,237KOHM,0.1%,1/20W,0201	R8171	CRITICAL	PBUS:12VDCIN

<=== For 3S BATTERY (7V UVLO)
VDDHI = 1.49669V @ 7V-PBUS
VDDHI = 1.5V @ 7.0155V-PBUS

<=== For 12V DCIN (8.46V UVLO)
VDDHI = 1.49964V @ 8.46V-PBUS
VDDHI = 1.5V @ 8.46203V-PBUS

BOM_COST_GROUP=SOC POWER

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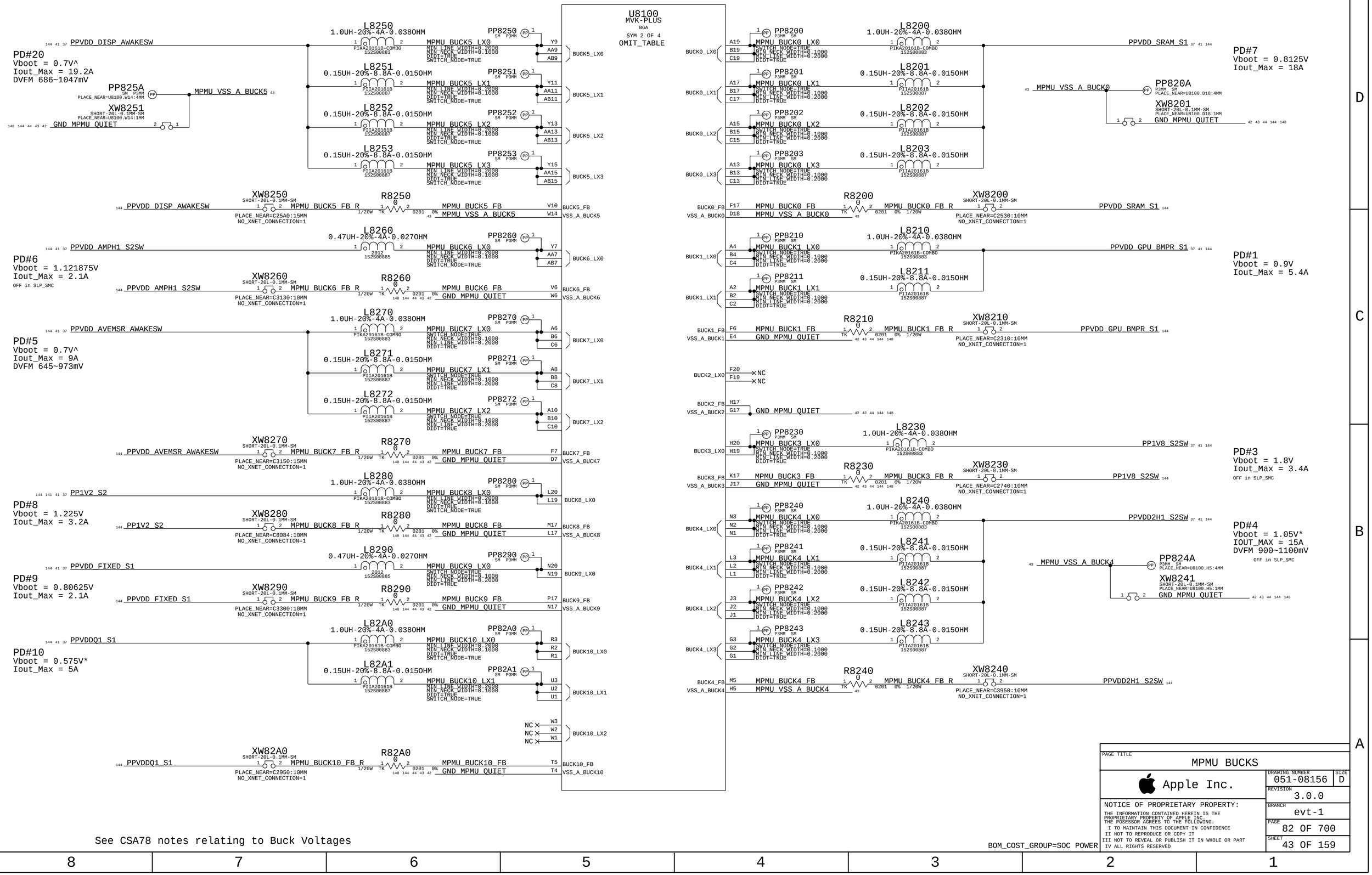
U8100
MVK-PLUS
BGA
SYM 2 OF 4
OMIT_TABLE
PD#20
Vboot = 0.7V^
Iout_Max = 19.2A
DVFM 686~1047mV
PP825A
MPMU_VSS_A_BUCK5
XW8251
SHORT-20L-0.1MM-SM
GND_MPMU_QUIET
L8250
1.0UH-20%-4A-0.038OHM
PP8250
MPMU_BUCK5_LX0
BUCK5_LX0
L8251
0.15UH-20%-8.8A-0.015OHM
PP8251
MPMU_BUCK5_LX1
BUCK5_LX1
L8252
0.15UH-20%-8.8A-0.015OHM
PP8252
MPMU_BUCK5_LX2
BUCK5_LX2
L8253
0.15UH-20%-8.8A-0.015OHM
PP8253
MPMU_BUCK5_LX3
BUCK5_LX3
XW8250
R8250
0
MPMU_BUCK5_FB_R
MPMU_BUCK5_FB
BUCK5_FB
MPMU_VSS_A_BUCK5
VSS_A_BUCK5
PLACE_NEAR=C25A0:15MM
NO_XNET_CONNECTION=1
PD#6
Vboot = 1.121875V
Iout_Max = 2.1A
OFF in SLP_SMC
L8260
0.47UH-20%-4A-0.027OHM
PP8260
MPMU_BUCK6_LX0
BUCK6_LX0
XW8260
R8260
0
MPMU_BUCK6_FB_R
MPMU_BUCK6_FB
GND_MPMU_QUIET
BUCK6_FB
VSS_A_BUCK6
PLACE_NEAR=C3130:10MM
NO_XNET_CONNECTION=1
PD#5
Vboot = 0.7V^
Iout_Max = 9A
DVFM 645~973mV
L8270
1.0UH-20%-4A-0.038OHM
PP8270
MPMU_BUCK7_LX0
BUCK7_LX0
L8271
0.15UH-20%-8.8A-0.015OHM
PP8271
MPMU_BUCK7_LX1
BUCK7_LX1
L8272
0.15UH-20%-8.8A-0.015OHM
PP8272
MPMU_BUCK7_LX2
BUCK7_LX2
XW8270
R8270
0
MPMU_BUCK7_FB_R
MPMU_BUCK7_FB
GND_MPMU_QUIET
BUCK7_FB
VSS_A_BUCK7
PLACE_NEAR=C3150:15MM
NO_XNET_CONNECTION=1
PD#8
Vboot = 1.225V
Iout_Max = 3.2A
L8280
1.0UH-20%-4A-0.038OHM
PP8280
MPMU_BUCK8_LX0
BUCK8_LX0
XW8280
R8280
0
MPMU_BUCK8_FB_R
MPMU_BUCK8_FB
GND_MPMU_QUIET
BUCK8_FB
VSS_A_BUCK8
PLACE_NEAR=C8084:10MM
NO_XNET_CONNECTION=1
PD#9
Vboot = 0.80625V
Iout_Max = 2.1A
L8290
0.47UH-20%-4A-0.027OHM
PP8290
MPMU_BUCK9_LX0
BUCK9_LX0
XW8290
R8290
0
MPMU_BUCK9_FB_R
MPMU_BUCK9_FB
GND_MPMU_QUIET
BUCK9_FB
VSS_A_BUCK9
PLACE_NEAR=C3300:10MM
NO_XNET_CONNECTION=1
PD#10
Vboot = 0.575V*
Iout_Max = 5A
L82A0
1.0UH-20%-4A-0.038OHM
PP82A0
MPMU_BUCK10_LX0
BUCK10_LX0
L82A1
0.15UH-20%-8.8A-0.015OHM
PP82A1
MPMU_BUCK10_LX1
BUCK10_LX1
NC
NC
NC
BUCK10_LX2
XW82A0
R82A0
0
MPMU_BUCK10_FB_R
MPMU_BUCK10_FB
GND_MPMU_QUIET
BUCK10_FB
VSS_A_BUCK10
PLACE_NEAR=C2950:10MM
NO_XNET_CONNECTION=1
BUCK0_LX0
BUCK0_LX1
BUCK0_LX2
BUCK0_LX3
L8200
1.0UH-20%-4A-0.038OHM
PP8200
MPMU_BUCK0_LX0
L8201
0.15UH-20%-8.8A-0.015OHM
PP8201
MPMU_BUCK0_LX1
L8202
0.15UH-20%-8.8A-0.015OHM
PP8202
MPMU_BUCK0_LX2
L8203
0.15UH-20%-8.8A-0.015OHM
PP8203
MPMU_BUCK0_LX3
BUCK0_FB
VSS_A_BUCK0
R8200
0
MPMU_BUCK0_FB
MPMU_BUCK0_FB_R
XW8200
PLACE_NEAR=C2530:10MM
NO_XNET_CONNECTION=1
PPVDD_SRAM_S1
PD#7
Vboot = 0.8125V
Iout_Max = 18A
MPMU_VSS_A_BUCK0
PP820A
XW8201
SHORT-20L-0.1MM-SM
GND_MPMU_QUIET
BUCK1_LX0
BUCK1_LX1
L8210
1.0UH-20%-4A-0.038OHM
PP8210
MPMU_BUCK1_LX0
L8211
0.15UH-20%-8.8A-0.015OHM
PP8211
MPMU_BUCK1_LX1
BUCK1_FB
VSS_A_BUCK1
R8210
0
MPMU_BUCK1_FB
GND_MPMU_QUIET
MPMU_BUCK1_FB_R
XW8210
PLACE_NEAR=C2310:10MM
NO_XNET_CONNECTION=1
PPVDD_GPU_BMPR_S1
PD#1
Vboot = 0.9V
Iout_Max = 5.4A
BUCK2_LX0
NC
NC
BUCK2_FB
VSS_A_BUCK2
GND_MPMU_QUIET
BUCK3_LX0
BUCK3_FB
VSS_A_BUCK3
L8230
1.0UH-20%-4A-0.038OHM
PP8230
MPMU_BUCK3_LX0
R8230
0
MPMU_BUCK3_FB
GND_MPMU_QUIET
MPMU_BUCK3_FB_R
XW8230
PLACE_NEAR=C2740:10MM
NO_XNET_CONNECTION=1
PP1V8_S2SW
PD#3
Vboot = 1.8V
Iout_Max = 3.4A
OFF in SLP_SMC
BUCK4_LX0
BUCK4_LX1
BUCK4_LX2
BUCK4_LX3
L8240
1.0UH-20%-4A-0.038OHM
PP8240
MPMU_BUCK4_LX0
L8241
0.15UH-20%-8.8A-0.015OHM
PP8241
MPMU_BUCK4_LX1
L8242
0.15UH-20%-8.8A-0.015OHM
PP8242
MPMU_BUCK4_LX2
L8243
0.15UH-20%-8.8A-0.015OHM
PP8243
MPMU_BUCK4_LX3
BUCK4_FB
VSS_A_BUCK4
R8240
0
MPMU_BUCK4_FB
MPMU_VSS_A_BUCK4
MPMU_BUCK4_FB_R
XW8240
PLACE_NEAR=C3950:10MM
NO_XNET_CONNECTION=1
PPVDD2H1_S2SW
PD#4
Vboot = 1.05V*
IOUT_MAX = 15A
DVFM 900~1100mV
OFF in SLP_SMC
MPMU_VSS_A_BUCK4
PP824A
XW8241
SHORT-20L-0.1MM-SM
GND_MPMU_QUIET
See CSA78 notes relating to Buck Voltages
BOM_COST_GROUP=SOC POWER
PAGE TITLE
MPMU BUCKS
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AMUX assignments are program-specific
Sensor DRI must coordinate with CPMS spec to connect fast-sampling signals to the correct MPMU AMUX

U8100
MVK-PLUS
BGA
SYM 3 OF 4
OMIT_TABLE

AA20 AB20 D19 AB19 E18 F18 G18 H18 J18 K18 L18 M18 N18 D17 V17 N16 V16 D15 V15 W15 D14 T14 D13 E13 F13 K13 L13 M13 R13 U13 W13 E12 G12 H12 J12 L12 N12 P12 R12 U12 V12 D11 K11 M11 R11 T11 W11 D10 J10 N10 R10 W10 E9 G9 J9 W9 D8 E8 F8 H8 R8 G7 K7 U7 V7 W7 D6 U6 E5 K5 P5 U5 V5 D4 G4 H4 J4 L4 M4 N4 R4 U4 W4 D3 E3 D2 E2 AA2

VSS

AB2 E1 AA1 AB1 V18 Y5 E16 E17 E6 F5 T9 U8 P15 R14 A20 B20 C20 D20 C16 D16 A16 B16 A12 B12 C12 D12 A5 B5 C5 D5 A1 B1 C1 D1 G20 G19 P4 P3 P2 P1 K4 K3 K2 K1 F4 F3 F2 F1 W8 Y8 AA8 AB8 W12 Y12 AA12 AB12 W16 Y16 AA16 AB16 A9 B9 C9 D9 M20 M19 V4 V3 V2 V1 P18 U14 Y4 V19

VSS_A VSS_P VSS_A VSS_P VSS_A VSS_P VSS_A VSS_P
VSS_SW_B0_P0
VSS_SW_B0_P1-2
VSS_SW_B0_P3
VSS_SW_B1_P0_B7_P0
VSS_SW_B1_P1
VSS_SW_B2_P0_B3_P0
VSS_SW_B2_P0_B3_P0
VSS_SW_B4_P0_B10_P0
VSS_SW_B4_P1-2
VSS_SW_B4_P3
VSS_SW_B5_P0_B6_P0
VSS_SW_B5_P1-2
VSS_SW_B5_P3
VSS_SW_B7_P1-2
VSS_SW_B8_P0_B9_P0
VSS_SW_B8_P0_B9_P0
VSS_SW_B10_P1-2
VSS_P_LDO
VSS_XTAL

GND_MPMU_QUIET 42 43 44 144 148

XW8300 SHORT-20L-0.1MM-SM
XW8301 SHORT-20L-0.1MM-SM
XW8302 SHORT-20L-0.1MM-SM
XW8303 SHORT-20L-0.1MM-SM

148 144 44 43 42 GND_MPMU_QUIET
103S00584 R8311 3.92K 0.1% 1/20W TK 0201
131S0805 C8311 100PF 5% 25V C0G 0201

U8100
MVK-PLUS
BGA
SYM 4 OF 4
OMIT_TABLE

AMUX
45 DCIN_ISENSE H14 AMUX_A0
45 DCIN_VSENSE G15 AMUX_A1
45 BMON_ISENSE H13 AMUX_A2
45 PBUS_VSENSE J14 AMUX_A3
45 P5VUSB23_HS_ISENSE J13 AMUX_A4
45 P5VS2_HS_ISENSE K16 AMUX_A5
45 SPKRAMP_ABC_ISENSE K14 AMUX_A6
45 HDMI0V95_HS_ISENSE L14 AMUX_A7
148 45 NC_MPMU_AMUX_AY K12 AMUX_AY
45 IPD_3V8_ISENSE M14 AMUX_B0
45 MPMU_3V8_ISENSE L15 AMUX_B1
45 VCCNAND0_HS_ISENSE M12 AMUX_B2
45 VCCNAND1_HS_ISENSE M15 AMUX_B3
45 P3V8AON_ISENSE N14 AMUX_B4
45 USB23_3V8_ISENSE P13 AMUX_B5
45 SSD0_3V8_ISENSE N15 AMUX_B6
45 SSD1_3V8_ISENSE N13 AMUX_B7
148 45 NC_MPMU_AMUX_BY P14 AMUX_BY

TDEV
45 P3V8AON_THMSNS T10 TDEV1
45 MPMU_THMSNS R9 TDEV2
45 AIRFLOW_L_THMSNS T8 TDEV3
45 AIRFLOW_R_THMSNS M7 TDEV4
45 WING_R_THMSNS N7 TDEV5
45 CHGR_THMSNS V8 TDEV6
45 SOC_THMSNS_1 U9 TDEV7
45 WING_L_THMSNS L6 TDEV8

XTAL
MPMU_TCAL M6 TCAL
136 44 GND_MPMU_QUIET E7 VPP_OTP
148 144 44 43 42 GND_MPMU_QUIET M9 VPP_OTP2
44 MPMU_XTAL1 V20 XTAL1
44 MPMU_XTAL2 U20 XTAL2

SPM
Debug Only
138 135 45 IN PMU_SHDN E15 SHDN (1V8AON,IPD)
136 45 44 BI PMU_CRASH_L J5 CRASH_L (1V2AON,O/D)
135 44 46 BI PMU_SCRASH_L L5 SCRASH_L (1V2AON,O/D)
44 PMU_FORCE_DFU U10 FORCE_DFU (1V2AON)
137 135 134 73 44 10 5 OUT PMU_ACTIVE_READY F16 ACTIVE_RDY (O/D)
NC_PMU_FAULT_OUT_L U11 FAULT_OUT_L (O/D)
148 45 NC_MPMU_LDOX_EN W5 LDOX_EN (1V2AON,IPD)
148 NC_MPMU_VDDHI_PRE_UPO J16 VDD_HI_PRE_UPO (DIS,O/D)
136 11 OUT PMU_VDDHI_UVWARN_L G16 VDD_HI_PRE_UVLO (O/D)
136 11 OUT PMU_VDDMAIN_UVWARN_L H16 PRE_UVLO (O/D)
135 117 112 107 93 89 87 44 OUT PMU_SYS_ALIVE V9 SYS_ALIVE (O/D)
135 44 40 BI PMU_WAKE2MS L8 WAKE2MS (1V2AON,O/D)
45 OUT NC_PMU_SHDN_REQ R5 OFF_REQ (1V2AON)
TO M2 SHDN (2C only)

CONF
144 PP3V8_AON_MPMU P7 CONF_MS0 (3V8AON)
144 PP3V8_AON_MPMU P6 CONF_MS1 (3V8AON)
144 GND_MPMU_QUIET R7 CONF_ID0 (3V8AON)
144 GND_MPMU_QUIET T7 CONF_ID1 (3V8AON)
144 GND_MPMU_QUIET T6 CONF_ID2 (3V8AON)

GPIO
(1V8AON) GPIO1 P9 IPD_LID_OPEN_1V8 IN 45
[xAON,IPU] GPIO2 P11 SDCONN_STATE_CHANGE IN 45
[1V2S2,IPU] GPIO3 N11 CODEC_WAKE_L IN 122 134
[1V2S2,IPD] GPIO4 P10 WLBT_WAKE IN 101 102
(1V8AON,IPU) GPIO5 G11 IPD_WAKE_L IN 45
(1V8S2,IPD)[1V8y] GPIO6 K10 DP2HDMI_PWR_EN_PMU BI 45
(1V2AON)[O/D] GPIO7 J11 MPMU_THERMCRASH_L 44
[1V8AON,O/D] GPIO8 P8 DP2HDMI_RESET_L OUT 93 136
(1V8AON) GPIO9 N9 P3V8AON_LPM OUT 45
note-> GPIO10 L16 CHGR_AUX_OK BI 45
(1V2AON) GPIO11 M10 P1V8VDDH_PWR_EN OUT 45 48 136
(1V2AON) GPIO12 L11 P1V8VDDH_SLP_L OUT 48 136 137
[1V8AON] GPIO13 L10 WLBT_PWR_EN OUT 45 101 102 136
[1V8AON] GPIO14 M8 IPD_PWR_EN_PMU OUT 45
[1V2S2] GPIO15 G5 BL_PMIC_PWR_EN BI 45
[1V8AON] GPIO16 L7 HDMI_CECFET_EN OUT 90 136
(1V8AON) GPIO17 L9 P5VS2_PWR_EN OUT 29 45 135
(1V2AON) GPIO18 K9 CLVR_RESET_L OUT 51 52 53 136
[z] GPIO19 K8 BL_PWR_EN OUT 45
[1V8AON] GPIO20 K6 LCD_PWR_EN OUT 45
(1V8AON)[1V2AON,O/D] GPIO21 J6 PVBAT_ILIMIT_L OUT 5 45
[q] GPIO22 G6 SD_PWR_EN BI 45
[1V8AON] GPIO23 H6 HDMI_PWR_EN OUT 90 136
(1V8AON) GPIO24 M16 PVDD1_PWR_EN OUT 17
(3V8AON,O/D)[s] GPIO25 J15 IPD_TOUCH_RESET_L OUT 45
(r) GPIO26 K15 IPD_MCU_RESET_L OUT 45

BUTTON
(1V8AON,L) BUTTON1 N5 PMU_ONOFF_L IN 44 45 132 135 138
(1V8AON,L) BUTTON2 N8 PMU_RSLOC_RST_L IN 44 45 128 135 138

(1V2S2) DBLCLICK_DET V11 DBL_CLICK_DET OUT 6 136

RESET
(1V2S2,L) RESET_IN1 E11 SOC_WDOG_L IN 10
(1V2S2,H,IPD) RESET_IN2 E14 UPC_PMU_RESET_1V2 IN 45 136
(1V2S2,L) RESET_IN3 E10 SOC_SOCHOT_L IN 5 135
(O/D) NRESET N6 PMU_RESET_L OUT 10 12 44 134 135

CLK
(1V2AON) OUT_32K_1 F15 PMU_CLK32K_CLVR_R OUT 45
(1V2S2) OUT_32K_2 F14 PMU_CLK32K_WLBT_IPD_R OUT 45
(1V2AON) SLEEP_32K G14 PMU_CLK32K_SOC_R OUT 45

(1V2AON) SWD_CLK F11 SWD_NUB_MPMU_SWCLK IN 11
(1V2AON) SWD_DAT F10 SWD_NUB_MPMU_SWDIO BI 11
(1V2AON) M0_SWD_CLK G13
(1V2AON) M0_SWD_DAT F12

SERIAL
(1V2AON) SPMI_CLK F9 SPMI_NUB_MPMU_CLK IN 11 136
(1V2AON) SPMI_DATA G10 SPMI_NUB_MPMU_DATA BI 11 136

(1V2AON) SGPIO_SCK0 J7 SGPIO_PMU_SPMU_CLK_R OUT 45
(1V2AON) SGPIO_SCK1 J8 SGPIO_PMU_CLVR_CLK_R OUT 45
(1V2AON) SGPIO_DATA H7 SGPIO_PMU_DATA_R BI 45

GPIO2: x = 1V8 for portable, 1V2 for desktop
GPIO6: y = S2 for portable, AON for desktop
GPIO10: (1V8AON,IPU) for portable, [1V8AON] for desktop
GPIO19: z = 1V2S2 for portable, 1V8AON for desktop
GPIO22: q = 1V8AON for portable, 1V2AON,IPU for desktop
GPIO25: s = <no override> for portable, [3V3S2] for desktop
GPIO26: r = 3V8AON,O/D for portable, 1V8AON for desktop

PP1V8_S2 145 42
PP1V8_AON 144 45 44
PP1V2_S2 144 45 42
PP1V2_AWAKE 145
PP1V2_AON 144 45 42

136 45 44 PMU_CRASH_L R8312 1K 5% 1/20W 0201-1 TK
135 44 40 PMU_SCRASH_L R8313 10K 5% 1/20W 0201 TK
135 44 40 PMU_WAKE2MS R8314 10K 5% 1/20W 0201 TK
134 73 44 10 5 137 135 PMU_ACTIVE_READY R8320 10K 5% 1/20W 0201 TK
134 44 12 10 135 PMU_RESET_L R8321 10K 5% 1/20W 0201 TK
135 132 45 44 138 PMU_ONOFF_L R8317 1K 5% 1/20W 0201-1 TK
135 128 45 44 138 PMU_RSLOC_RST_L R8318 10K 5% 1/20W 0201 TK
107 93 89 87 44 135 117 112 PMU_SYS_ALIVE R8319 10K 5% 1/20W 0201 TK

44 MPMU_THERMCRASH_L R8331 0 0% 1/20W 0201 TK PMU_SCRASH_L 40 44 135
44 PMU_FORCE_DFU R8330 2.2K 5% 1/20W 0201 TK SOC_FORCE_DFU OUT 5 74 134 135 138
136 44 GND_MPMU_QUIET R8390 10K 5% 1/20W 0201 TK GND_MPMU_QUIET 42 43 44 144 148
PACK_IGNORE=TRUE
PACK_OPTION=PMUOTP:R
PACK_OPTION=PMUOTP:GND

197S00323 32.768KHZ-20PPM-1.8V 2.5X2.0-SM
U8355 CRITICAL
4 VCC
3 OUT
EN/DIS 1
GND 2
PACK_OPTION=PMU32K:OSC_QRTZ
BOMOPTION=PMU32K:OSC_QRTZ
148 144 44 43 42 GND_MPMU_QUIET
PMUOSC_PIN1

132S0395 C8355 0.1UF 10% 6.3V X6S 0201
PACK_OPTION=PMU32K:OSC_QRTZ
BOMOPTION=PMU32K:OSC_QRTZ
PP1V8_AON 44 45 144
R8355 1K 5% 1/20W TK 0201-1
PACK_OPTION=PMU32K:OSC_QRTZ
BOMOPTION=PMU32K:OSC_QRTZ

MPMU_XTAL_R
R8351 0 1/20W 0% TK 0201 MPMU_XTAL2 44
Inverter Output<-> (RTC bypass)
R8350 0 1/20W 0% TK 0201 NOSTUFF NO_XNET_CONNECTION=1 MPMU_XTAL1 44
Inverter Input->
R8352 0 0% 1/20W TK 0201 GND_MPMU_QUIET 42 43 44 144 148

BOM_COST_GROUP=SOC POWER

(Pin notes) are based on OTP version noted in CSA79
https://seg-docs.csg.apple.com/projects/maverick/release/OTP/

[Pin notes] are based on SW Overrides: rdar://77849658

GPIO without (OTP notes) are Input/IPD/1V8AON
GPIO without [SW notes] are left in their OTP state
GPIO that are unused per project are left in their OTP state

GND_MPMU_QUIET 42 43 44 144 148
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000

PAGE TITLE
MPMU GPIO & GND

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SIZE D
REVISION 3.0.0
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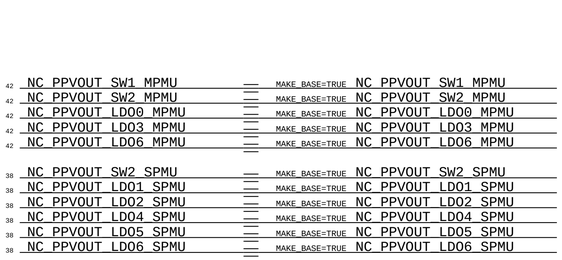

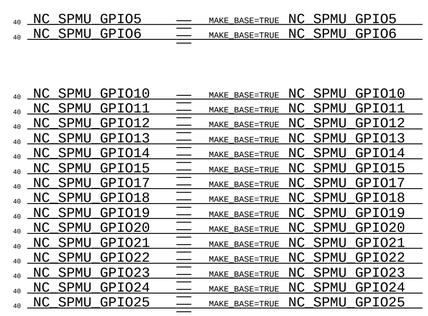

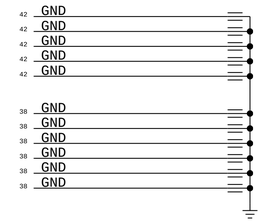

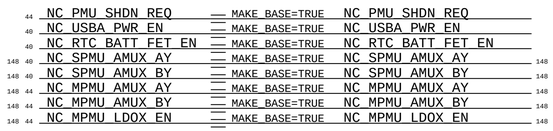

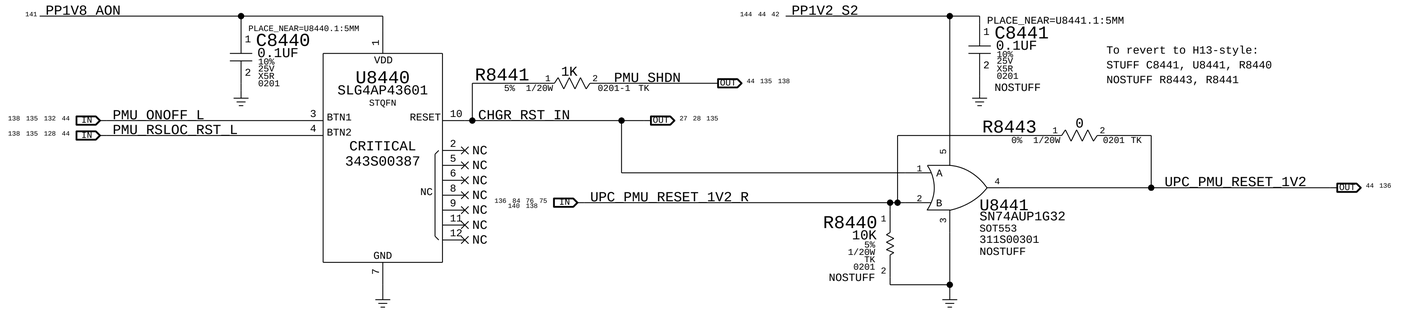

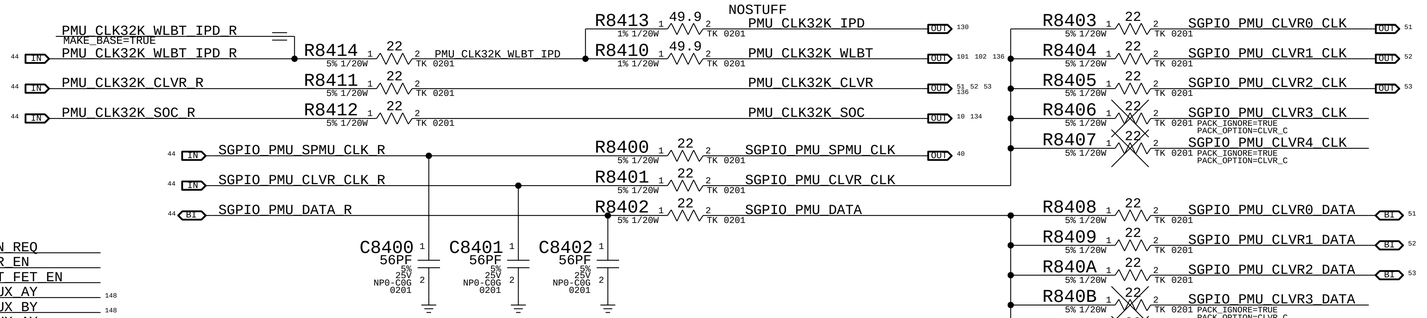

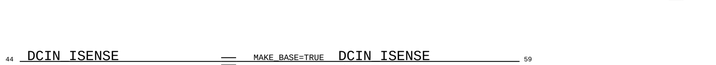

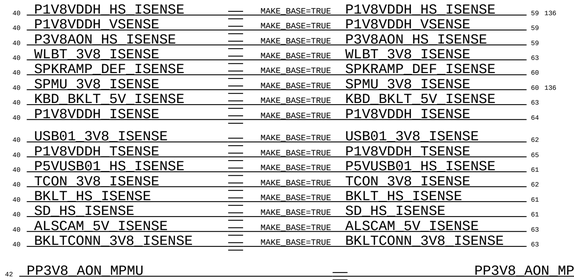

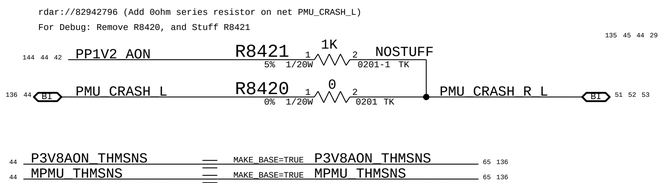

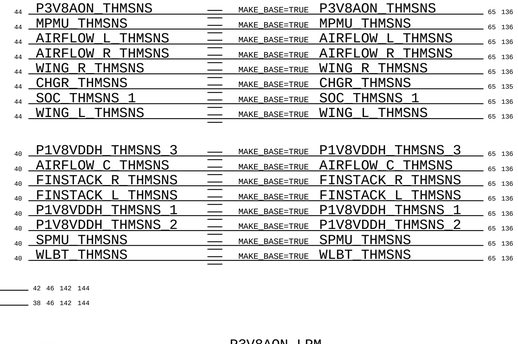

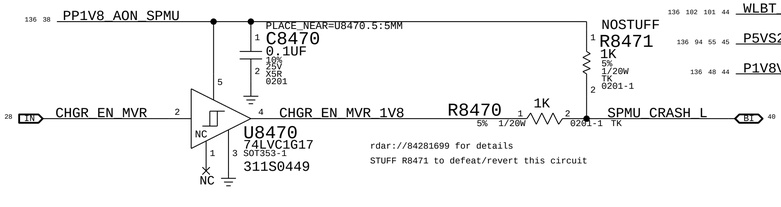

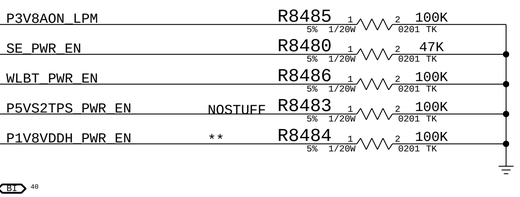

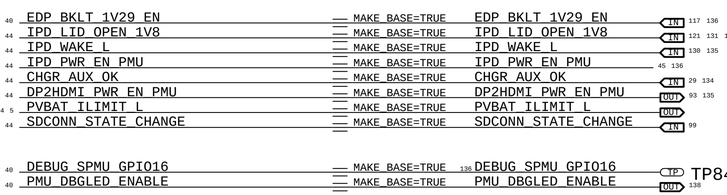

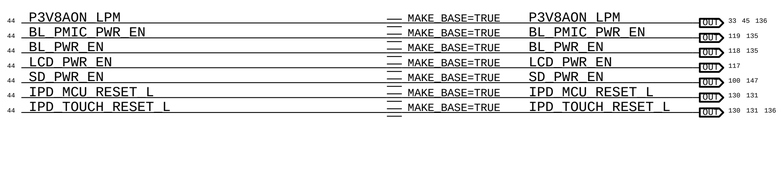

BOM_COST_GROUP=SOC POWER

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Input desense caps are shared across portables, until further notice

MPMU

144 142 45 42 PP3V8_AON_MPMU

C8500 12PF 5% 25V NP0-C0G 0201	C8501 1.8PF +/-0.1PF 100V C0G 0201	C8502 12PF 5% 25V NP0-C0G 0201	C8503 3.0PF +/-0.1PF 25V NP0-C0G 0201	C8504 12PF 5% 25V NP0-C0G 0201	C8505 3.0PF +/-0.1PF 25V NP0-C0G 0201	C8506 12PF 5% 25V NP0-C0G 0201	C8507 1.8PF +/-0.1PF 100V C0G 0201	C8508 1.8PF +/-0.1PF 100V C0G 0201
C8509 12PF 5% 25V NP0-C0G 0201	C850A 3.0PF +/-0.1PF 25V NP0-C0G 0201	C850B 1.8PF +/-0.1PF 100V C0G 0201	C850C 12PF 5% 25V NP0-C0G 0201	C850D 3.0PF +/-0.1PF 25V NP0-C0G 0201	C850E 3.0PF +/-0.1PF 25V NP0-C0G 0201	C850F 12PF 5% 25V NP0-C0G 0201	C850G 3.0PF +/-0.1PF 25V NP0-C0G 0201	C850H 12PF 5% 25V NP0-C0G 0201
C850I 12PF 5% 25V NP0-C0G 0201								

143 53 52 51 PP1V8_S1_CLVR_VDDH

C9296A 100V C0G	1.8PF +/-0.1PF 0201		
C9296 25V NP0-C0G	3.0PF +/-0.1PF 0201		
C9297 25V NP0-C0G	12PF 5% 0201		
C9299A 100V C0G	1.8PF +/-0.1PF 0201		
C9298 25V NP0-C0G	3.0PF +/-0.1PF 0201		
C9299 25V NP0-C0G	12PF 5% 0201		

142 59 47 PPVIN_P1V8VDDH

C928C 100V C0G	1.8PF +/-0.1PF 0201		
C928B 25V NP0-C0G	12PF 5% 0201		
C92A2Y 100V C0G	1.8PF +/-0.1PF 0201		
C92A0 25V NP0-C0G	3.0PF +/-0.1PF 0201		

ADDITIONAL VIPER DESENSE CAPS REQUIRED FOR T728 IN ADDITION TO DESENSE CAPS IN REF DESIGN

143 139 50 49 47 PP1V8_S1_CLVR_VDDH

C9290 12PF 5% 25V NP0-C0G 0201	C9291 3.0PF +/-0.1PF 25V NP0-C0G 0201	C9291A 1.8PF +/-0.1PF 100V C0G 0201	C9292 12PF 5% 25V NP0-C0G 0201	C9293 3.0PF +/-0.1PF 25V NP0-C0G 0201	C9292A 1.8PF +/-0.1PF 100V C0G 0201	C9294 12PF 5% 25V NP0-C0G 0201	C9295 3.0PF +/-0.1PF 25V NP0-C0G 0201	C9295A 1.8PF +/-0.1PF 100V C0G 0201

SPMU

144 142 45 38 PP3V8_AON_SPMU

C8550 3.0PF +/-0.1PF 25V NP0-C0G 0201	C8551 12PF 5% 25V NP0-C0G 0201	C8552 3.0PF +/-0.1PF 25V NP0-C0G 0201	C8553 3.0PF +/-0.1PF 25V NP0-C0G 0201	C8554 12PF 5% 25V NP0-C0G 0201	C8555 1.8PF +/-0.1PF 100V C0G 0201	C8556 12PF 5% 25V NP0-C0G 0201	C8557 12PF 5% 25V NP0-C0G 0201	C8558 12PF 5% 25V NP0-C0G 0201
C8559 3.0PF +/-0.1PF 25V NP0-C0G 0201	C855A 3.0PF +/-0.1PF 25V NP0-C0G 0201	C855B 12PF 5% 25V NP0-C0G 0201	C855C 1.8PF +/-0.1PF 100V C0G 0201	C855D 3.0PF +/-0.1PF 25V NP0-C0G 0201	C855E 1.8PF +/-0.1PF 100V C0G 0201	C855F 12PF 5% 25V NP0-C0G 0201	C855G 3.0PF +/-0.1PF 25V NP0-C0G 0201	C855H 12PF 5% 25V NP0-C0G 0201
C855I 1.8PF +/-0.1PF 100V C0G 0201	C855J 12PF 5% 25V NP0-C0G 0201	C855K 12PF 5% 25V NP0-C0G 0201	C855L 3.0PF +/-0.1PF 25V NP0-C0G 0201	C855M 3.0PF +/-0.1PF 25V NP0-C0G 0201	C855N 12PF 5% 25V NP0-C0G 0201	C8550 12PF 5% 25V NP0-C0G 0201	C855P 1.8PF +/-0.1PF 100V C0G 0201	

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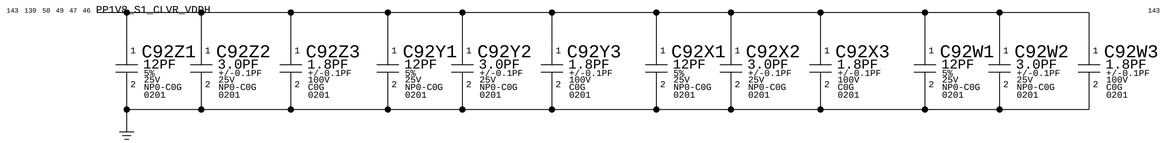
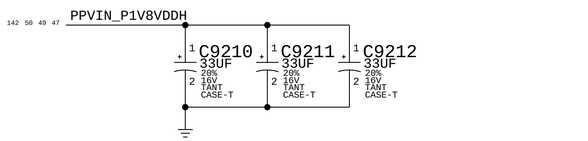
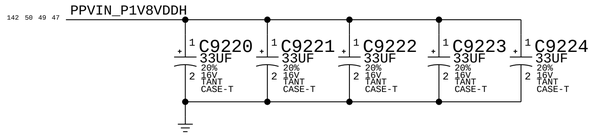
<rdar://problem/65184113> Add 4x Pairs of desense caps to Austringer support page



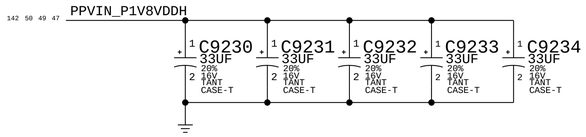
<rdar://problem/61127187> Add PBUS caps on Austringer input



PH1

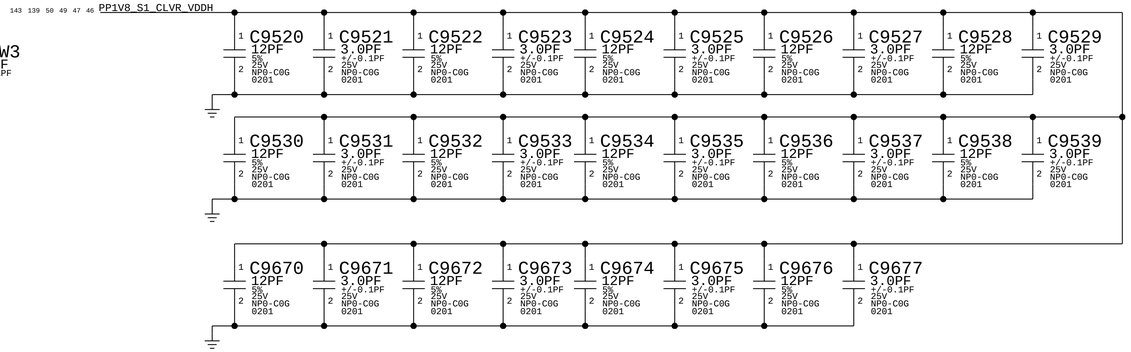


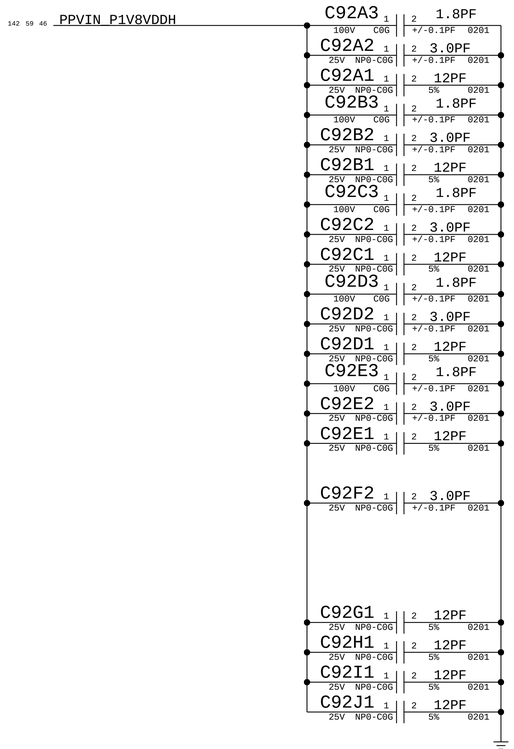
PH2



PH3

Desense caps below used to live in ref design





BOM_COST_GROUP=SOC POWER

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OK2INTEGRATE

AUSTRINGER CONTROLLER

ROUTE AUSTRINGER_BOOT_1, AUSTRINGER_GSW1, AUSTRINGER_GSENSE1 TOGETHER IN DIFFENTIAL-TRIPLET FASHION, WITH AUSTRINGER_GSW1 IN THE MIDDLE

R9330 0 0% 1/20W TK 0201
P1V8VDDH_PWR_EN
P1V8VDDH_PWR_EN_R
R9331 0 0% 1/20W TK 0201
P1V8VDDH_SLP_L
P1V8VDDH_SLP_R_L
R9310 1 5% 1/20W TK 0201
PPVIN_P1V8VDDH
PLACE_NEAR=U9300.34:10MM
C9310 2.2UF 20% 25V X6S-CERM 0402
R9315 1 5% 1/20W TK 0201
PP5V_S2_MAIN
PLACE_NEAR=U9300.39:10MM
C9315 2.2UF 20% 25V X6S-CERM 0402
PP1V2_S2
PLACE_NEAR=U9300.40:10MM
C9320 2.2UF 20% 25V X6S-CERM 0402
PLACE_NEAR=U9300.38:10MM
C9321 2.2UF 20% 25V X6S-CERM 0402
C9307 330PF 10% 16V X7R 0201
PLACE_NEAR=U9300:10MM
XW9300 SHORT-16L-0.1MM-SM
PP1V8_S1_CLVR_VDDH
PLACE_NEAR=UA100:10MM
P1V8S1MONVDDH_SENSE_R_P
R9305 0 0% 1/20W TK 0201
NOSTUFF
C9305 100PF 5% 50V C0G 0201-1
PLACE_NEAR=U9300:10MM
XW9301 SHORT-16L-0.1MM-SM
PLACE_NEAR=XW9300:5MM
P1V8S1MONVDDH_SENSE_R_N
R9306 0 0% 1/20W TK 0201
C9306 330PF 10% 16V X7R 0201
PLACE_NEAR=U9300:10MM
R9325 0 0% 1/20W TK 0201
P1V8VDDH_IREF_R
PLACE_NEAR=U9300.12:10MM
C9325 1UF 20% 10V X6S-CERM 0201
P1V8VDDH_IMON
R9323 200K 1% 1/20W TK 0201
PLACE_NEAR=U9300.10:10MM
P1V8VDDH_IMON_FILT
NOSTUFF
PLACE_NEAR=U9300.10:10MM
R9322 100K 1% 1/20W TK 0201
PLACE_NEAR=U9300.10:10MM
C9322 0.1UF 10% 25V X6S-CERM 0201
U9300
RAA225503A-3PH-SPM-A0-1
TQFN-THICKSTNCL
OMIT_TABLE
PPVIN_P1V8VDDH_CTRL_VIN 34 VIN
VOLTAGE=12V
PP5V_P1V8VDDH_CTRL_VCC 39 VCC
VOLTAGE=5V
P1V8VDDH_VPP 36 VPP
40 VIN1V2
PP1V5_P1V8VDDH_LDO15 38 LDO15
VOLTAGE=1.5V
P1V8VDDH_IMON 11 IMON
P1V8VDDH_IMON_FILT 10 IMON_FILT
P1V8VDDH_PWR_EN_R 3 ENABLE
P1V8VDDH_SLP_R_L 6 SLP*
P1V8VDDH_FAULT_L 37 FAULT*
P1V8S1MONVDDH_SENSE_P 8 VSENSE
P1V8S1MONVDDH_SENSE_N 9 VRTN
P1V8VDDH_IREF 12 IREF
P1V8VDDH_SPM_L_R 35 SPM*
EPAD 41
BOOT1 33 P1V8VDDH_BOOT1_R
GSW1 32 P1V8VDDH_GSW1_R
GSENSE1 31 P1V8VDDH_GSENSE1_R
PWM1 23 P1V8VDDH_DRMOS_PWM1
PWM2 24 P1V8VDDH_DRMOS_PWM2
PWM3 25 P1V8VDDH_DRMOS_PWM3
PWM4 26 P1V8VDDH_DRMOS_PWM4
PWM5 27 P1V8VDDH_DRMOS_PWM5
PWM6 28 NC_P1V8VDDH_DRMOS_PWM6
PWM7 29 NC_P1V8VDDH_DRMOS_PWM7
PWM8 30 NC_P1V8VDDH_DRMOS_PWM8
ISENSE1 13 P1V8VDDH_ISENSE1
ISENSE2 14 P1V8VDDH_ISENSE2
ISENSE3 15 P1V8VDDH_ISENSE3
ISENSE4 16 PP5V_P1V8VDDH_CTRL_VCC
ISENSE5 17 PP5V_P1V8VDDH_CTRL_VCC
ISENSE6 18
ISENSE7 19
ISENSE8 20
TSENSE 7 P1V8VDDH_DRMOS_TSENSE_R
SPS_EN 22 P1V8VDDH_DRMOS_EN
FET_FAULT* 21 P1V8VDDH_DRMOS_FAULT_L
TRIGGER0* 4 P1V8VDDH_ILIMIT_THROTTLE_L
TRIGGER1* 5 P1V8VDDH_TLIMIT_THROTTLE_L
SCLK 2 SPMI_NUB_P1V8VDDH_CLK
SDATA 1 SPMI_NUB_P1V8VDDH_DATA
PACK_OPTION=VDDH_3PH
PP5V_P1V8VDDH_CTRL_VCC
MAKE_BASE=TRUE
R9300 49.9 1% 1/20W TK 0201
SWITCH_NODE=TRUE DIDT=TRUE
P1V8VDDH_BOOT1
PLACE_NEAR=R9301:5MM
PLACE_NEAR=U9300.32:10MM
C9300 100PF 5% 50V C0G 0201-1
R9301 1 1% 1/20W TK 0201
P1V8VDDH_GSW1
PLACE_NEAR=C9301:5MM
NO_XNET_CONNECTION=1
PLACE_NEAR=U9300.32:10MM
C9301 100PF 5% 50V C0G 0201-1
NOSTUFF
R9302 49.9 1% 1/20W TK 0201
P1V8VDDH_GSENSE1
PLACE_NEAR=R9301:5MM
NO_XNET_CONNECTION=1
PLACE_NEAR=U9300.31:10MM
C9302 100PF 5% 50V C0G 0201-1
R9303 10K 1% 1/20W TK 0201
P1V8VDDH_DRMOS_TSENSE
C9303 470PF 10% 16V X5R-X7R-CERM 0201
PLACE_NEAR=U9300.7:10MM
PP5V_P1V8VDDH_CTRL_VCC
NOSTUFF
R9340 1K 1% 1/20W TK 0201
R9345 0 0% 1/20W TK 0201
P1V8VDDH_SPM_L_R
P1V8VDDH_SPM_L
R9341 1K 1% 1/20W TK 0201
CONTROLLER:AUSTRINGER
CONTROLLER:VIPER
PP5V_P1V8VDDH_CTRL_VCC
R9344 1K 1% 1/20W TK 0201
P1V8VDDH_VPP
PP5V_S2_MAIN
R9342 1K 1% 1/20W TK 0201
P1V8VDDH_DRMOS_FAULT_L
PP1V2_S2
R9343 100K 1% 1/20W TK 0201
P1V8VDDH_FAULT_L

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02884	1	IC,RAA225503,AUS,ES,3PH,SPM,A0_0,TQFN40	U9300	CRITICAL	AUSTRINGER:A0_3PH_SPM
353S03124	1	IC,RAA225503A,AUS,ES,3PH,SPM,A0_2,TQFN40	U9300	CRITICAL	AUSTRINGER:A0_2_3PH_SPM
353S03110	1	IC,RAA225503A,AUS,ES,5PH,SPM,A0_2,TQFN40	U9300	CRITICAL	AUSTRINGER:A0_5PH_SPM
353S03154	1	IC,RAA225503A,AUS,ES,3PH,SPM,A1_0,TQFN40	U9300	CRITICAL	AUSTRINGER:A1_0_3PH_SPM
353S03155	1	IC,RAA225503A,AUS,ES,5PH,SPM,A1_0,TQFN40	U9300	CRITICAL	AUSTRINGER:A1_0_5PH_SPM
353S02886	1	IC,RAA225503,AUS,ES,8PH,SPM,A0_0,TQFN40	U9300	CRITICAL	AUSTRINGER:A0_8PH_SPM
353S02887	1	IC,RAA225503,AUS,ES,3PH,APM,A0_0,TQFN40	U9300	CRITICAL	AUSTRINGER:A0_3PH_APM
353S02888	1	IC,RAA225503,AUS,ES,5PH,APM,A0_0,TQFN40	U9300	CRITICAL	AUSTRINGER:A0_5PH_APM
353S02889	1	IC,RAA225503,AUS,ES,8PH,APM,A0_0,TQFN40	U9300	CRITICAL	AUSTRINGER:A0_8PH_APM
353S02843	1	IC,RAA225502C,VIPER,5PH,OTP-A2_1,TQFN40	U9300	CRITICAL	VIPER:A2_1_5PH

PLEASE REFER TO BELOW RADAR FOR AUSTRINGER OTPS
RDAR://82847664 (UMBRELLA : AUSTRINGER OTP)

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PAGE TITLE: AUSTRINGER CONTROLLER

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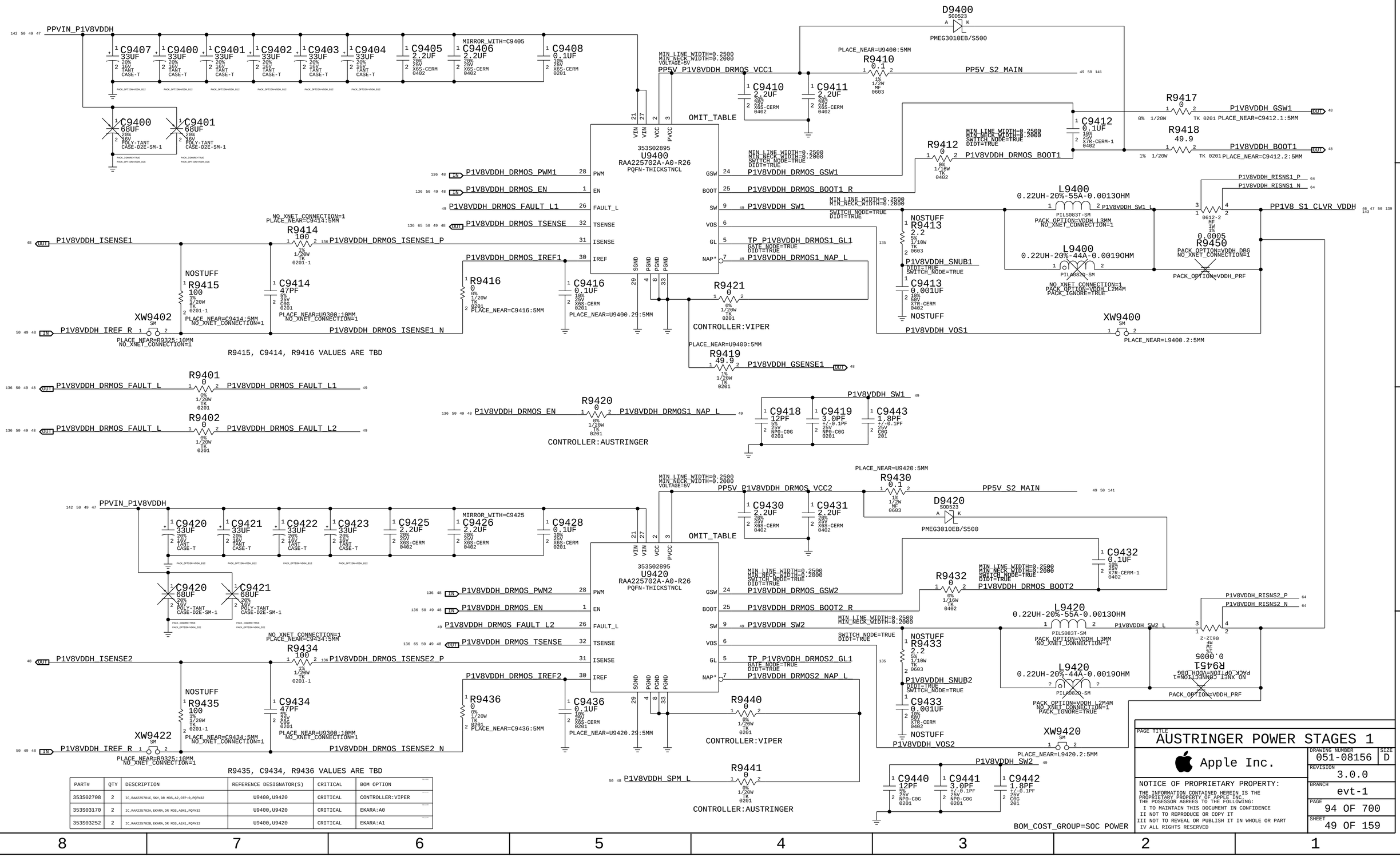
AUSTRINGER POWER STAGES 1



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02708	2	IC,RAA225701C,SKY,DR MOS,A2,OTP-0,PQFN32	U9400,U9420	CRITICAL	CONTROLLER:VIPER
353S03170	2	IC,RAA225702A,EKARA,DR MOS,A0N1,PQFN32	U9400,U9420	CRITICAL	EKARA:A0
353S03252	2	IC,RAA225702B,EKARA,DR MOS,A1N1,PQFN32	U9400,U9420	CRITICAL	EKARA:A1

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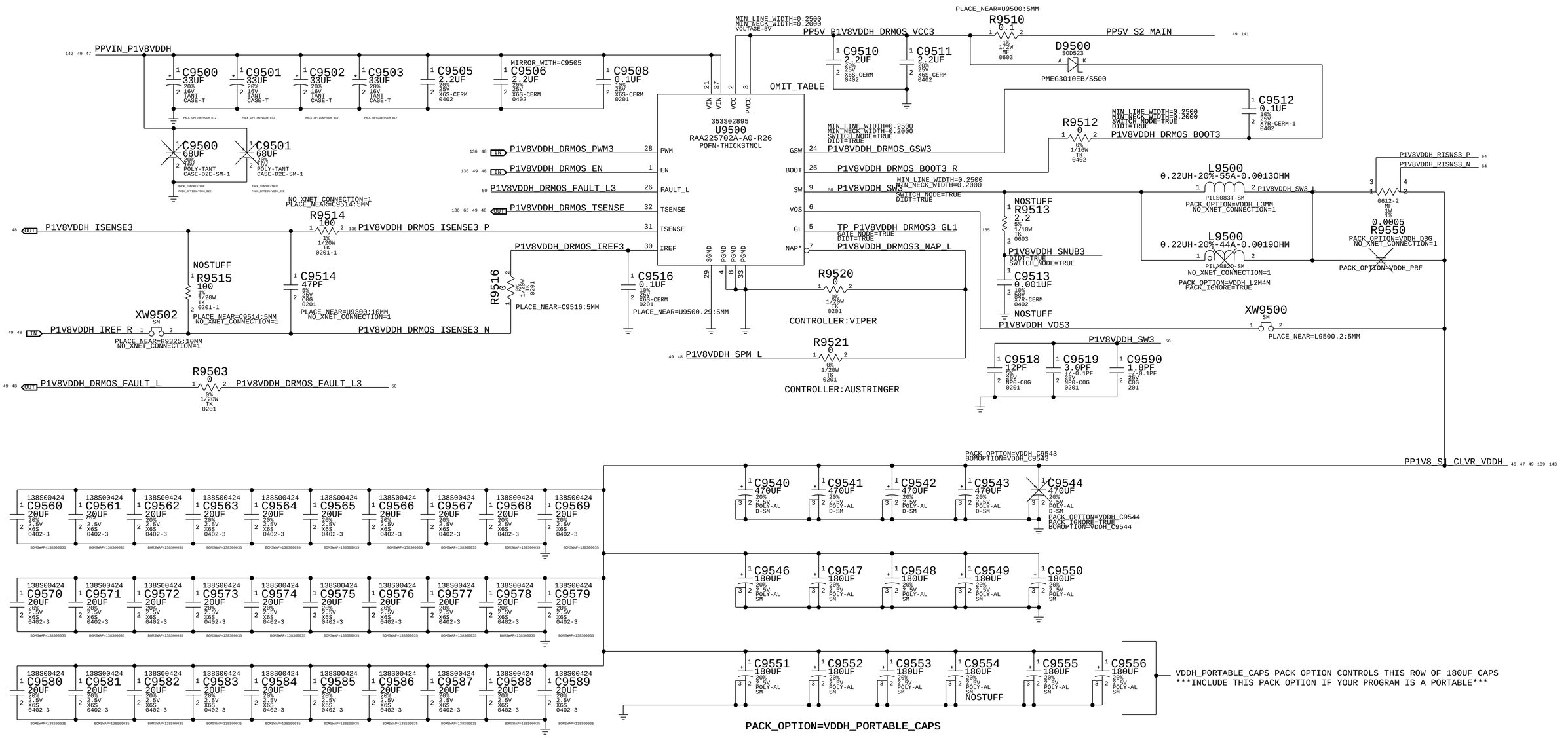
AUSTRINGER POWER STAGES 2



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S03170	1	IC,RAA225702A,EKARA,DR MOS,A0_1,PQFN32	U9500	CRITICAL	EKARA:A0
353S02708	1	IC,RAA225701C,SKY,DR MOS,A2,OTP-0,PQFN32	U9500	CRITICAL	CONTROLLER:VIPER
353S03252	1	IC,RAA225702B,EKARA,DR MOS,A1_N1,PQFN32	U9500	CRITICAL	EKARA:A1

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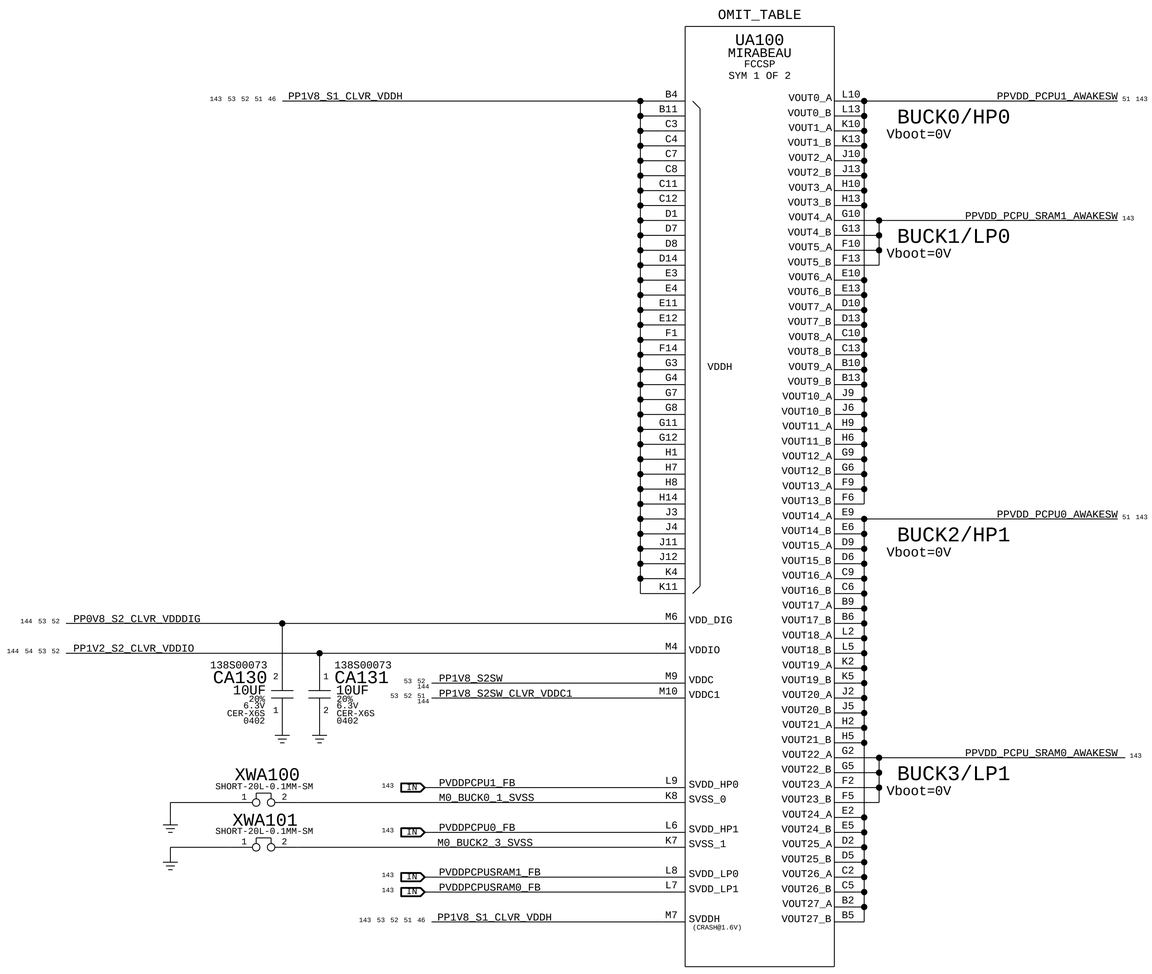
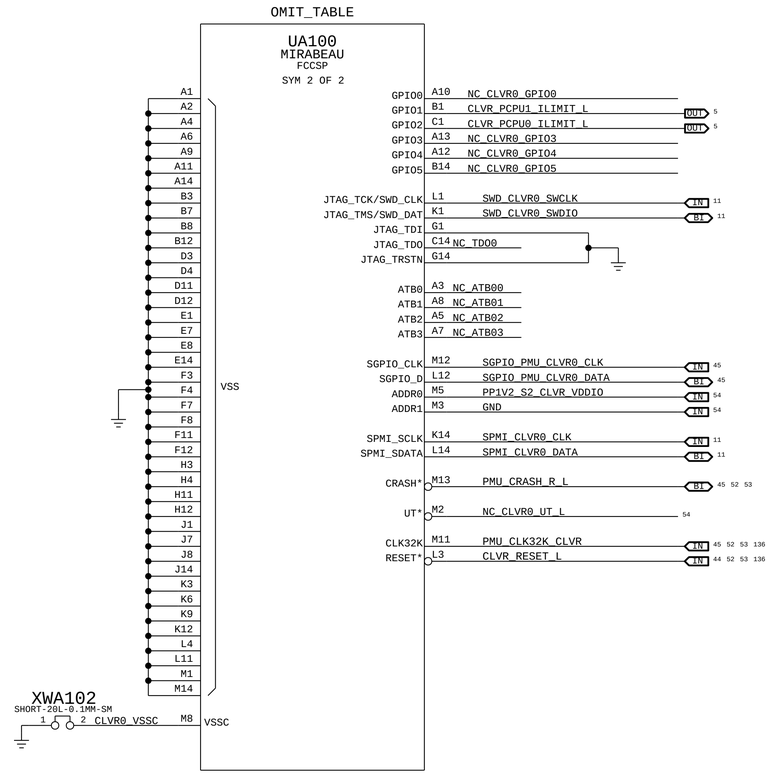
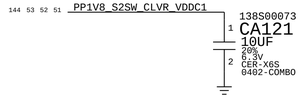
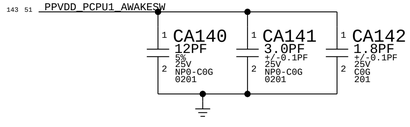
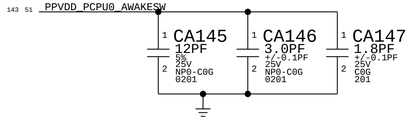
INSTANCE = C0
CFG = D (12+2+12+2)
OTP = MP_











PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-28851	1	IC,Mirabeau,A0,OTP-MPG	UA100	CRITICAL	
998-28851	1	IC,Mirabeau,A0,OTP-MPG	UA700	CRITICAL	MIRABEAU_D

BOM_COST_GROUP=SOC POWER

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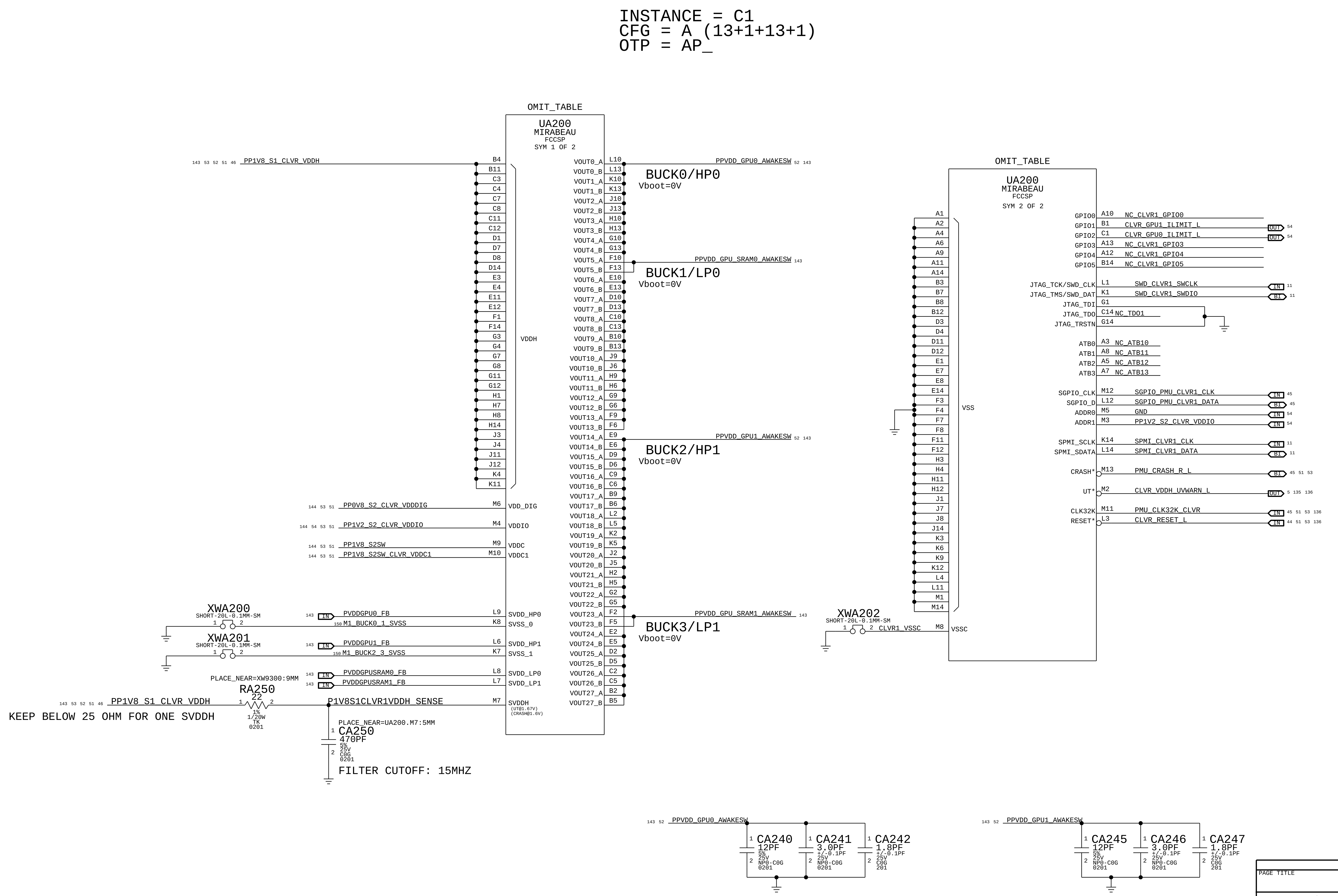
INSTANCE = C1
CFG = A (13+1+13+1)
OTP = AP_
OMIT_TABLE
UA200
MIRABEAU
FCCSP
SYM 1 OF 2
143 53 52 51 46 PP1V8_S1_CLVR_VDDH
B4 B11 C3 C4 C7 C8 C11 C12 D1 D7 D8 D14 E3 E4 E11 E12 F1 F14 G3 G4 G7 G8 G11 G12 H1 H7 H8 H14 J3 J4 J11 J12 K4 K11
VDDH
144 53 51 PP0V8_S2_CLVR_VDDDIG M6 VDD_DIG
144 54 53 51 PP1V2_S2_CLVR_VDDIO M4 VDDIO
144 53 51 PP1V8_S2SW M9 VDDC
144 53 51 PP1V8_S2SW_CLVR_VDDC1 M10 VDDC1
XWA200
SHORT-20L-0.1MM-SM
143 IN PVDDGPU0_FB L9 SVDD_HP0
150 M1_BUCK0_1_SVSS K8 SVSS_0
XWA201
SHORT-20L-0.1MM-SM
143 IN PVDDGPU1_FB L6 SVDD_HP1
150 M1_BUCK2_3_SVSS K7 SVSS_1
PLACE_NEAR=XW9300:9MM
143 IN PVDDGPUSRAM0_FB L8 SVDD_LP0
143 IN PVDDGPUSRAM1_FB L7 SVDD_LP1
RA250
22
1% 1/20W TK 0201
143 53 52 51 46 PP1V8_S1_CLVR_VDDH
P1V8S1CLVR1VDDH_SENSE M7 SVDDH (UT@1.67V) (CRASH@1.6V)
KEEP BELOW 25 OHM FOR ONE SVDDH
PLACE_NEAR=UA200.M7:5MM
CA250
470PF
5% 25V C0G 0201
FILTER CUTOFF: 15MHZ
VOUT0_A L10 VOUT0_B L13 VOUT1_A K10 VOUT1_B K13 VOUT2_A J10 VOUT2_B J13 VOUT3_A H10 VOUT3_B H13 VOUT4_A G10 VOUT4_B G13
VOUT5_A F10 VOUT5_B F13 VOUT6_A E10 VOUT6_B E13 VOUT7_A D10 VOUT7_B D13 VOUT8_A C10 VOUT8_B C13 VOUT9_A B10 VOUT9_B B13
VOUT10_A J9 VOUT10_B J6 VOUT11_A H9 VOUT11_B H6 VOUT12_A G9 VOUT12_B G6 VOUT13_A F9 VOUT13_B F6
VOUT14_A E9 VOUT14_B E6 VOUT15_A D9 VOUT15_B D6 VOUT16_A C9 VOUT16_B C6 VOUT17_A B9 VOUT17_B B6 VOUT18_A L2 VOUT18_B L5 VOUT19_A K2 VOUT19_B K5 VOUT20_A J2 VOUT20_B J5 VOUT21_A H2 VOUT21_B H5 VOUT22_A G2 VOUT22_B G5
VOUT23_A F2 VOUT23_B F5 VOUT24_A E2 VOUT24_B E5 VOUT25_A D2 VOUT25_B D5 VOUT26_A C2 VOUT26_B C5 VOUT27_A B2 VOUT27_B B5
PPVDD_GPU0_AWAKESW 52 143
BUCK0/HP0
Vboot=0V
PPVDD_GPU_SRAM0_AWAKESW 143
BUCK1/LP0
Vboot=0V
PPVDD_GPU1_AWAKESW 52 143
BUCK2/HP1
Vboot=0V
PPVDD_GPU_SRAM1_AWAKESW 143
BUCK3/LP1
Vboot=0V
OMIT_TABLE
UA200
MIRABEAU
FCCSP
SYM 2 OF 2
A1 A2 A4 A6 A9 A11 A14 B3 B7 B8 B12 D3 D4 D11 D12 E1 E7 E8 E14 F3 F4 F7 F8 F11 F12 H3 H4 H11 H12 J1 J7 J8 J14 K3 K6 K9 K12 L4 L11 M1 M14
VSS
XWA202
SHORT-20L-0.1MM-SM
CLVR1_VSSC M8 VSSC
GPIO0 A10 NC_CLVR1_GPIO0
GPIO1 B1 CLVR_GPU1_ILIMIT_L OUT 54
GPIO2 C1 CLVR_GPU0_ILIMIT_L OUT 54
GPIO3 A13 NC_CLVR1_GPIO3
GPIO4 A12 NC_CLVR1_GPIO4
GPIO5 B14 NC_CLVR1_GPIO5
JTAG_TCK/SWD_CLK L1 SWD_CLVR1_SWCLK IN 11
JTAG_TMS/SWD_DAT K1 SWD_CLVR1_SWDIO BI 11
JTAG_TDI G1
JTAG_TDO C14 NC_TDO1
JTAG_TRSTN G14
ATB0 A3 NC_ATB10
ATB1 A8 NC_ATB11
ATB2 A5 NC_ATB12
ATB3 A7 NC_ATB13
SGPIO_CLK M12 SGPIO_PMU_CLVR1_CLK IN 45
SGPIO_D L12 SGPIO_PMU_CLVR1_DATA BI 45
ADDR0 M5 GND IN 54
ADDR1 M3 PP1V2_S2_CLVR_VDDIO IN 54
SPMI_SCLK K14 SPMI_CLVR1_CLK IN 11
SPMI_SDATA L14 SPMI_CLVR1_DATA BI 11
CRASH* M13 PMU_CRASH_R_L BI 45 51 53
UT* M2 CLVR_VDDH_UVWARN_L OUT 5 135 136
CLK32K M11 PMU_CLK32K_CLVR IN 45 51 53 136
RESET* L3 CLVR_RESET_L IN 44 51 53 136
143 52 PPVDD_GPU0_AWAKESW
CA240 12PF 5% 25V NP0-C0G 0201
CA241 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA242 1.8PF +/-0.1PF 25V C0G 201
143 52 PPVDD_GPU1_AWAKESW
CA245 12PF 5% 25V NP0-C0G 0201
CA246 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA247 1.8PF +/-0.1PF 25V C0G 201

TODO_DT: Update with APN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-28849	1	IC,Mirabeau,A0,OTP-APG	UA200	CRITICAL	
998-28849	1	IC,Mirabeau,A0,OTP-APG	UA300	CRITICAL	MIRABEAU_C
998-28849	3	IC,Mirabeau,A0,OTP-APG	UA300,UA800,UA900	CRITICAL	MIRABEAU_D

BOM_COST_GROUP=SOC POWER

PAGE TITLE
CLVR1

Apple Inc.

DRAWING NUMBER 051-08156 SIZE D
REVISION 3.0.0
BRANCH evt-1

8 7 6 5 4 3 2 1

OK2INTEGRATE

TODO_DT: Quantity of desense and 11uF VDDH caps is still TBD based on layout study. Baseline is from X2724/X2728 quantity
TODO_DT: Potentitally add or remove, or PACK_OPTION some desense input caps based on layout

PP1V8_S1_CLVR_VDDH 46 51 52 53 143

11UF APN: 138S00328

INSTANCE = C2
CFG = C (8+1+13+6)
OTP = IP_

CA600 CA601 CA602 CA603 CA604 CA605 CA606 CA607 CA608 CA609
11UF 20% 2.5V X6T 0402

CA610 CA611 CA612 CA613 CA614 CA615 CA616 CA617 CA618 CA619
11UF 20% 2.5V X6T 0402

CA620 CA621 CA622 CA623 CA624 CA625 CA626 CA627
11UF 20% 2.5V X6T 0402

CLVR0

CA650 1.8PF +/-0.1PF 25V C0G 201
CA651 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA652 12PF 5% 25V NP0-C0G 0201
CA653 1.8PF +/-0.1PF 25V C0G 201
CA654 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA655 12PF 5% 25V NP0-C0G 0201

CLVR1

CA660 1.8PF +/-0.1PF 25V C0G 201
CA661 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA662 12PF 5% 25V NP0-C0G 0201
CA663 1.8PF +/-0.1PF 25V C0G 201
CA664 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA665 12PF 5% 25V NP0-C0G 0201

CLVR2

CA670 1.8PF +/-0.1PF 25V C0G 201
CA671 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA672 12PF 5% 25V NP0-C0G 0201
CA673 1.8PF +/-0.1PF 25V C0G 201
CA674 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA675 12PF 5% 25V NP0-C0G 0201
CA676 1.8PF +/-0.1PF 25V C0G 201
CA677 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA678 12PF 5% 25V NP0-C0G 0201

OMIT_TABLE

UA600
MIRABEAU
FCCSP
SYM 1 OF 2

B4 B11 C3 C4 C7 C8 C11 C12 D1 D7 D8 D14 E3 E4 E11 E12 F1 F14 G3 G4 G7 G8 G11 G12 H1 H7 H8 H14 J3 J4 J11 J12 K4 K11 — VDDH

VOUT0_A L10
VOUT0_B L13
VOUT1_A K10 — PPVDD_ANE_AWAKESW 53 143
VOUT1_B K13
VOUT2_A J10
VOUT2_B J13
VOUT3_A H10
VOUT3_B H13
VOUT4_A G10
VOUT4_B G13
VOUT5_A F10 — PPVDD_ANE_SRAM_AWAKESW 143
VOUT5_B F13
VOUT6_A E10
VOUT6_B E13
VOUT7_A D10
VOUT7_B D13
VOUT8_A C10
VOUT8_B C13
VOUT9_A B10
VOUT9_B B13
VOUT10_A J9 — PPVDD_FABRIC_S1 53 143
VOUT10_B J6
VOUT11_A H9
VOUT11_B H6
VOUT12_A G9
VOUT12_B G6
VOUT13_A F9
VOUT13_B F6
VOUT14_A E9
VOUT14_B E6
VOUT15_A D9
VOUT15_B D6
VOUT16_A C9
VOUT16_B C6
VOUT17_A B9
VOUT17_B B6
VOUT18_A L2 — PPVDD_AFR_CS_S1 53 143
VOUT18_B L5
VOUT19_A K2
VOUT19_B K5
VOUT20_A J2
VOUT20_B J5
VOUT21_A H2
VOUT21_B H5
VOUT22_A G2
VOUT22_B G5
VOUT23_A F2
VOUT23_B F5
VOUT24_A E2
VOUT24_B E5
VOUT25_A D2
VOUT25_B D5
VOUT26_A C2
VOUT26_B C5
VOUT27_A B2
VOUT27_B B5

BUCK0/HP0
Vboot=0V

BUCK1/LP0
Vboot=0V

BUCK2/HP1
Vboot=750mV

BUCK3/LP1
Vboot=700mV

144 52 51 PP0V8_S2_CLVR_VDDDIG — M6 VDD_DIG
144 54 52 51 PP1V2_S2_CLVR_VDDIO — M4 VDDIO
144 52 51 PP1V8_S2SW — M9 VDDC
144 52 51 PP1V8_S2SW_CLVR_VDDC1 — M10 VDDC1

XWA600 SHORT-20L-0.1MM-SM
143 IN PVDDANE_FB — L9 SVDD_HP0
M2_BUCK0_1_SVSS — K8 SVSS_0

XWA601 SHORT-20L-0.1MM-SM
143 IN PVDDFABRIC_FB — L6 SVDD_HP1
M2_BUCK2_3_SVSS — K7 SVSS_1

143 IN PVDDANESRAM_FB — L8 SVDD_LP0
143 IN PVDDAFRCS_FB — L7 SVDD_LP1

143 53 52 51 46 PP1V8_S1_CLVR_VDDH — M7 SVDDH (CRASH@1.6V)

143 53 PPVDD_ANE_AWAKESW
CA640 12PF 5% 25V NP0-C0G 0201
CA641 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA642 1.8PF +/-0.1PF 25V C0G 201

143 53 PPVDD_FABRIC_S1
CA645 12PF 5% 25V NP0-C0G 0201
CA646 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA647 1.8PF +/-0.1PF 25V C0G 201

143 53 PPVDD_AFR_CS_S1
CA64A 12PF 5% 25V NP0-C0G 0201
CA64B 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA64C 1.8PF +/-0.1PF 25V C0G 201

OMIT_TABLE

UA600
MIRABEAU
FCCSP
SYM 2 OF 2

A1 A2 A4 A6 A9 A11 A14 B3 B7 B8 B12 D3 D4 D11 D12 E1 E7 E8 E14 F3 F4 F7 F8 F11 F12 H3 H4 H11 H12 J1 J7 J8 J14 K3 K6 K9 K12 L4 L11 M1 M14 — VSS

GPIO0 A10 NC_CLVR2_GPIO0
GPIO1 B1 CLVR_ANE_ILIMIT_L — OUT 5
GPIO2 C1 CLVR_FABRIC_ILIMIT_L — OUT 5
GPIO3 A13 CLVR_AFRCS_ILIMIT_L — OUT 5
GPIO4 A12 NC_CLVR2_GPIO4
GPIO5 B14 NC_CLVR2_GPIO5

JTAG_TCK/SWD_CLK L1 SWD_CLVR2_SWCLK — IN 11
JTAG_TMS/SWD_DAT K1 SWD_CLVR2_SWDIO — BI 11
JTAG_TDI G1
JTAG_TDO C14 NC_TDO3
JTAG_TRSTN G14

ATB0 A3 NC_ATB30
ATB1 A8 NC_ATB31
ATB2 A5 NC_ATB32
ATB3 A7 NC_ATB33

SGPIO_CLK M12 SGPIO_PMU_CLVR2_CLK — IN 45
SGPIO_D L12 SGPIO_PMU_CLVR2_DATA — BI 45
ADDR0 M5 PP1V2_S2_CLVR_VDDIO — IN 54
ADDR1 M3 GND — IN 54

SPMI_SCLK K14 SPMI_CLVR2_CLK — IN 11
SPMI_SDATA L14 SPMI_CLVR2_DATA — BI 11

CRASH* M13 PMU_CRASH_R_L — BI 45 51 52
UT* M2 NC_CLVR2_UT_L 54

CLK32K M11 PMU_CLK32K_CLVR — IN 45 51 52 136
RESET* L3 CLVR_RESET_L — IN 44 51 52 136

XWA602 SHORT-20L-0.1MM-SM
M8 VSSC — 2 CLVR2_VSSC 1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-28850	1	IC,Mirabeau,A0,OTP-IPG	UA600	CRITICAL	

BOM_COST_GROUP=SOC POWER

PAGE TITLE
CLVR2 (S)

Apple Inc.

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CLVR Throttle Probe Access (Different between S,C,D)

52 CLVR_GPU1_ILIMIT_L — CLVR_GPU1_ILIMIT_L 5
MAKE_BASE=TRUE

52 CLVR_GPU0_ILIMIT_L — CLVR_GPU0_ILIMIT_L 5
MAKE_BASE=TRUE

CLVR Address Straps (Different between S vs C/D)

SWD TINSTANCE and SGPIO SID are the same value within a given CLVR
ADDR[1:0] define LSB
OTP defines MSB

CLVR	Hex	MSB (OTP)	LSB (ADDR strap)	
0	0x1	b00	b01 :	51 OUT PP1V2_S2_CLVR_VDDIO — PP1V2_S2_CLVR_VDDIO 51 52 53 54 144
				51 OUT GND — GND MAKE_BASE=TRUE
1	0x2	b00	b10 :	52 OUT GND — GND MAKE_BASE=TRUE
				52 OUT PP1V2_S2_CLVR_VDDIO — PP1V2_S2_CLVR_VDDIO 51 52 53 54 144
2	0x9	b10	b01 :	53 OUT PP1V2_S2_CLVR_VDDIO — PP1V2_S2_CLVR_VDDIO 51 52 53 54 144
				53 OUT GND — GND MAKE_BASE=TRUE

51 NC_CLVR0_UT_L — NC_CLVR0_UT_L
MAKE_BASE=TRUE

53 NC_CLVR2_UT_L — NC_CLVR2_UT_L
MAKE_BASE=TRUE

BOM_COST_GROUP=SOC POWER

PAGE TITLE
CLVR PROJECT SUPPORT (S)

Apple Inc.

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* OK2INTEGRATE *

5V_S2 Voltage Regulator (low power option)

SET ONE OPTION FOR PBUS CAPS

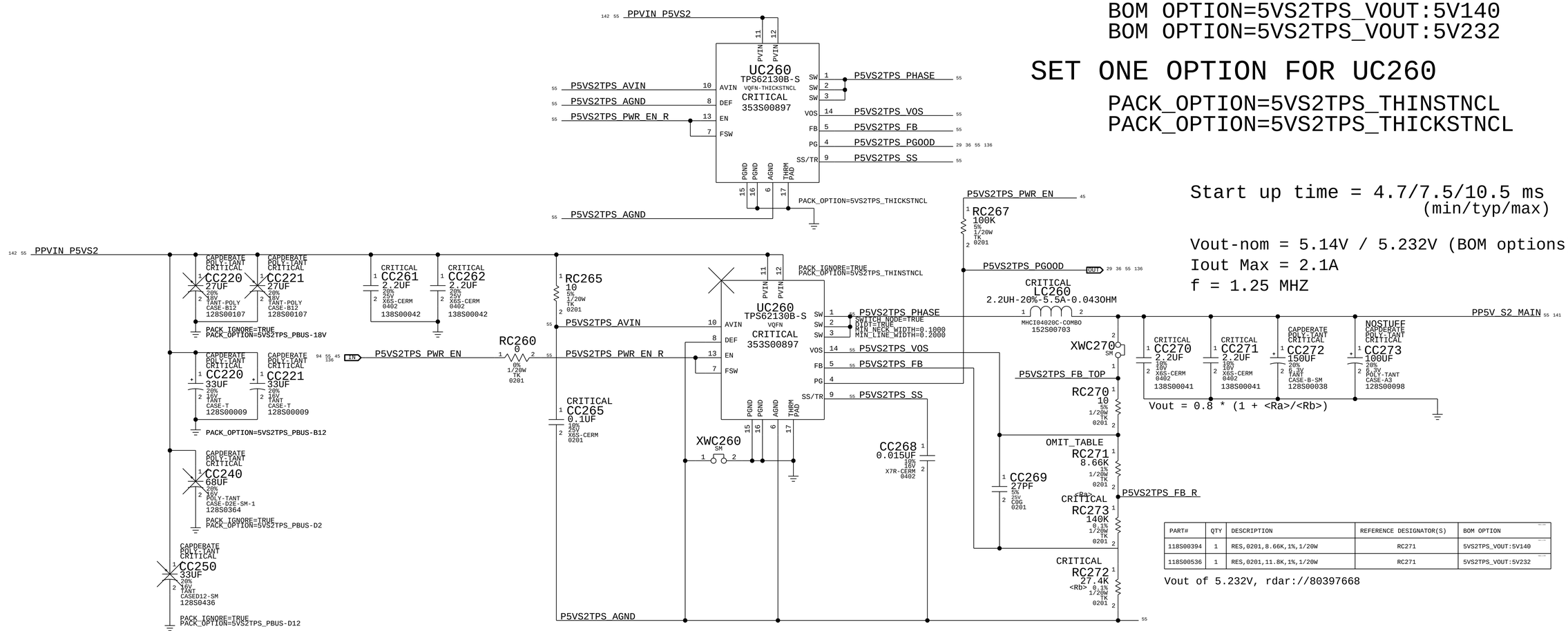
PACK_OPTION=5VS2TPS_PBUS-B12
PACK_OPTION=5VS2TPS_PBUS-D2
PACK_OPTION=5VS2TPS_PBUS-D12
PACK_OPTION=5VS2TPS_PBUS-18V

SET ONE OPTION FOR OUTPUT VOLTAGE

BOM OPTION=5VS2TPS_VOUT:5V140
BOM OPTION=5VS2TPS_VOUT:5V232

SET ONE OPTION FOR UC260

PACK_OPTION=5VS2TPS_THINSTNCL
PACK_OPTION=5VS2TPS_THICKSTNCL

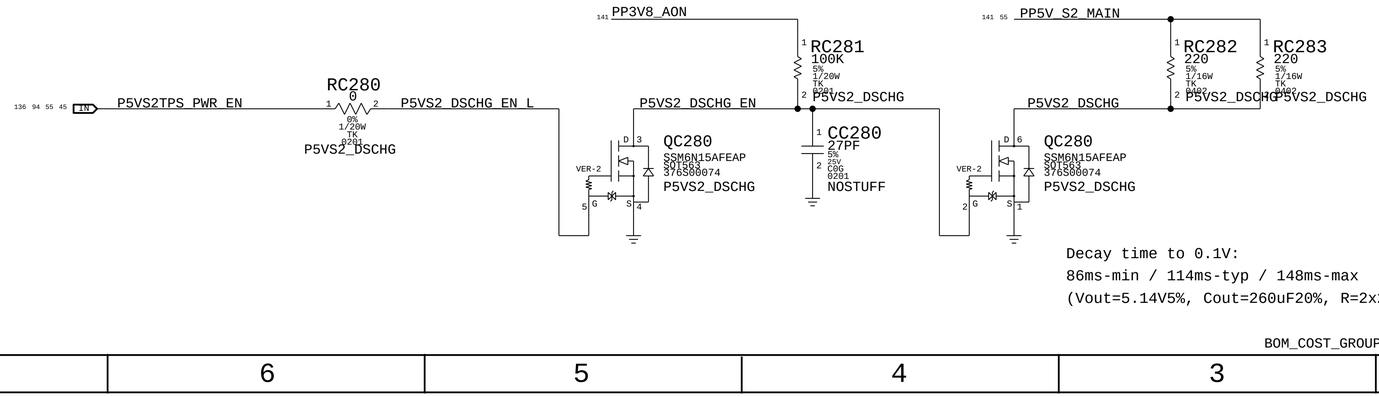


Start up time = 4.7/7.5/10.5 ms (min/typ/max)

Vout-nom = 5.14V / 5.232V (BOM options)
Iout Max = 2.1A
f = 1.25 MHZ

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
118S00394	1	RES,0201,8.66K,1%,1/20W	RC271	5VS2TPS_VOUT:5V140
118S00536	1	RES,0201,11.8K,1%,1/20W	RC271	5VS2TPS_VOUT:5V232

Vout of 5.232V, rdar://80397668



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: POWER: 5V S2 TPS62130

Apple Inc.

DRAWING NUMBER: 051-08156 | SIZE: D
REVISION: 3.0.0
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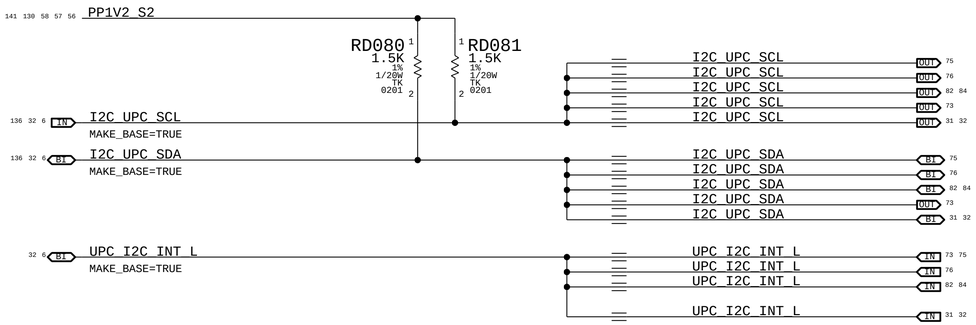
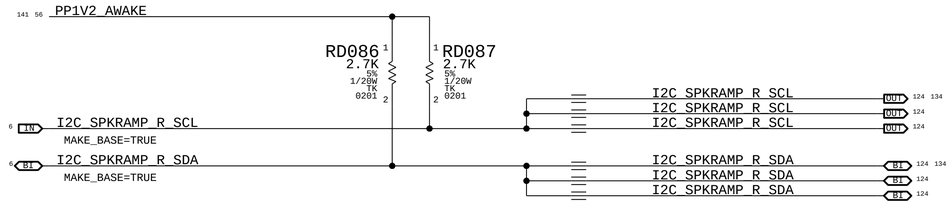
AP_I2C0

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	0	380kHz	0X38	0X70	ACE2 - 0 (DEBUG)
AP	0	380kHz	0X3F	0X7E	ACE2 - 1 (DEBUG)
AP	0	380kHz	0X3B	0X76	ACE2 - 2 (DEBUG)
AP	0	380kHz	0X3A	0X74	ACE2 - 5 (DEBUG)
AP	0	380kHz	0X6B	0XD6	BANK ALL CALL



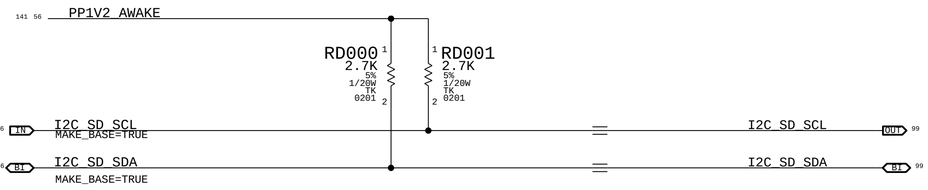
AP_I2C3

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	3	400kHz	0x3B	0x76	SPKRAMP_TAWANG_D
AP	3	400kHz	0x3C	0x78	SPKRAMP_TAWANG_E
AP	3	400kHz	0x3D	0x7A	SPKRAMP_TAWANG_F



AP_I2C4

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	4	400kHz	0x6A	0xD4	SDCARD

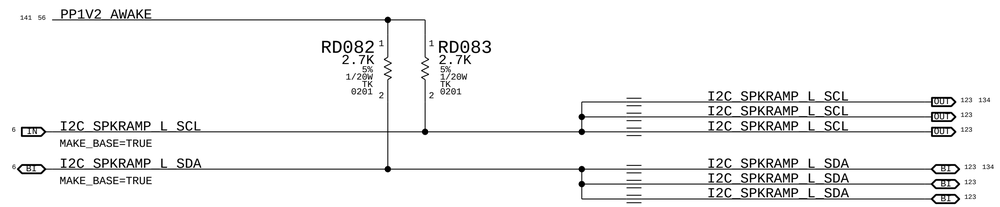


UNUSED:

AOP_I2C1
ISP_I2C0
ISP_I2C1
ISP_I2C3

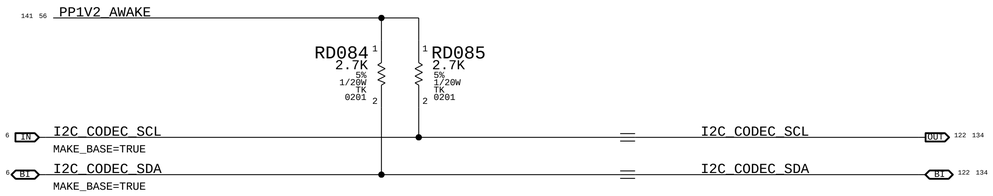
AP_I2C1

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	1	400kHz	0x38	0x70	SPKRAMP_TAWANG_A
AP	1	400kHz	0x39	0x72	SPKRAMP_TAWANG_B
AP	1	400kHz	0x3A	0x74	SPKRAMP_TAWANG_C



AP_I2C2

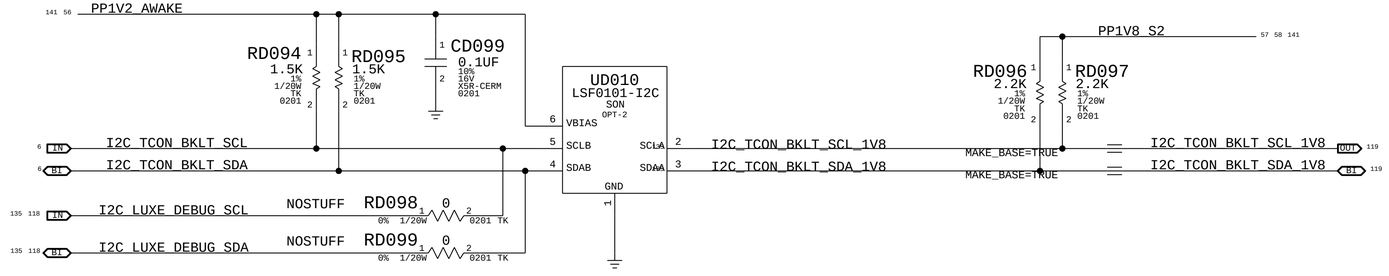
MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	2	400kHz	0x48	0x90	CODEC - CLIFDEN
AP	2	400kHz	0x4B	0x95	CODEC - CARLOW (POR)



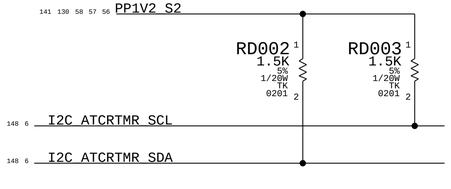
AP_I2C7

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	7	1MHz	0XXX	0XX	Aveillino PMIC

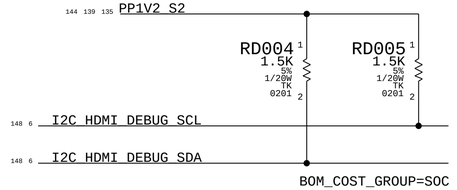
I2C is hooked up to testpoints on BCON brd

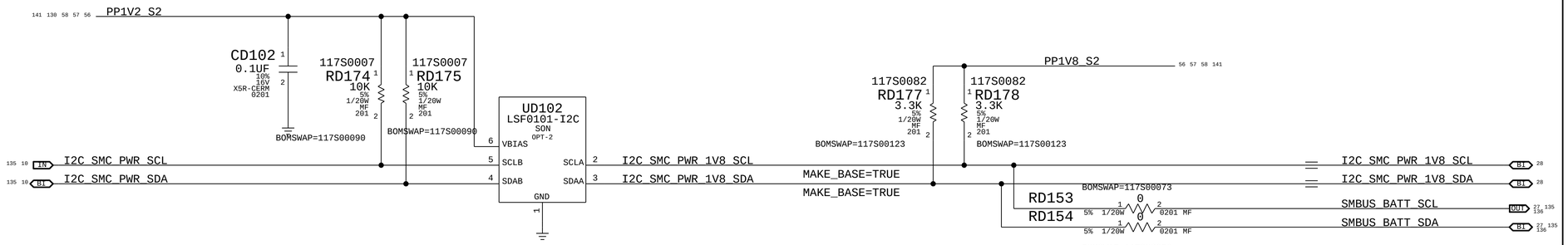


AP_I2C6



AP_I2C8





SMC_I2C0

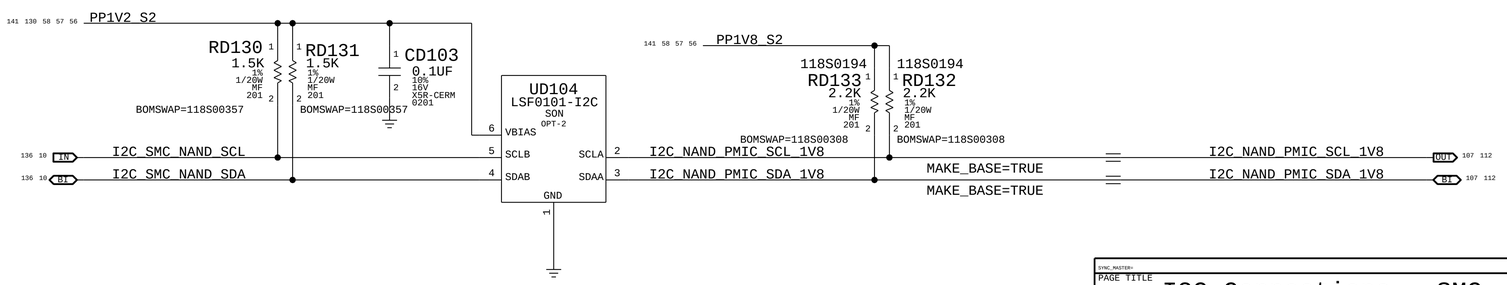
MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	0	400kHz	0X09	0X12	CHARGER - SUONA
SMC	0	400kHz	0X09	0X12	CHARGER - WHAMOLA
SMC	0	NC	0XXX	0XX	ICEMAN
SMC	0	400kHz	0X0B	0X16	BMU

SMC_I2C1

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	1	363kHz	0X38	0X70	ACE2 - 0 (DEBUG)
SMC	1	363kHz	0X3F	0X7E	ACE2 - 1 (DEBUG)
SMC	1	363kHz	0X3B	0X76	ACE2 - 2 (DEBUG)
SMC	1	363kHz	0X3A	0X74	ACE2 - 5 (DEBUG)
SMC	1	363kHz	0X6B	0XD6	BANK1 ALL CALL

SMC_I2C2

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	2	100kHz	0X79	0XF2	NAND PMIC 0
SMC	2	100kHz	0X78	0XF0	NAND PMIC 1



BOM_COST_GROUP=SOC

SYNC_MASTER= SYNC_DATE=

PAGE TITLE

I2C Connections - SMC

Apple Inc.

DRAWING NUMBER 051-08156 SIZE D

REVISION 3.0.0

BRANCH evt-1

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SMC_I2C3

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	3	400kHz	0X4C	0X98	Palm Rest Temp

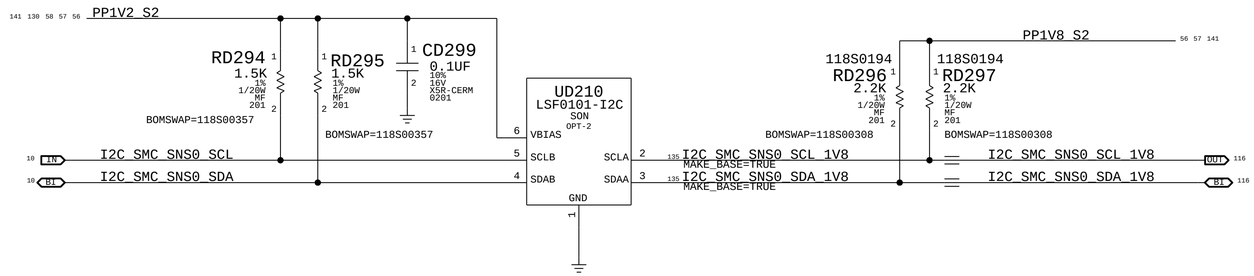
CHECK SPEED VALUE

Moved to IPD Ref design

SMC_I2C4

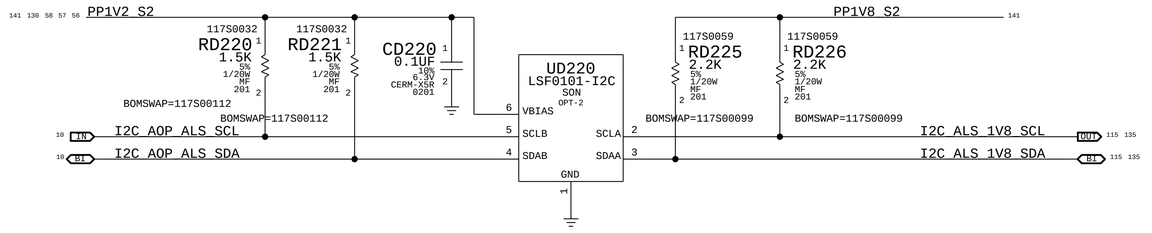
MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	4	400kHz	0X48	0X90	Temp Sensors

CHECK SPEED VALUE



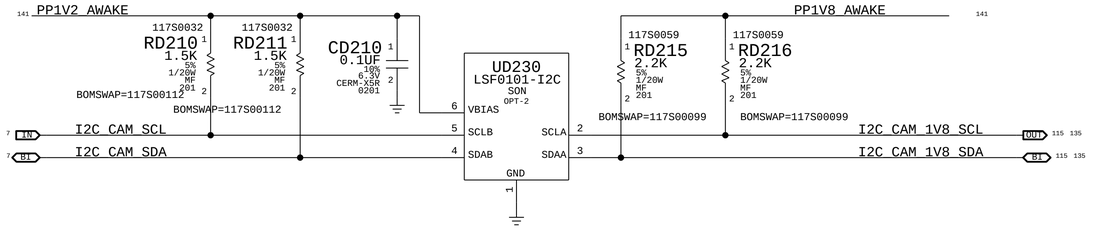
AOP_I2C0

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AOP	0	400kHz	0X29	0X52	ALS
AOP	0	400kHz	0X24	0X48	ALS Temp



ISP_I2C2

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
ISP	2	400kHz	0X10	0X20	FHS1+
ISP	2	400kHz	0X6C	0XD8	Camera Sensor



UNUSED and already aliased
ISP_I2C0 SMC_I2C6
ISP_I2C1
ISP_I2C3
AOP_I2C1

SI2C

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
S	0	400kHz	0XXX	0XX	SEP EEPROM

Need to confirm if this needs/has pull-ups

MISSING WLAN/BT, R1, CELL - VENDOR CARDS

BOM_COST_GROUP=SOC

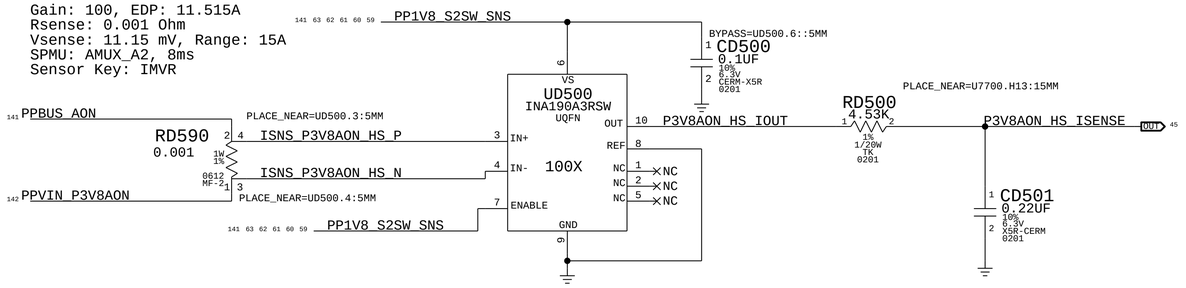
PAGE TITLE: I2C Connections - Other

Apple Inc.

DRAWING NUMBER: 051-08156 | SIZE: D
REVISION: 3.0.0
BRANCH: evt-1
PAGE: 132 OF 700
SHEET: 58 OF 159

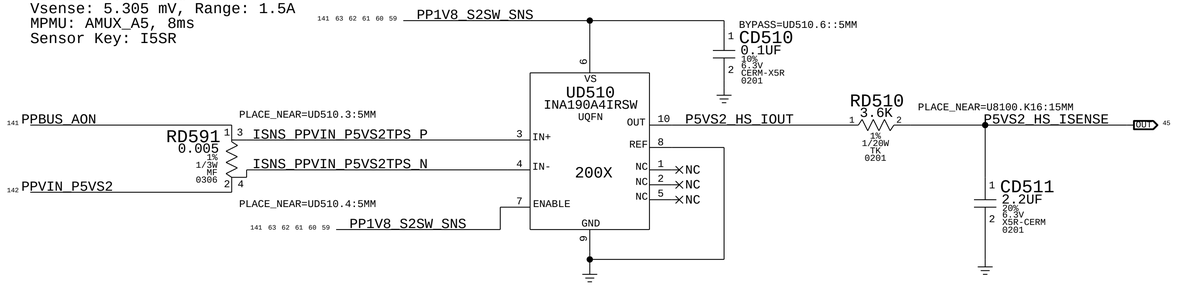
P3V8 AON HIGH SIDE ISENSE

Gain: 100, EDP: 11.515A
Rsense: 0.001 Ohm
Vsense: 11.15 mV, Range: 15A
SPMU: AMUX_A2, 8ms
Sensor Key: IMVR



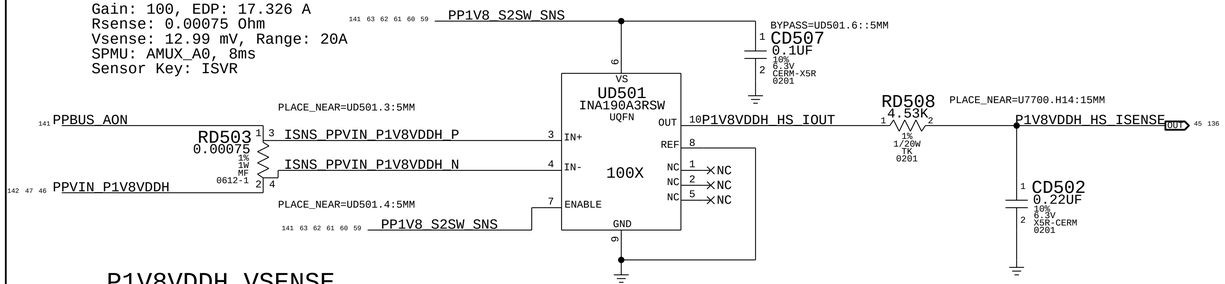
5V S2 VR HIGH SIDE ISENSE

Gain: 200, EDP: 1.061A
Rsense: 0.005 Ohm
Vsense: 5.305 mV, Range: 1.5A
MPMU: AMUX_A5, 8ms
Sensor Key: I5SR



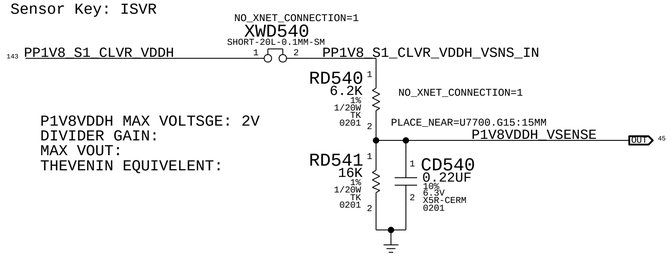
P1V8VDDH HIGH SIDE ISENSE

Gain: 100, EDP: 17.326 A
Rsense: 0.00075 Ohm
Vsense: 12.99 mV, Range: 20A
SPMU: AMUX_A0, 8ms
Sensor Key: ISVR



P1V8VDDH VSENSE

SPMU: AMUX_A1, 8ms
Sensor Key: ISVR



P1V8VDDH MAX VOLTSGE: 2V
DIVIDER GAIN:
MAX VOUT:
THEVENIN EQUIVELENT:

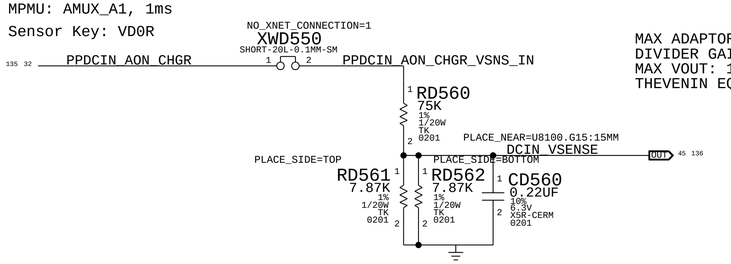
P3V8AON VSENSE

SPMU: AMUX_A2, 8ms

REMOVED in J414c

DCIN VOLTAGE SENSE

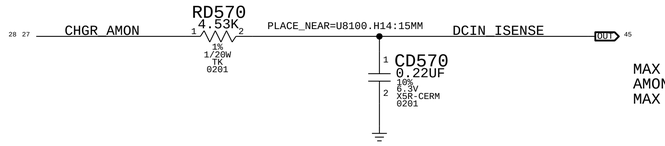
MPMU: AMUX_A1, 1ms
Sensor Key: VD0R



MAX ADAPTOR VOLTAGE = 28V + 5% -> 30V
DIVIDER GAIN: 0.0491
MAX VOUT: 1.4733
THEVENIN EQUIVELENT: 4.47K

DCIN ISENSE AMON

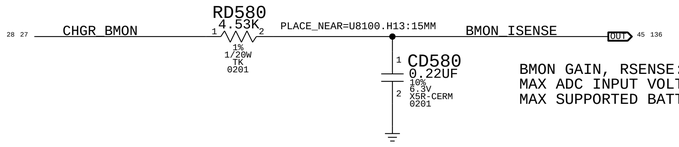
MPMU: AMUX_A0, 1ms
Sensor Key: ID0R



MAX ADAPTOR CURRENT: 5A
AMON GAIN, RSENSE: 20X, 10m
MAX AMON OUTPUT VOLTAGE: 1V

BATTERY ISENSE BMON

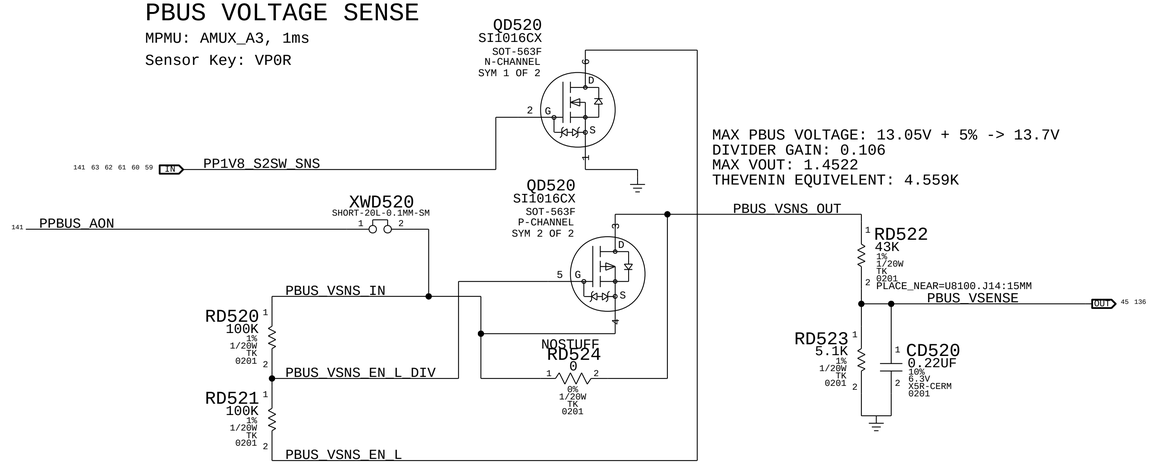
MPMU: AMUX_A2, 1ms
Sensor Key: IPBR



BMON GAIN, RSENSE: 7.9X, 5m
MAX ADC INPUT VOLTAGE: 1.5V (G=1)
MAX SUPPORTED BATTERY CURRENT SENSE: 37.97A

PBUS VOLTAGE SENSE

MPMU: AMUX_A3, 1ms
Sensor Key: VP0R



MAX PBUS VOLTAGE: 13.05V + 5% -> 13.7V
DIVIDER GAIN: 0.106
MAX VOUT: 1.4522
THEVENIN EQUIVELENT: 4.559K

BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: HIGH-SIDE (1/3)

Apple Inc.

DRAWING NUMBER: 051-08156
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REVISION: 3.0.0
BRANCH: evt-1
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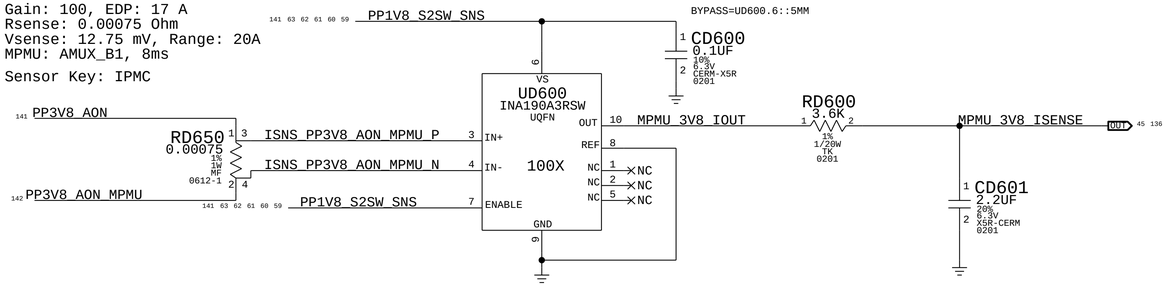
MPMU HIGH SIDE 3V8 ISENSE

Gain: 100, EDP: 17 A
Rsense: 0.00075 Ohm
Vsense: 12.75 mV, Range: 20A
MPMU: AMUX_B1, 8ms

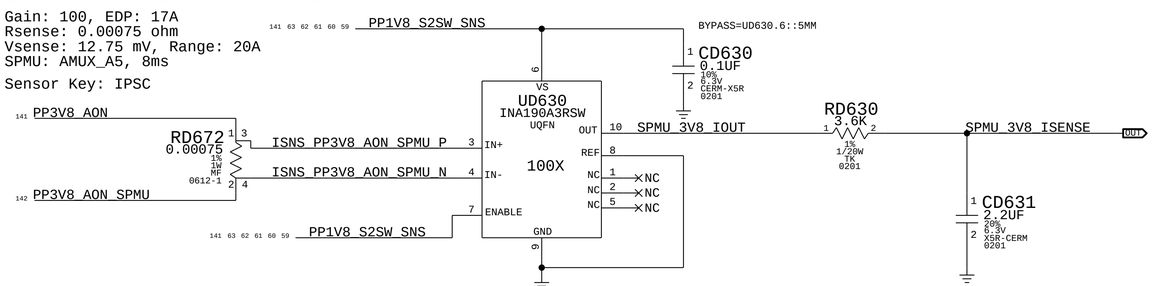
Sensor Key: IPMC



SPMU HIGH SIDE 3V8 ISENSE

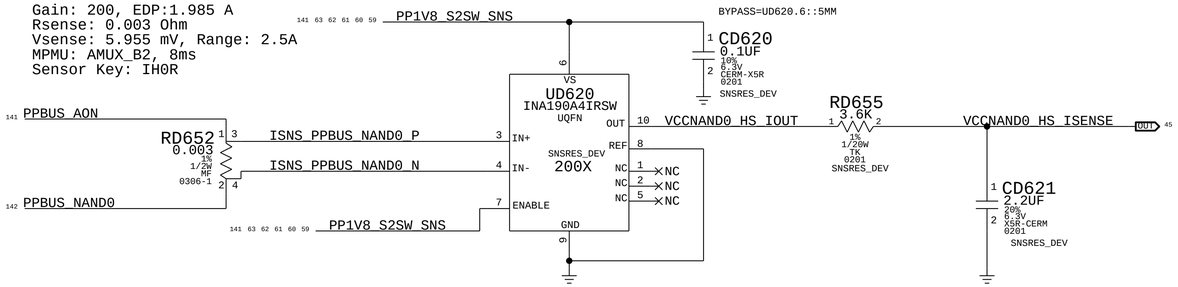
Gain: 100, EDP: 17A
Rsense: 0.00075 ohm
Vsense: 12.75 mV, Range: 20A
SPMU: AMUX_A5, 8ms

Sensor Key: IPSC



NAND 0 PBUS ISENSE

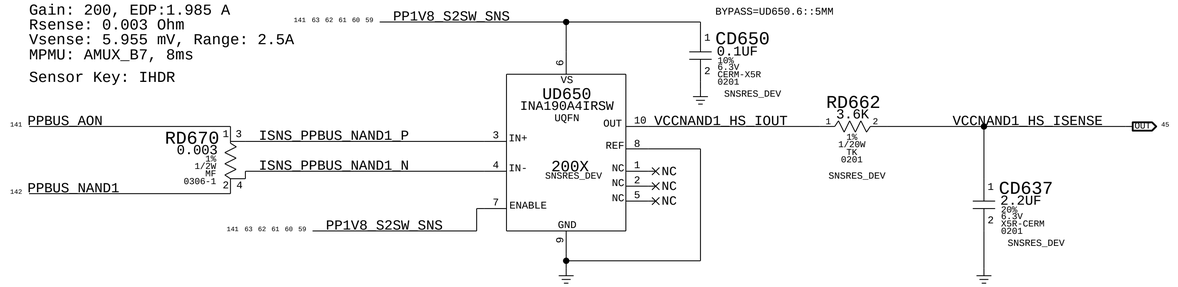
Gain: 200, EDP:1.985 A
Rsense: 0.003 Ohm
Vsense: 5.955 mV, Range: 2.5A
MPMU: AMUX_B2, 8ms
Sensor Key: IH0R



NAND 1 PBUS ISENSE

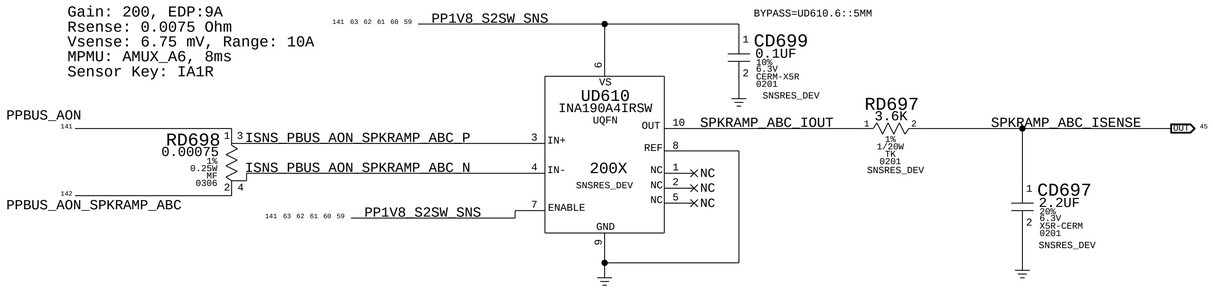
Gain: 200, EDP:1.985 A
Rsense: 0.003 Ohm
Vsense: 5.955 mV, Range: 2.5A
MPMU: AMUX_B7, 8ms

Sensor Key: IHDR



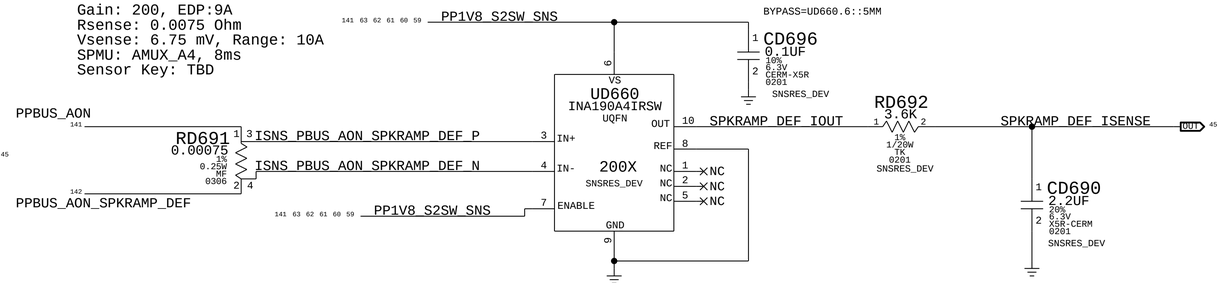
LEFT SPKRAMP PBUS ISENSE

Gain: 200, EDP:9A
Rsense: 0.0075 Ohm
Vsense: 6.75 mV, Range: 10A
MPMU: AMUX_A6, 8ms
Sensor Key: IA1R



RIGHT SPKRAMP PBUS ISENSE

Gain: 200, EDP:9A
Rsense: 0.0075 Ohm
Vsense: 6.75 mV, Range: 10A
SPMU: AMUX_A4, 8ms
Sensor Key: TBD



BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: HIGH-SIDE (2/3)

Apple Inc.

DRAWING NUMBER 051-08156
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REVISION 3.0.0
BRANCH evt-1
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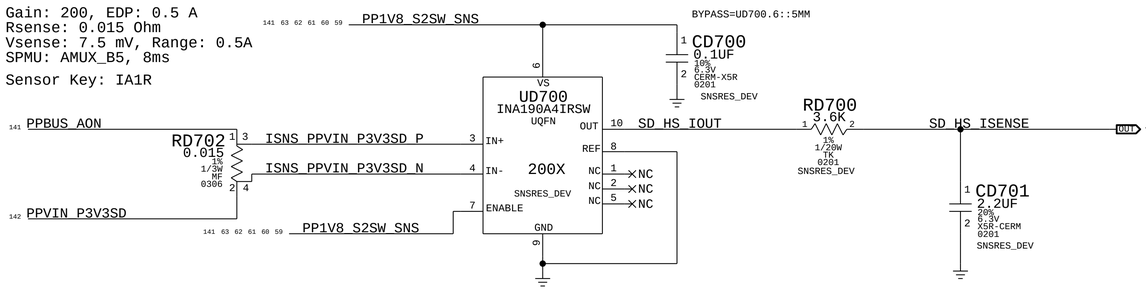
SD PBUS ISENSE

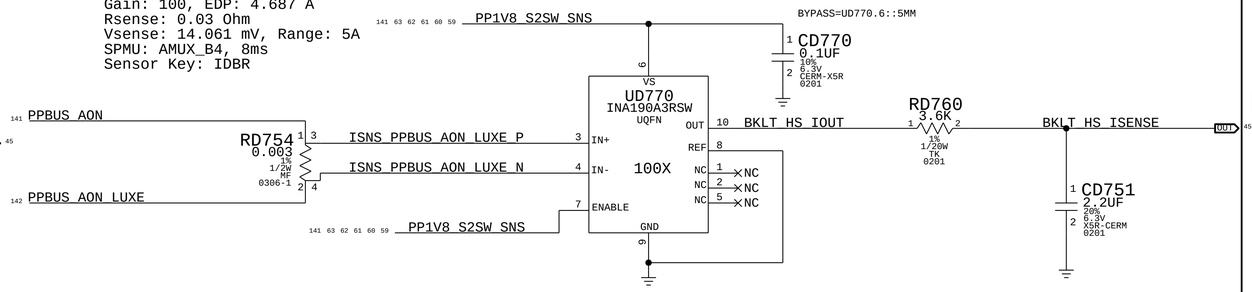
Gain: 200, EDP: 0.5 A
Rsense: 0.015 Ohm
Vsense: 7.5 mV, Range: 0.5A
SPMU: AMUX_B5, 8ms

Sensor Key: IA1R



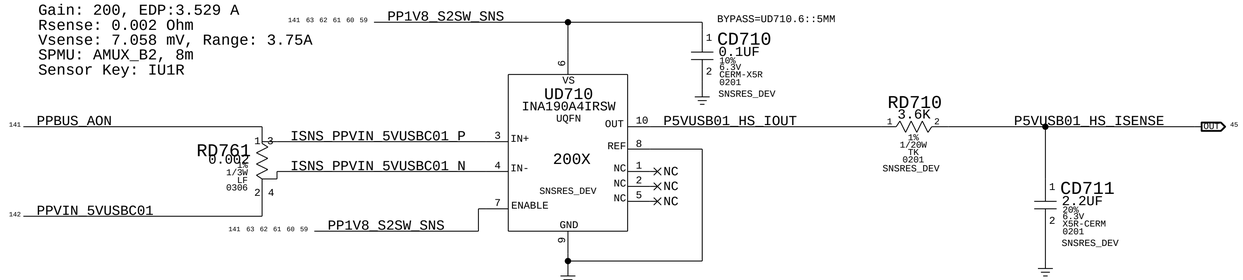
LCD BKLT (LUXE) ISENSE

Gain: 100, EDP: 4.687 A
Rsense: 0.03 Ohm
Vsense: 14.061 mV, Range: 5A
SPMU: AMUX_B4, 8ms
Sensor Key: IDBR



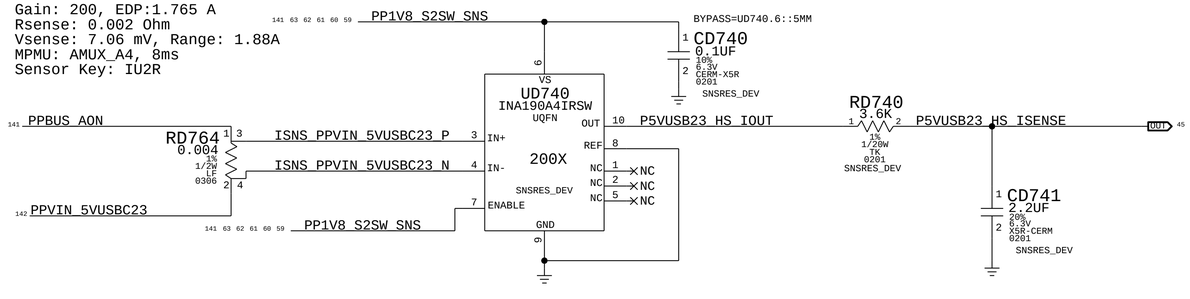
USB 5V OUT LEFT ISENSE

Gain: 200, EDP:3.529 A
Rsense: 0.002 Ohm
Vsense: 7.058 mV, Range: 3.75A
SPMU: AMUX_B2, 8m
Sensor Key: IU1R



USB 5V OUT RIGHT ISENSE

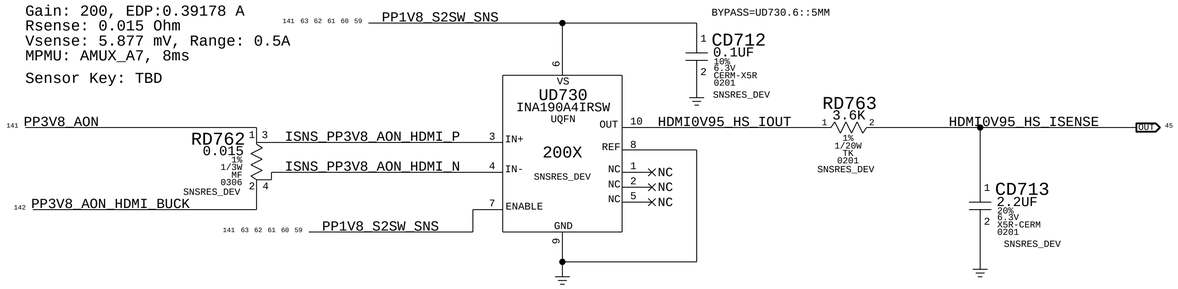
Gain: 200, EDP:1.765 A
Rsense: 0.002 Ohm
Vsense: 7.06 mV, Range: 1.88A
MPMU: AMUX_A4, 8ms
Sensor Key: IU2R



HDMI 3V8 ISENSE

Gain: 200, EDP:0.39178 A
Rsense: 0.015 Ohm
Vsense: 5.877 mV, Range: 0.5A
MPMU: AMUX_A7, 8ms

Sensor Key: TBD



SYNC_MASTER=J416_JAMES_PENG_MLB_C_1.0.1 SYNC_DATE=10/26/2021
PAGE TITLE: SENSORS: HIGH-SIDE(3/3)
Apple Inc.
DRAWING NUMBER: 051-08156
SIZE: D
REVISION: 3.0.0
BRANCH: evt-1
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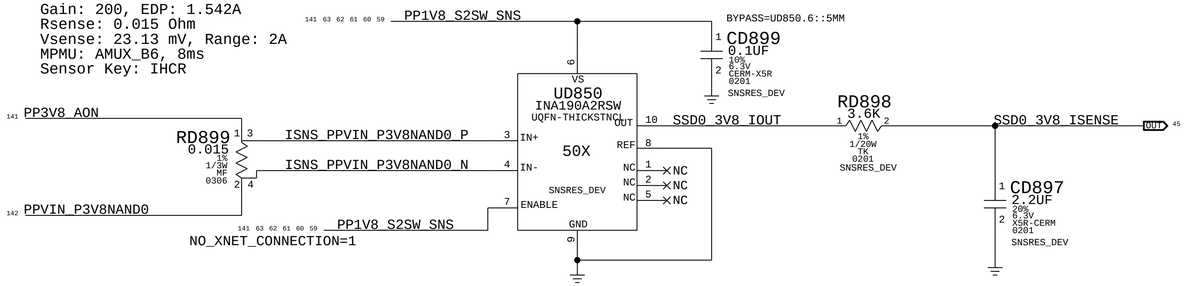
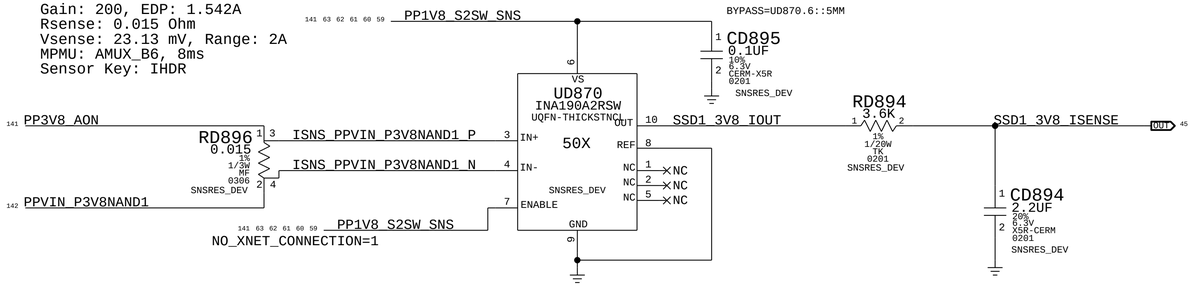
OCARINA 0 ISENSE

Gain: 200, EDP: 1.542A
Rsense: 0.015 Ohm
Vsense: 23.13 mV, Range: 2A
MPMU: AMUX_B6, 8ms
Sensor Key: IHCR



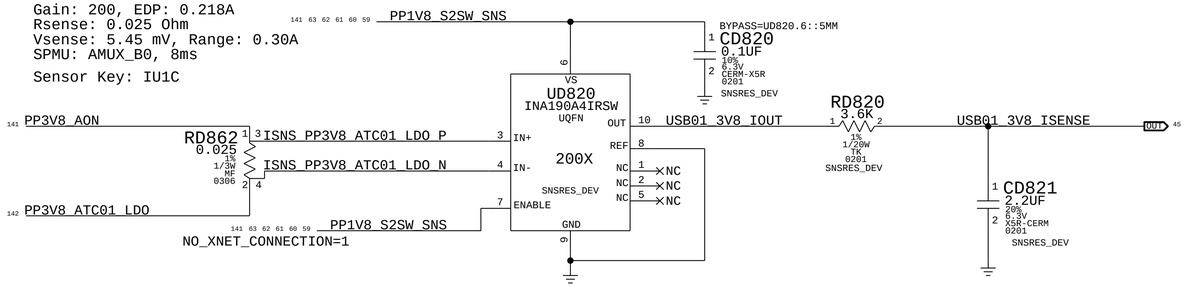
OCARINA 1 ISENSE

Gain: 200, EDP: 1.542A
Rsense: 0.015 Ohm
Vsense: 23.13 mV, Range: 2A
MPMU: AMUX_B6, 8ms
Sensor Key: IHDR



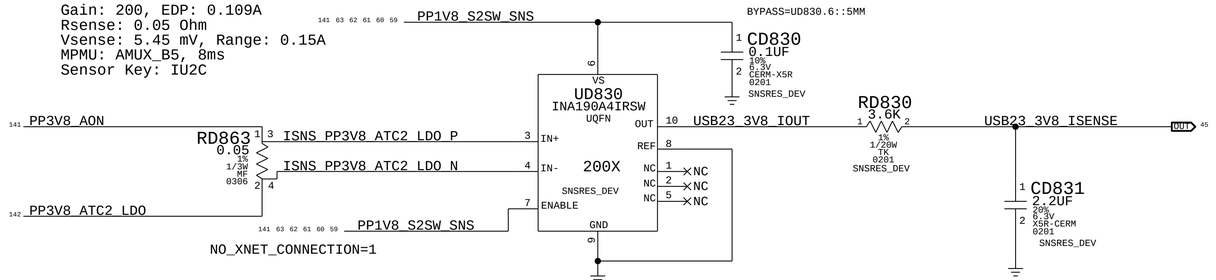
USB 3V8 LEFT ISENSE

Gain: 200, EDP: 0.218A
Rsense: 0.025 Ohm
Vsense: 5.45 mV, Range: 0.30A
SPMU: AMUX_B0, 8ms
Sensor Key: IU1C



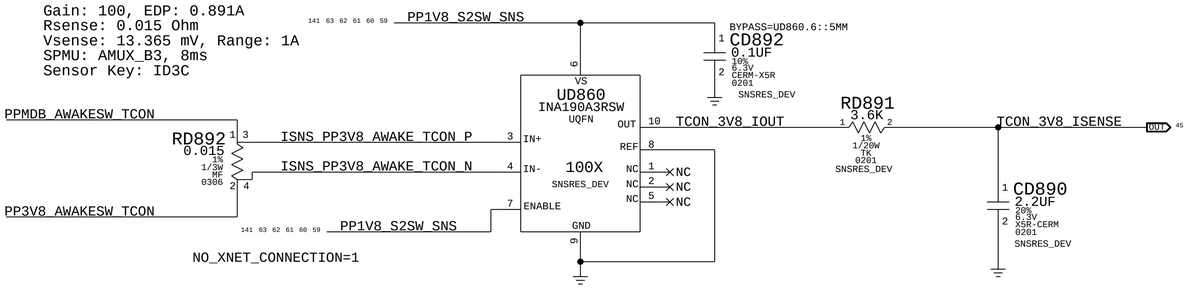
USB 3V8 RIGHT ISENSE

Gain: 200, EDP: 0.109A
Rsense: 0.05 Ohm
Vsense: 5.45 mV, Range: 0.15A
MPMU: AMUX_B5, 8ms
Sensor Key: IU2C



DISPLAY (TCON) 3V8 ISENSE

Gain: 100, EDP: 0.891A
Rsense: 0.015 Ohm
Vsense: 13.365 mV, Range: 1A
SPMU: AMUX_B3, 8ms
Sensor Key: ID3C



BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: LOW-SIDE (1/3)

Apple Inc.

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REVISION 3.0.0
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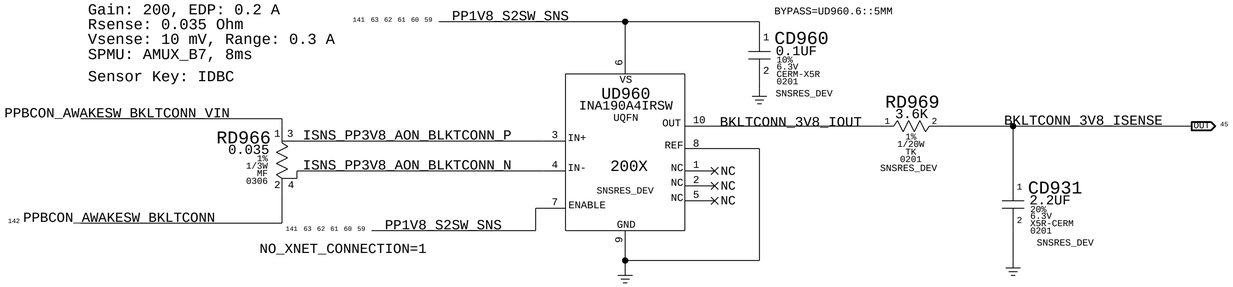
DISPLAY BACKLIGHT 3V8 ISENSE

Gain: 200, EDP: 0.2 A
Rsense: 0.035 Ohm
Vsense: 10 mV, Range: 0.3 A
SPMU: AMUX_B7, 8ms

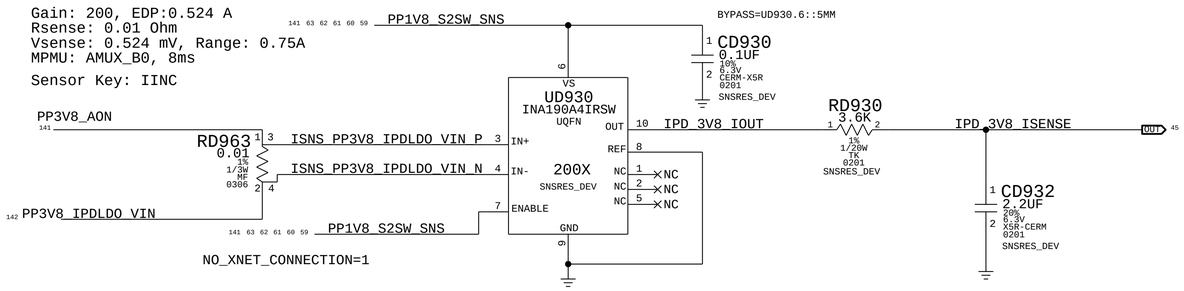
Sensor Key: IDBC



IPD 3V8 ISENSE

Gain: 200, EDP:0.524 A
Rsense: 0.01 Ohm
Vsense: 0.524 mV, Range: 0.75A
MPMU: AMUX_B0, 8ms

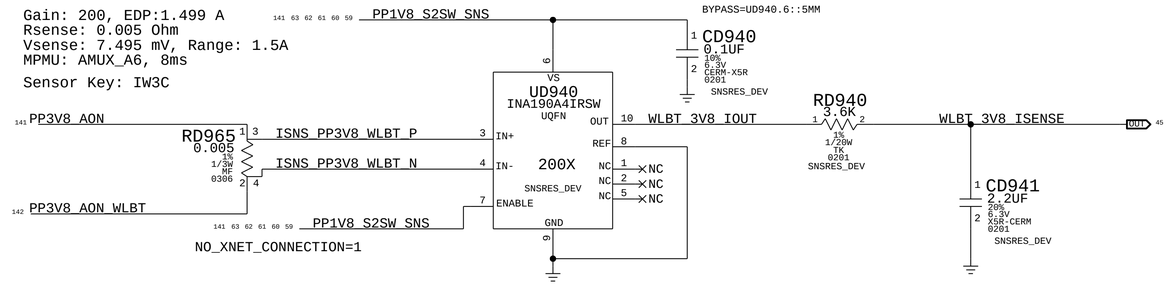
Sensor Key: IINC



WLAN BT 3V8 ISENSE

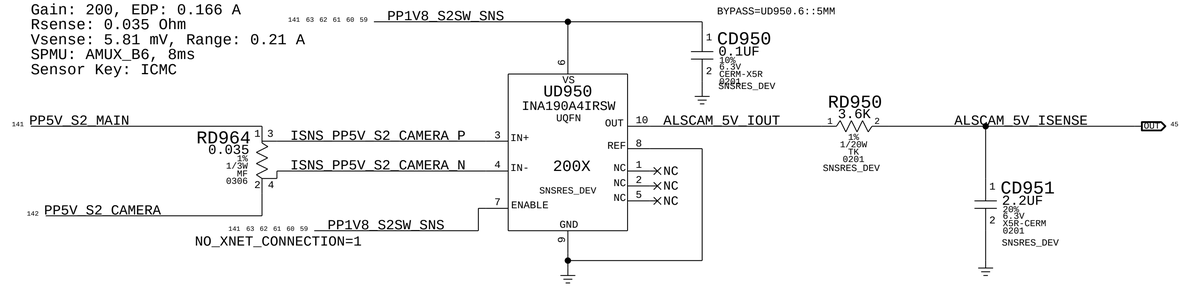
Gain: 200, EDP:1.499 A
Rsense: 0.005 Ohm
Vsense: 7.495 mV, Range: 1.5A
MPMU: AMUX_A6, 8ms

Sensor Key: IW3C



CAMERA 5V ISENSE

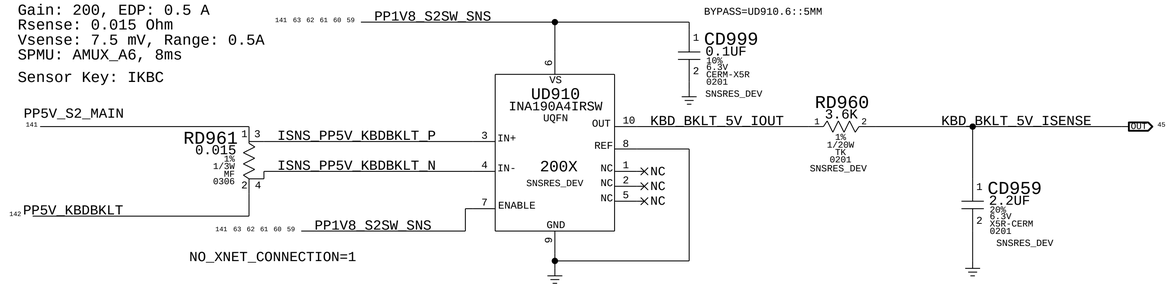
Gain: 200, EDP: 0.166 A
Rsense: 0.035 Ohm
Vsense: 5.81 mV, Range: 0.21 A
SPMU: AMUX_B6, 8ms
Sensor Key: ICMC



KBD BACKLIGHT ISENSE

Gain: 200, EDP: 0.5 A
Rsense: 0.015 Ohm
Vsense: 7.5 mV, Range: 0.5A
SPMU: AMUX_A6, 8ms

Sensor Key: IKBC



BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: LOW-SIDE (2/3)

Apple Inc.

DRAWING NUMBER: 051-08156
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BRANCH: evt-1
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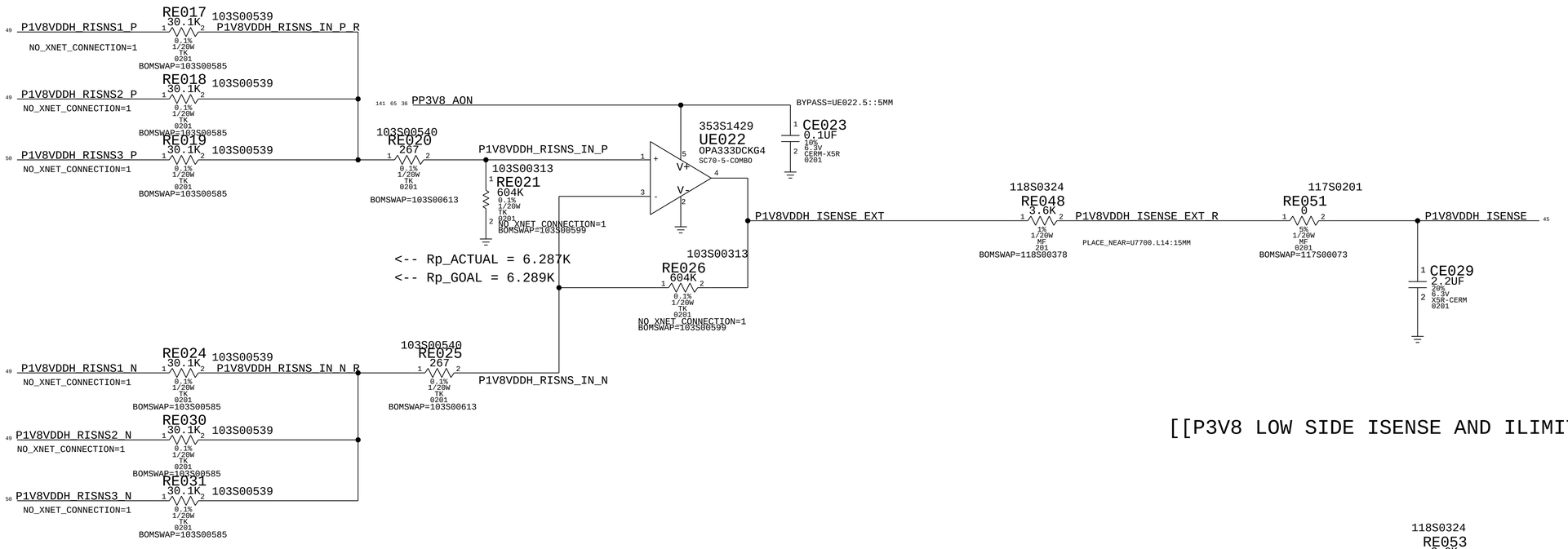
P1V8VDDH LOW SIDE ISENSE (SUMMING AMP FOR 3 PHASES)

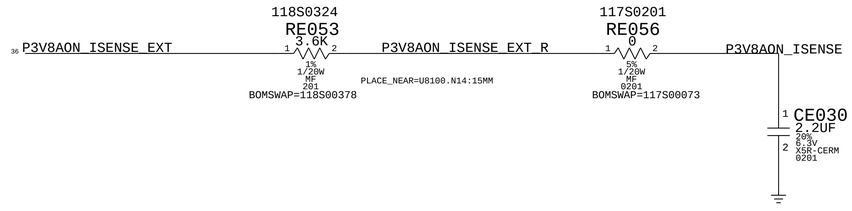
EDP: 156.2A, 32.24A/PHASE

SPMU AMUX_A7, 8ms



[[P3V8 LOW SIDE ISENSE AND ILIMIT moved to CSA140]]

SPMU AMUX_A7, 8ms



BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: LOW-SIDE (3/3)

Apple Inc.

DRAWING NUMBER: 051-08156 | SIZE: D

REVISION: 3.0.0

BRANCH: evt-1

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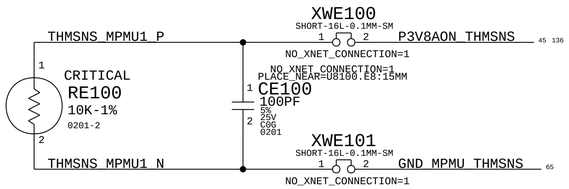
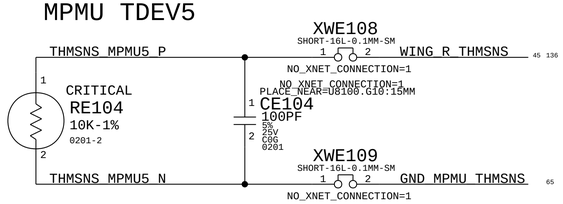
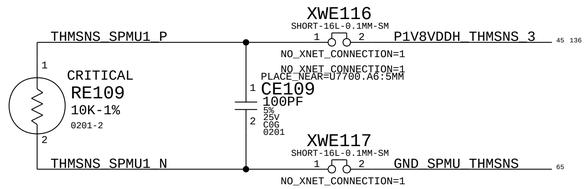
MPMU TDEV1



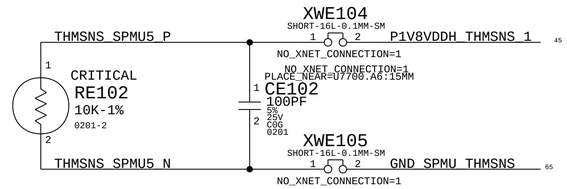
MPMU TDEV5



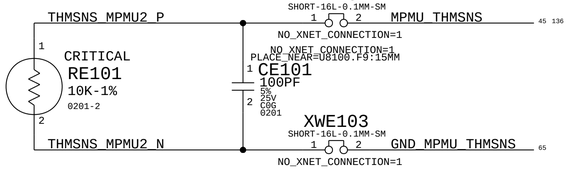
SPMU TDEV1



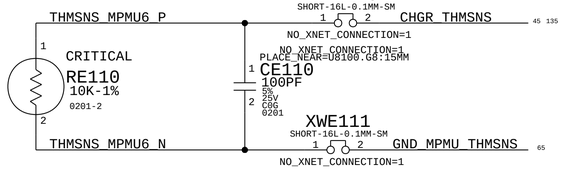
SPMU TDEV5



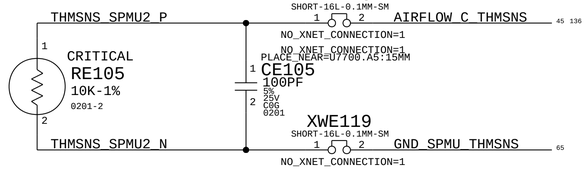
MPMU TDEV2



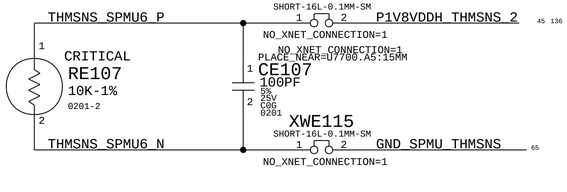
MPMU TDEV6



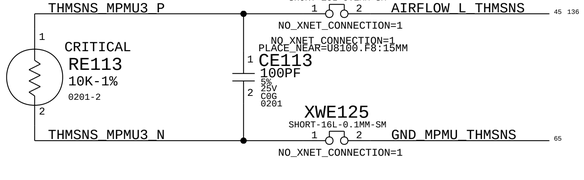
SPMU TDEV2



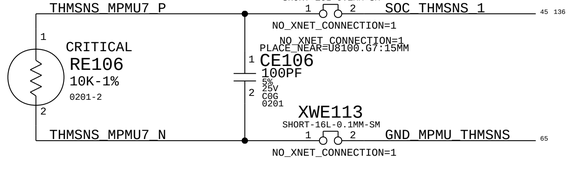
SPMU TDEV6



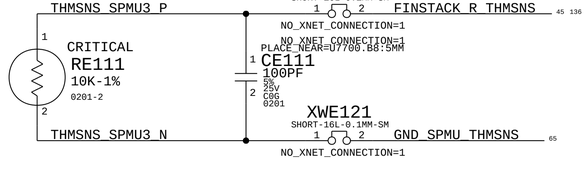
MPMU TDEV3



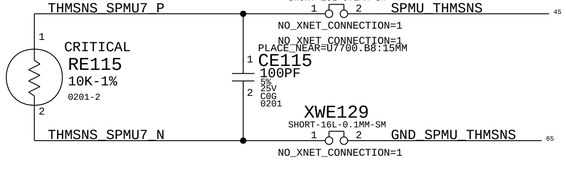
MPMU TDEV7



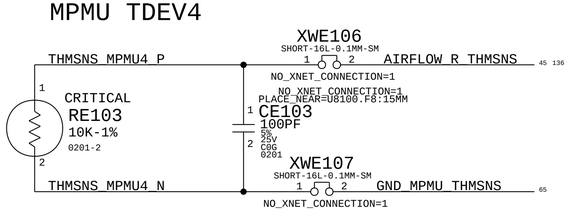
SPMU TDEV3



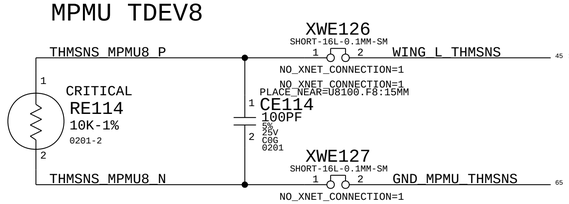
SPMU TDEV7



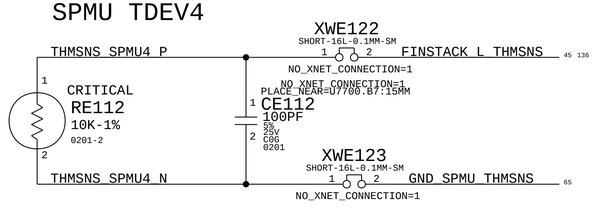
MPMU TDEV4



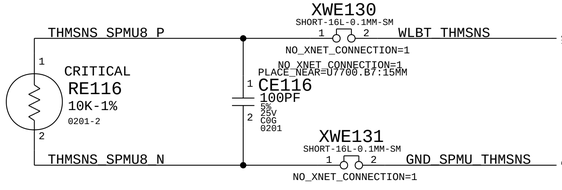
MPMU TDEV8



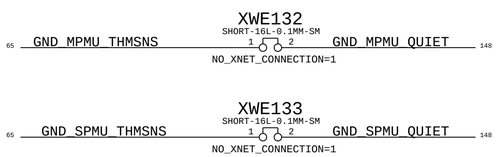
SPMU TDEV4



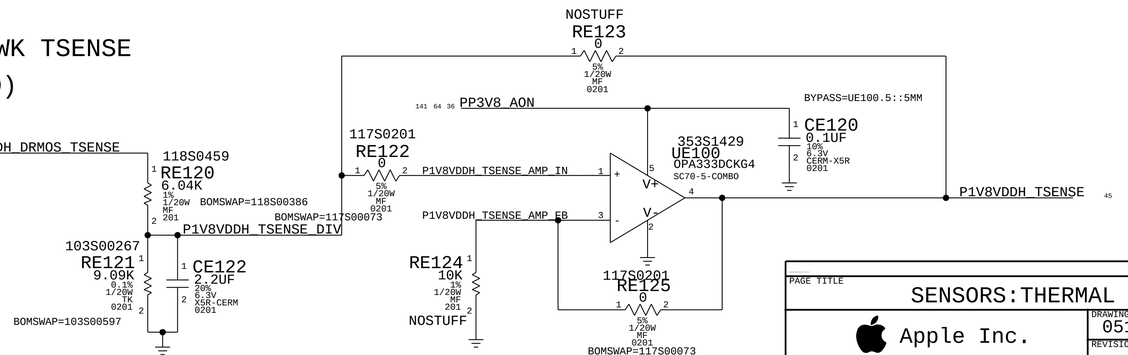
SPMU TDEV8



MPMU AND SPMU ANALOG GROUND CONNECTION



VIPER/SKYHAWK TSENSE
(VALUES TBD)



BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS:THERMAL

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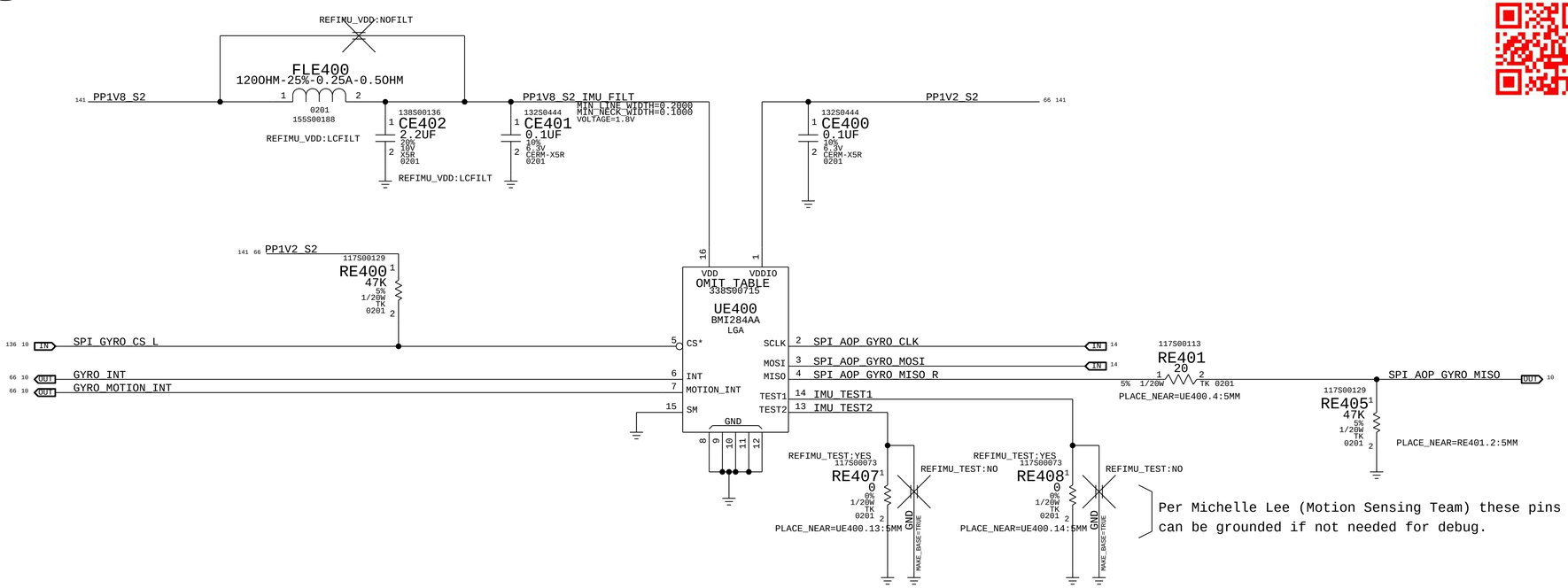
*** OK2INTEGRATE ***

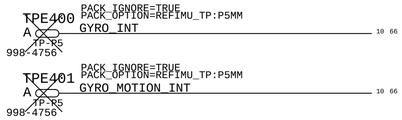
A Sovereign Accelerometer and Gyroscope

Datasheet Radar:



MFG: Bosch
MPN: BMI284AA
APN: 338S00715
URL: https://www.bosch-sensortec.com/products/motion-sensors/imus/
Radar: rdar://61521702 (Sovereign: Datasheet)

B Test Points



C Sovereign BOM Options

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00715	1	IC,SOVEREIGN,BMI284,AA,LGA16	UE400	CRITICAL	REFIMU_IC:BMI284
338S00849	1	IC,SOVEREIGN2,BMI286,AA,LGA16	UE400	CRITICAL	REFIMU_IC:BMI286

BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: MOTION

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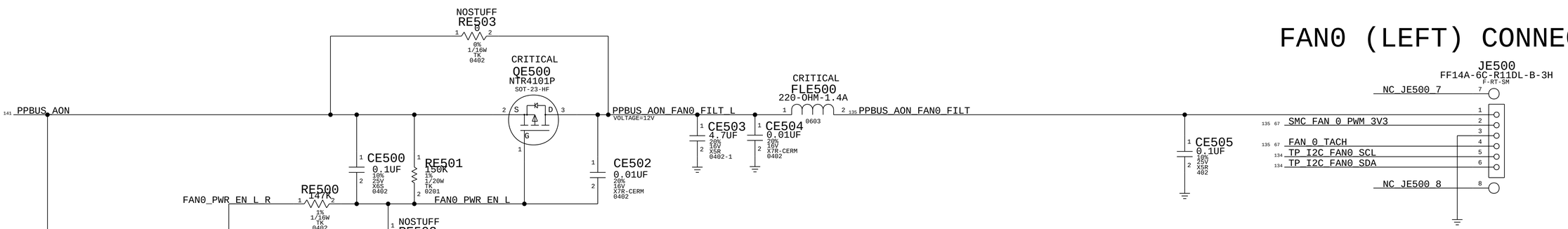
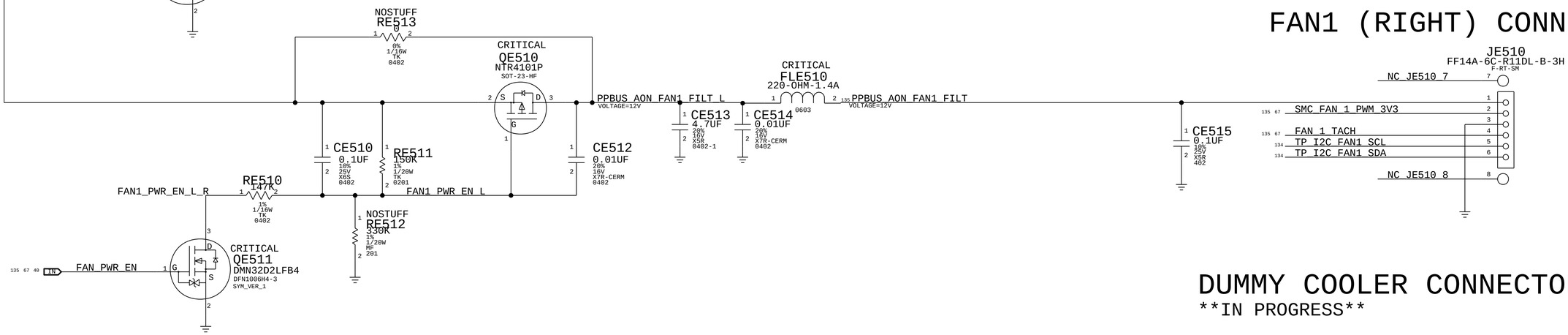
FAN0 (LEFT) CONNECTOR

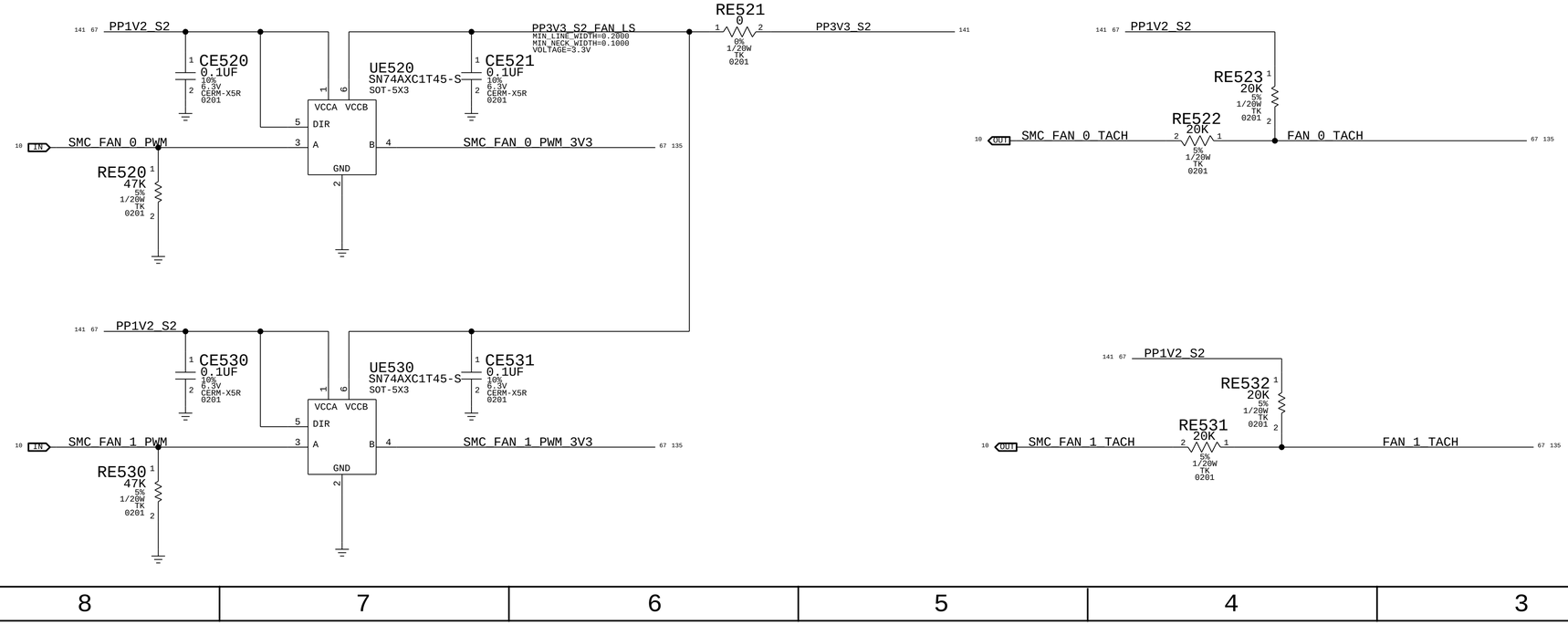


FAN1 (RIGHT) CONNECTOR



DUMMY COOLER CONNECTOR

IN PROGRESS



PAGE TITLE

FANS

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Left Side Port

PLACE VBUS CAP NEAR EACH VBUS PIN

PPVBUS_USBC0
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=20V

PLACE_NEAR=JE700.30:5MM

ALLOW_APPLE_PREFIX=D

DE722
TVS2200
WSON
4 IN
5 IN
6 IN
GND 1
GND 2
GND 3
EPAD 7

516S00686
PACK_IGNORE=TRUE
JE700
20875-028E-01
F-ST-SMM
PACK_OPTION=NOT_FLIPPED

29	PWR		30
1	TP_USBC0_PP20V		2
3	USBC0_D2R_CR_N<1>	USBC0_SBU2	4
5	USBC0_D2R_CR_P<1>	USBC0_CC1_CONN	6
7		USBC0_USB_BOT_N	8
9	USBC0_R2D_N<1>	USBC0_USB_BOT_P	10
11	USBC0_R2D_P<1>	USBC0_SBU1	12
13		USBC0_CC2_CONN	14
15	USBC0_USB_TOP_P	USBC0_R2D_N<2>	16
17	USBC0_USB_TOP_N	USBC0_R2D_P<2>	18
19			20
21			22
23	USBC0_D2R_CR_N<2>		24
25	USBC0_D2R_CR_P<2>		26
27			28
31	PWR		32
33			34
35			36
37			38
39			40
41			42
43			44
45			46
47			48
49			50

516S00686
PACK_IGNORE=TRUE
JE701
20875-028E-01
F-ST-SMM
PACK_OPTION=NOT_FLIPPED

29	PWR		30
1	TP_USBC1_PP20V		2
3	USBC1_D2R_CR_N<1>	USBC1_SBU2	4
5	USBC1_D2R_CR_P<1>	USBC1_CC1_CONN	6
7		USBC1_USB_BOT_N	8
9	USBC1_R2D_N<1>	USBC1_USB_BOT_P	10
11	USBC1_R2D_P<1>	USBC1_SBU1	12
13		USBC1_CC2_CONN	14
15	USBC1_USB_TOP_P	USBC1_R2D_N<2>	16
17	USBC1_USB_TOP_N	USBC1_R2D_P<2>	18
19			20
21			22
23	USBC1_D2R_CR_N<2>		24
25	USBC1_D2R_CR_P<2>		26
27			28
31	PWR		32
33			34
35			36
37			38
39			40
41			42
43			44
45			46
47			48
49			50

PLACE VBUS CAP NEAR EACH VBUS PIN

PPVBUS_USBC1
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=20V

PLACE_NEAR=JE701.30:5MM

ALLOW_APPLE_PREFIX=D

DE702
TVS2200
WSON
4 IN
5 IN
6 IN
GND 1
GND 2
GND 3
EPAD 7

BOM_COST_GROUP=USB-C

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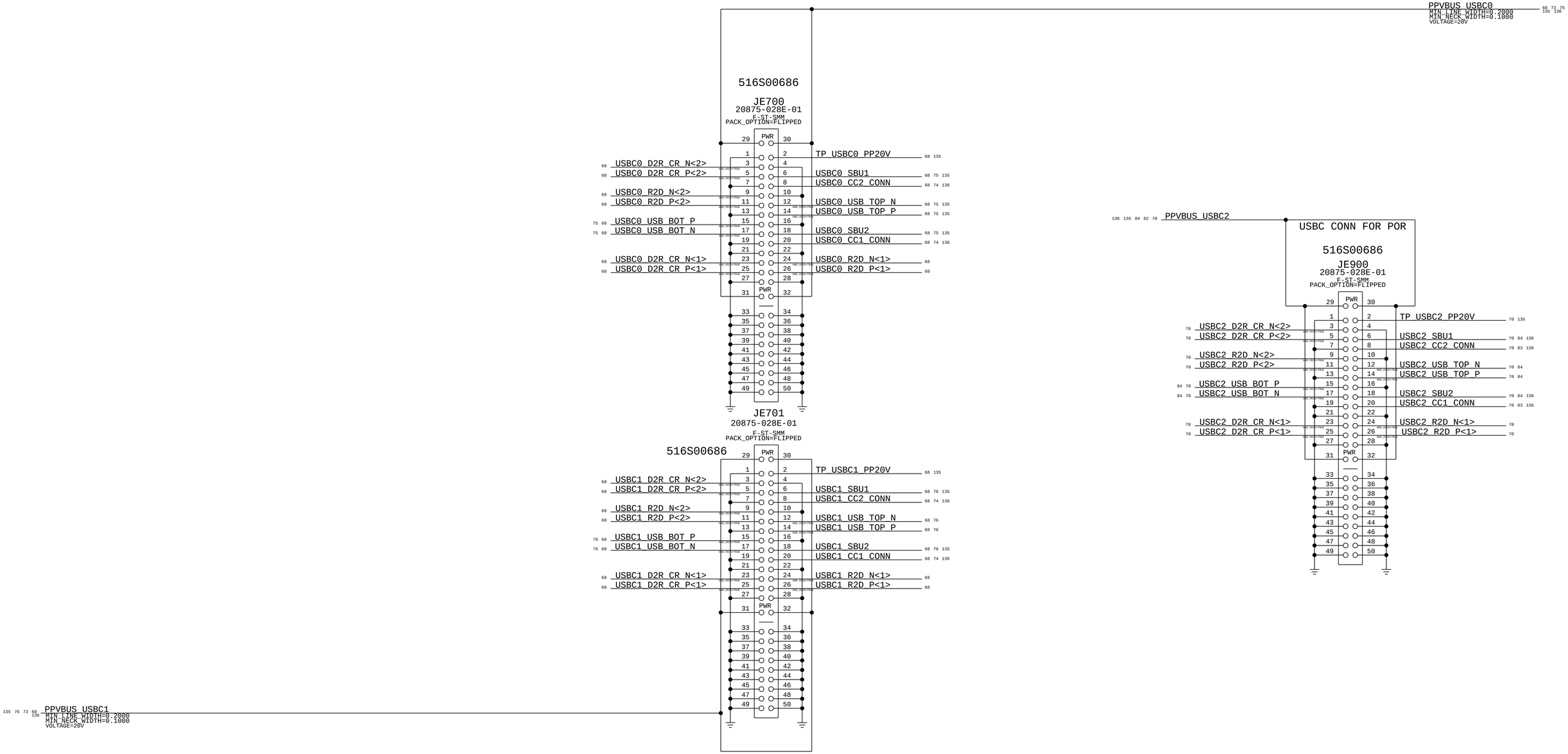
Flipped Top/Bottom Connections

To use reversed top/bottom connections,
Specify PACK_OPTION=FLIPPED and include CSA148



PAGE TITLE
USB-C: Alt Flipped Connector(s)

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*** FOR REFERENCE ONLY ***

Right Side Port

PPVBUS_USBC2
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=20V

PLACE_NEAR=JE900.30:5MM

ALLOW_APPLE_PREFIX=D

DE922
TVS2200
WSON

USBC CONN FOR POR

516S00686
PACK_IGNORE=TRUE
JE900
20875-028E-01
F-ST-SMM
PACK_OPTION=NOT_FLIPPED

PLACE VBUS CAP NEAR EACH VBUS PIN

CRITICAL CE920 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CE921 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CE922 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CE923 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CE926 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CE927 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CE928 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CE925 0.01UF 10% 25V X5R-CERM 0201

RE961 2 USBC2_R2D_C_N<1>
RE960 2 USBC2_R2D_C_P<1>
RE963 2 USBC2_D2R_R_N<1>
RE962 2 USBC2_D2R_R_P<1>
5% 1/20W TK 0201

CE961 0.22UF X5R 10% 25V 0201
CE960 0.22UF X5R 10% 25V 0201
CE963 0.33UF CER-X5R 10% 25V 0201
CE962 0.33UF CER-X5R 10% 25V 0201

RE965 RE964 RE967 RE966 51K 5% 1/20W TK 0201

DZE962 DZE963 DZE960 DZE961 DZE964 DZE965 DZE967 DZE966 CRITICAL ESD120-1BF4 0201-TH1CKSTNCL

RE996 RE997 RE994 RE995 51K 5% 1/20W TK 0201

CE991 0.22UF X5R 10% 25V 0201
CE990 0.22UF X5R 10% 25V 0201
CE993 0.33UF CER-X5R 10% 25V 0201
CE992 0.33UF CER-X5R 10% 25V 0201

RE991 RE990 RE993 RE992 5% 1/20W TK 0201

DZE996 DZE997 DZE994 DZE995 DZE991 DZE990 DZE993 DZE992 CRITICAL ESD120-1BF4 0201-TH1CKSTNCL

BOM_COST_GROUP=USB-C

PAGE TITLE	USB-C: Connector(s)
	Apple Inc.
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*** OK2INTEGRATE ***

No lane swapping is allowed
Re-timer to SOC connections are set

Re-timer to connector connections are set

USBC HIGH-SPEED AC COUPLING

9 IN	USBC_ATC0_R2D_C_P<1>	CF020 0.22UF	USBC_ATC0_R2D_P<1>	71
9 IN	USBC_ATC0_R2D_C_N<1>	CF021 0.22UF	USBC_ATC0_R2D_N<1>	71
9 IN	USBC_ATC0_R2D_C_P<2>	CF024 0.22UF	USBC_ATC0_R2D_P<2>	71
9 IN	USBC_ATC0_R2D_C_N<2>	CF025 0.22UF	USBC_ATC0_R2D_N<2>	71
9 BI	USBC_ATC0_D2R_P<1>	CF022 0.22UF	USBC_ATC0_D2R_C_P<1>	71
9 BI	USBC_ATC0_D2R_N<1>	CF023 0.22UF	USBC_ATC0_D2R_C_N<1>	71
9 BI	USBC_ATC0_D2R_P<2>	CF026 0.22UF	USBC_ATC0_D2R_C_P<2>	71
9 BI	USBC_ATC0_D2R_N<2>	CF027 0.22UF	USBC_ATC0_D2R_C_N<2>	71

All: GND_VOID=TRUE; 0201, 6.3V, 20%, X5R

PP1V2_ATCRTMR01_VDDIO 71 74 141 — RF045 47K 5% 1/20W TK 0201 — ATCRTMR0_JTAG_TDO 71

ATCRTMR0_XTAL24M_OUT 71 — RF060 499 1% 1/20W TK 0201 — ATCRTMR0_XTAL24M_IN 71

CRITICAL YF000 197S0591 24.000MHZ-20PPM-9.5PF-60OHM 1.60X1.20MM — ATC0_24M_O_R

CRITICAL CF060 15PF 5% 50V C0G 0201

CRITICAL CF061 15PF 5% 50V C0G 0201

PP0V855_ATCRTMR01_VDD_CIO 141 — CF030 14UF 20% 4V X5R 0402-D2X-1 138S00149 — CF031 14UF 20% 4V X5R 0402-D2X-1

CF032 0.1UF 10% 6.3V X6S 0201 — CF033 0.1UF 10% 6.3V X6S 0201

PP1V2_ATCRTMR01_VDDIO 71 74 141 — CF034 0.1UF 10% 6.3V X6S 0201 — CF035 2.2UF 20% 4V X6S-CERM 0201 — CF036 14UF 20% 4V X5R 0402-D2X-1 — CF037 14UF 20% 4V X5R 0402-D2X-1

PP0V805_ATCRTMR01_VDD_FIXED 141 71 — CF040 0.1UF 10% 6.3V X6S 0201 — CF041 0.1UF 10% 6.3V X6S 0201 — CF042 2.2UF 20% 4V X6S-CERM 0201 — CF043 2.2UF 20% 4V X6S-CERM 0201 — CF044 2.2UF 20% 4V X6S-CERM 0201

CF045 14UF 20% 4V X5R 0402-D2X-1 — CF046 14UF 20% 4V X5R 0402-D2X-1

PP0V805_ATCRTMR01_VDD_FIXED 141 71 — CF050 0.1UF 10% 6.3V X6S 0201 — PLACE_NEAR=UF000.G7:5MM

VDD_FIXED_XTAL_ATC0_F

PP0V805_ATCRTMR01_VDD_FIXED 141 — RF051 10 5% 1/20W TK 0201 — VOLTAGE=0.805V — CF051 4UF 20% 2.5V X6S 0201 — 117S00094 — 138S00129

UF000 TMNB25B0-C1 FCCSP
OMIT_TABLE CRITICAL SYM 2 OF 2

J4	VDD_CIO_0	VDDIO12_CIO_0	K5
J6	VDD_CIO_0	VDDIO12_CIO_0	K7
J8	VDD_CIO_0	VDDIO12_CIO_0	L6
F4	VDD_CIO_1	VDDIO12_CIO_1	D6
F6	VDD_CIO_1	VDDIO12_CIO_1	E5
F8	VDD_CIO_1	VDDIO12_CIO_1	E7
G4	VDD_FIXED	VDDIO12_PLL_SOC0	K8
G5	VDD_FIXED	VDDIO12_PLL_SOC1	H8
H5	VDD_FIXED	VDDIO12_XTAL	H9
H6	VDD_FIXED	VDDIO12	E9
G7	VDD_FIXED_PLL	VDDIO12	H3
G9	VDD_FIXED_XTAL	VDDIO12	K9
		VDDIO12_EFUSE1	F3
		VDDIO12_AMUX	F7
A1, A2, A4, A6, A8, A10, A11, B2, B4, B6, B8, B10, C3, C5, C6, C7, C9, D1, D5, D7, D11, E3, E4, E6, E8, F2, F5, F10, G3, G6, G8	VSS	H4, H7, J2, J3, J5, J7, J10, K4, K6, L1, L5, L7, L11, M3, M5, M6, M7, M9, N2, N4, N6, N8, N10, P1, P2, P4, P6, P8, P10, P11	VSS

PP1V2_ATCRTMR01_VDDIO 141 — CF052 2.2UF 20% 4V X6S-CERM 0201 — PLACE_NEAR=UF000.K8:5MM

PP1V2_ATCRTMR0_VDDIO_XTAL_F — VOLTAGE=1.2V — 155S0644 FLF000 240-OHM-0.2A-0.9-OHM 0201 — PP1V2_ATCRTMR01_VDDIO 141

CF062 0.1UF 10% 6.3V X6S 0201 — CF063 2.2UF 20% 4V X6S-CERM 0201

GND 141 — Connect to GND directly or via a resistor

PP1V2_ATCRTMR01_VDDIO 141 — CF064 0.1UF 10% 6.3V X6S 0201

ATCRTMR0_CFP_RCAL_NEG 71 — CF011 10PF 5% 25V C0G 0201 — RF011 200 1% 1/20W TK 0201-1 — ATCRTMR0_CFP_RCAL_POS 71

ATCRTMR0_SFP_RCAL_NEG 71 — CF010 10PF 5% 25V C0G 0201 — RF010 200 1% 1/20W TK 0201-1 — ATCRTMR0_SFP_RCAL_POS 71

UF000 TMNB25B0-C1 FCCSP
OMIT_TABLE CRITICAL 998-25504 SYM 1 OF 2

71	USBC_ATC0_D2R_C_P<1>	P9	SFP_PHY_RXTX_0_P	SFP PHY	CFP PHY	CFP_PHY_RXTX_0_P A9 USBC0_R2D_CR_P<1> OUT 68
71	USBC_ATC0_D2R_C_N<1>	N9	SFP_PHY_RXTX_0_N			CFP_PHY_RXTX_0_N B9 USBC0_R2D_CR_N<1> OUT 68
71	USBC_ATC0_D2R_C_P<2>	P5	SFP_PHY_RXTX_2_P			CFP_PHY_RXTX_2_P A5 USBC0_R2D_CR_P<2> OUT 68
71	USBC_ATC0_D2R_C_N<2>	N5	SFP_PHY_RXTX_2_N			CFP_PHY_RXTX_2_N B5 USBC0_R2D_CR_N<2> OUT 68
71	USBC_ATC0_R2D_P<1>	P7	SFP_PHY_RXTX_1_P			CFP_PHY_RXTX_1_P A7 USBC0_D2R_P<1> BI 68
71	USBC_ATC0_R2D_N<1>	N7	SFP_PHY_RXTX_1_N			CFP_PHY_RXTX_1_N B7 USBC0_D2R_N<1> BI 68
71	USBC_ATC0_R2D_P<2>	P3	SFP_PHY_RXTX_3_P			CFP_PHY_RXTX_3_P A3 USBC0_D2R_P<2> BI 68
71	USBC_ATC0_R2D_N<2>	N3	SFP_PHY_RXTX_3_N			CFP_PHY_RXTX_3_N B3 USBC0_D2R_N<2> BI 68
73 BI	USBC_ATC0_AUX_C_P	L4	SFP_LPDP_AUX_P			CFP_LPDP_AUX_P D4 USBC0_AUX_P BI 73
73 BI	USBC_ATC0_AUX_C_N	M4	SFP_LPDP_AUX_N			CFP_LPDP_AUX_N C4 USBC0_AUX_N IN 73
89 71 IN	CIO_ATC0_LSTX	G1	USB4_SFP_SB_RX			USB4_CFP_SB_RX F1 USBC0_CIO_LSRX IN 78
89 71 OUT	CIO_ATC0_LSRX	G2	USB4_SFP_SB_TX			USB4_CFP_SB_TX E1 USBC0_CIO_LSTX BI 78
						USB4_CFP_SB_TX_DIR H1 ATCRTMR0_LSTX_DIR OUT 78
71	ATCRTMR0_SFP_RCAL_POS	M8	SFP_PHY_RCAL_P			CFP_PHY_RCAL_P C8 ATCRTMR0_CFP_RCAL_POS 71
71	ATCRTMR0_SFP_RCAL_NEG	L8	SFP_PHY_RCAL_N			CFP_PHY_RCAL_N D8 ATCRTMR0_CFP_RCAL_NEG 71
74 IN	ATCRTMR0_CHIPID_0	M1	CHIP_ID_0	GPIO	PERIPHERAL	QSPI_CS* N11 SPI_ATCRTMR0_CS_L 71
74 IN	ATCRTMR0_CHIPID_1	N1	CHIP_ID_1			QSPI_SCLK M11 SPI_ATCRTMR0_CLK 71
74 IN	ATCRTMR0_BOOT_CONFIG0	H2	BOOT_CONFIG0			QSPI_DQ0 K10 SPI_ATCRTMR0_DIO<0> 71
74 IN	ATCRTMR0_BOOT_CONFIG1	J1	BOOT_CONFIG1			QSPI_DQ1 K11 SPI_ATCRTMR0_DIO<1> 71
74 IN	ATCRTMR0_BOOT_CONFIG2	K1	BOOT_CONFIG2			QSPI_DQ2 J9 SPI_ATCRTMR0_DIO<2> 71
75 73 IN	ATCRTMR0_FORCE_DFU	C1	FORCE_DFU			QSPI_DQ3 J11 SPI_ATCRTMR0_DIO<3> 71
	TP_ATCRTMR0_GPIO0	K2	GPIO0			I2C0_SCL C2 I2C_ATCRTMR_SCL IN 148
	NC_ATCRTMR0_GPIO1 NO_TEST=1	L3	GPIO1			I2C0_SDA D3 I2C_ATCRTMR_SDA BI 148
	TP_ATCRTMR0_GPIO2	K3	GPIO2			I2C1_SCL E2 I2C_UPC0_ATCRTMR0_SCL_1V2 IN 89
	TP_ATCRTMR0_GPIO3	L10	GPIO3			I2C1_SDA D2 I2C_UPC0_ATCRTMR0_SDA_1V2 BI 89
						I2C1_INT B1 INT_I2C_UPC0_ATCRTMR0_L OUT 73 75
74 IN	ATCRTMR0_COLD_RESET_L	L2	COLD_RESET*	CLOCKS AND RESET	TEST AND DEBUG	TESTMODE L9 ATCRTMR0_TESTMODE 71
74 IN	ATCRTMR0_CFSB	M2	CFSB			JTAG_SEL C11 ATCRTMR0_JTAGL_SEL 71
71	ATCRTMR0_XTAL24M_IN	F11	XI0			JTAG_TCK B11 SWD_NUB_ATCRTMR0_SWCLK BI 148
71	ATCRTMR0_XTAL24M_OUT	E11	XO0			JTAG_TMS D10 SWD_NUB_ATCRTMR0_SWDIO BI 148
						JTAG_TDI D9 TP_ATCRTMR0_JTAG_TDI
						JTAG_TDO C10 ATCRTMR0_JTAG_TDO 71
						JTAG_TRST* E10 TP_ATCRTMR0_JTAG_TRESET
						ANALOGMUX_OUT F9 TP_ATCRTMR0_ANALOGMUX_OUT
						TST_CLKOUT M10 TP_ATCRTMR0_TST_CLKOUT
						TST_CLK_LVDS_0_P H10 NC_ATCRTMR0_CLK_LVDS_P<0> NO_TEST=1
						TST_CLK_LVDS_0_N H11 NC_ATCRTMR0_CLK_LVDS_N<0> NO_TEST=1
						TST_CLK_LVDS_1_P G11 NC_ATCRTMR0_CLK_LVDS_P<1> NO_TEST=1
						TST_CLK_LVDS_1_N G10 NC_ATCRTMR0_CLK_LVDS_N<1> NO_TEST=1

SPI_ATCRTMR0_DIO<0> 71 — RF097 33 1/20W 5% TK 0201 — SPI_ATCRTMR0_R_DIO<0> 71

SPI_ATCRTMR0_DIO<1> 71 — RF098 33 1/20W 5% TK 0201 — SPI_ATCRTMR0_R_DIO<1> 71

PP1V2_ATCRTMR01_VDDIO 141

RF090 3.3K 5% 1/20W TK 0201

NOSTUFF RF091 3.3K 5% 1/20W TK 0201

NOSTUFF RF092 3.3K 5% 1/20W TK 0201

NOSTUFF RF093 3.3K 5% 1/20W TK 0201

CF090 1UF 10% 6.3V CERM 402

OMIT_TABLE CRITICAL 998-22093
UF090 64MBIT-1.2V W25Q64NE XSON

SPI_ATCRTMR0_CLK 71	RF094 33 1/20W 5% TK 0201	SPI_ATCRTMR0_CLK_R	6 CLK
SPI_ATCRTMR0_CS_L 71		SPI_ATCRTMR0_CS_L	1 CS*
SPI_ATCRTMR0_DIO<2> 71	RF095 33 1/20W 5% TK 0201	SPI_ATCRTMR0_R_DIO<2>	3 WP*(IO2)
		SPI_ATCRTMR0_R_DIO<3>	7 HOLD*(IO3)
SPI_ATCRTMR0_DIO<3> 71	RF096 33 1/20W 5% TK 0201		

DI(IO0) 5 SPI_ATCRTMR0_R_DIO<0> 71
DO(IO1) 2 SPI_ATCRTMR0_R_DIO<1> 71
GND 4, EPAD 9

RF047 47K 5% 0201 TK 1/20W — ATCRTMR0_JTAGL_SEL 71

RF040 10K 5% 1/20W TK 0201 — ATCRTMR0_TESTMODE 71

RF043 47K 5% 1/20W TK 0201 — CIO_ATC0_LSTX 71 89

RF044 47K 5% 1/20W TK 0201 — CIO_ATC0_LSRX 71 89

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C: High Speed ATC0

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*** OK2INTEGRATE ***

No lane swapping is allowed
Re-timer to SOC connections are set

Re-timer to connector connections are set

USBC HIGH-SPEED AC COUPLING

PP1V2_ATCRTMR01_VDDIO — 47K RF145 5% 1/20W TK 0201 — ATCRTMR1_JTAG_TDO

USBC_ATC1_R2D_C_P<1>	GND_VOID=TRUE	CF120 0.22UF 20% 6.3V X5R 0201		USBC_ATC1_R2D_P<1>	
USBC_ATC1_R2D_C_N<1>	GND_VOID=TRUE	CF121 0.22UF 20% 6.3V X5R 0201		USBC_ATC1_R2D_N<1>	
USBC_ATC1_R2D_C_P<2>	GND_VOID=TRUE	CF124 0.22UF 20% 6.3V X5R 0201		USBC_ATC1_R2D_P<2>	
USBC_ATC1_R2D_C_N<2>	GND_VOID=TRUE	CF125 0.22UF 20% 6.3V X5R 0201		USBC_ATC1_R2D_N<2>	
USBC_ATC1_D2R_P<1>	GND_VOID=TRUE	CF122 0.22UF 20% 6.3V X5R 0201		USBC_ATC1_D2R_C_P<1>	
USBC_ATC1_D2R_N<1>	GND_VOID=TRUE	CF123 0.22UF 20% 6.3V X5R 0201		USBC_ATC1_D2R_C_N<1>	
USBC_ATC1_D2R_P<2>	GND_VOID=TRUE	CF126 0.22UF 20% 6.3V X5R 0201		USBC_ATC1_D2R_C_P<2>	
USBC_ATC1_D2R_N<2>	GND_VOID=TRUE	CF127 0.22UF 20% 6.3V X5R 0201		USBC_ATC1_D2R_C_N<2>	

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OMIT_TABLE CRITICAL 998-25504 SYM 1 OF 2

USBC_ATC1_D2R_C_P<1>	GND_VOID=TRUE	P9	SFP_PHY_RXTX_0_P	SFP PHY	CFP PHY	CFP_PHY_RXTX_0_P	GND_VOID=TRUE	USBC1_R2D_CR_P<1>
USBC_ATC1_D2R_C_N<1>	GND_VOID=TRUE	N9	SFP_PHY_RXTX_0_N			CFP_PHY_RXTX_0_N	GND_VOID=TRUE	USBC1_R2D_CR_N<1>
USBC_ATC1_D2R_C_P<2>	GND_VOID=TRUE	P5	SFP_PHY_RXTX_2_P			CFP_PHY_RXTX_2_P	GND_VOID=TRUE	USBC1_R2D_CR_P<2>
USBC_ATC1_D2R_C_N<2>	GND_VOID=TRUE	N5	SFP_PHY_RXTX_2_N			CFP_PHY_RXTX_2_N	GND_VOID=TRUE	USBC1_R2D_CR_N<2>
USBC_ATC1_R2D_P<1>	GND_VOID=TRUE	P7	SFP_PHY_RXTX_1_P			CFP_PHY_RXTX_1_P	GND_VOID=TRUE	USBC1_D2R_P<1>
USBC_ATC1_R2D_N<1>	GND_VOID=TRUE	N7	SFP_PHY_RXTX_1_N			CFP_PHY_RXTX_1_N	GND_VOID=TRUE	USBC1_D2R_N<1>
USBC_ATC1_R2D_P<2>	GND_VOID=TRUE	P3	SFP_PHY_RXTX_3_P			CFP_PHY_RXTX_3_P	GND_VOID=TRUE	USBC1_D2R_P<2>
USBC_ATC1_R2D_N<2>	GND_VOID=TRUE	N3	SFP_PHY_RXTX_3_N			CFP_PHY_RXTX_3_N	GND_VOID=TRUE	USBC1_D2R_N<2>
USBC_ATC1_AUX_C_P		L4	SFP_LPDP_AUX_P			CFP_LPDP_AUX_P		USBC1_AUX_P
USBC_ATC1_AUX_C_N		M4	SFP_LPDP_AUX_N			CFP_LPDP_AUX_N		USBC1_AUX_N
CIO_ATC1_LSTX		G1	USB4_SFP_SB_RX			USB4_CFP_SB_RX		USBC1_CIO_LSRX
CIO_ATC1_LSRX		G2	USB4_SFP_SB_TX			USB4_CFP_SB_TX		USBC1_CIO_LSTX
						USB4_CFP_SB_TX_DIR		ATCRTMR1_LSTX_DIR
ATCRTMR1_SFP_RCAL_POS		M8	SFP_PHY_RCAL_P			CFP_PHY_RCAL_P		ATCRTMR1_CFP_RCAL_POS
ATCRTMR1_SFP_RCAL_NEG		L8	SFP_PHY_RCAL_N			CFP_PHY_RCAL_N		ATCRTMR1_CFP_RCAL_NEG
ATCRTMR1_CHIPID_0		M1	CHIP_ID_0	GPIO	PERIPHERAL	QSPI_CS*		SPI_ATCRTMR1_CS_L
ATCRTMR1_CHIPID_1		N1	CHIP_ID_1			QSPI_SCLK		SPI_ATCRTMR1_CLK
ATCRTMR1_BOOT_CONFIG0		H2	BOOT_CONFIG0			QSPI_DQ0		SPI_ATCRTMR1_DIO<0>
ATCRTMR1_BOOT_CONFIG1		J1	BOOT_CONFIG1			QSPI_DQ1		SPI_ATCRTMR1_DIO<1>
ATCRTMR1_BOOT_CONFIG2		K1	BOOT_CONFIG2			QSPI_DQ2		SPI_ATCRTMR1_DIO<2>
ATCRTMR1_FORCE_DFU		C1	FORCE_DFU			QSPI_DQ3		SPI_ATCRTMR1_DIO<3>
TP_ATCRTMR1_GPIO0		K2	GPIO0			I2C0_SCL		I2C_ATCRTMR_SCL
NC_ATCRTMR1_GPIO1	NO_TEST=1	L3	GPIO1			I2C0_SDA		I2C_ATCRTMR_SDA
TP_ATCRTMR1_GPIO2		K3	GPIO2			I2C1_SCL		I2C_UPC1_ATCRTMR1_SCL_1V2
TP_ATCRTMR1_GPIO3		L10	GPIO3			I2C1_SDA		I2C_UPC1_ATCRTMR1_SDA_1V2
						I2C1_INT		INT_I2C_UPC1_ATCRTMR1_L
ATCRTMR1_COLD_RESET_L		L2	COLD_RESET*			TESTMODE		ATCRTMR1_TESTMODE
ATCRTMR1_CFSB		M2	CFSB	CLOCKS AND RESET	TEST AND DEBUG	JTAG_SEL		ATCRTMR1_JTAGL_SEL
ATCRTMR1_XTAL24M_IN		F11	XI0			JTAG_TCK		SWD_NUB_ATCRTMR0_SWCLK
ATCRTMR1_XTAL24M_OUT		E11	XO0			JTAG_TMS		SWD_NUB_ATCRTMR0_SWDIO
						JTAG_TDI		TP_ATCRTMR1_JTAG_TDI
						JTAG_TDO		ATCRTMR1_JTAG_TDO
						JTAG_TRST*		TP_ATCRTMR1_JTAG_TRESET
						ANALOGMUX_OUT		TP_ATCRTMR1_ANALOGMUX_OUT
						TST_CLKOUT		TP_ATCRTMR1_TST_CLKOUT
						TST_CLK_LVDS_0_P		NC_ATCRTMR1_CLK_LVDS_P<0> NO_TEST=1
						TST_CLK_LVDS_0_N		NC_ATCRTMR1_CLK_LVDS_N<0> NO_TEST=1
						TST_CLK_LVDS_1_P		NC_ATCRTMR1_CLK_LVDS_P<1> NO_TEST=1
						TST_CLK_LVDS_1_N		NC_ATCRTMR1_CLK_LVDS_N<1> NO_TEST=1

ATCRTMR1_XTAL24M_OUT / ATCRTMR1_XTAL24M_IN

RF160 499 1% 1/20W TK 0201 — 197S0591 CRITICAL YF100 1.60X1.20MM 24.000MHZ-20PPM-9.5PF-60OHM — ATC1_24M_O_R

CRITICAL CF160 15PF 5% 50V C0G 0201 — CRITICAL CF161 15PF 5% 50V C0G 0201

PP0V855_ATCRTMR01_VDD_CIO

CF130 14UF 20% 4V X5R 0402-D2X-1 — CF131 14UF 20% 4V X5R 0402-D2X-1 — 138S00149

CF132 0.1UF 10% 6.3V X6S 0201 — CF133 0.1UF 10% 6.3V X6S 0201

PP0V805_ATCRTMR01_VDD_FIXED

CF140 0.1UF 10% 6.3V X6S 0201 — CF141 0.1UF 10% 6.3V X6S 0201 — CF142 2.2UF 20% 4V X6S-CERM 0201 — CF143 2.2UF 20% 4V X6S-CERM 0201 — CF144 2.2UF 20% 4V X6S-CERM 0201

CF145 14UF 20% 4V X5R 0402-D2X-1 — CF146 14UF 20% 4V X5R 0402-D2X-1

UF100 TMNB25B0-C1 FCCSP

OMIT_TABLE CRITICAL SYM 2 OF 2

VDD_CIO_0	J4	VDDIO12_CIO_0	K5
VDD_CIO_0	J6	VDDIO12_CIO_0	K7
VDD_CIO_0	J8	VDDIO12_CIO_0	L6
VDD_CIO_1	F4	VDDIO12_CIO_1	D6
VDD_CIO_1	F6	VDDIO12_CIO_1	E5
VDD_CIO_1	F8	VDDIO12_CIO_1	E7
		VDDIO12_PLL_SOC0	K8
		VDDIO12_PLL_SOC1	H8
		VDDIO12_XTAL	H9
		VDDIO12	E9
		VDDIO12	H3
		VDDIO12	K9
		VDDIO12_EFUSE1	F3
		VDDIO12_AMUX	F7
VDD_FIXED	G4		
VDD_FIXED	G5		
VDD_FIXED	H5		
VDD_FIXED	H6		
VDD_FIXED_PLL	G7		
VDD_FIXED_XTAL	G9		
VSS	A1	VSS	H4
VSS	A2	VSS	H7
VSS	A4	VSS	J2
VSS	A6	VSS	J3
VSS	A8	VSS	J5
VSS	A10	VSS	J7
VSS	A11	VSS	J10
VSS	B2	VSS	K4
VSS	B4	VSS	K6
VSS	B6	VSS	L1
VSS	B8	VSS	L5
VSS	B10	VSS	L7
VSS	C3	VSS	L11
VSS	C5	VSS	M3
VSS	C6	VSS	M5
VSS	C7	VSS	M6
VSS	C9	VSS	M7
VSS	D1	VSS	M9
VSS	D5	VSS	N2
VSS	D7	VSS	N4
VSS	D11	VSS	N6
VSS	E3	VSS	N8
VSS	E4	VSS	N10
VSS	E6	VSS	P1
VSS	E8	VSS	P2
VSS	F2	VSS	P4
VSS	F5	VSS	P6
VSS	F10	VSS	P8
VSS	G3	VSS	P10
VSS	G6	VSS	P11
VSS	G8		

PP1V2_ATCRTMR01_VDDIO

CF134 0.1UF 10% 6.3V X6S 0201 — CF135 2.2UF 20% 4V X6S-CERM 0201

CF136 14UF 20% 4V X5R 0402-D2X-1 — CF137 14UF 20% 4V X5R 0402-D2X-1

CF152 2.2UF 20% 4V X6S-CERM 0201 — PLACE_NEAR=UF100.K8:5MM

PP1V2_ATCRTMR01_VDDIO_XTAL_F — VOLTAGE=1.2V — FLF100 240-OHM-0.2A-0.9-OHM 155S0644 0201 — PP1V2_ATCRTMR01_VDDIO

CF162 0.1UF 10% 6.3V X6S 0201 — CF163 2.2UF 20% 4V X6S-CERM 0201

GND — Connect to GND directly or via a resistor

PP1V2_ATCRTMR01_VDDIO — CF164 0.1UF 10% 6.3V X6S 0201

PP0V805_ATCRTMR01_VDD_FIXED

CF150 0.1UF 10% 6.3V X6S 0201 — PLACE_NEAR=UF100.G7:5MM

VDD_FIXED_XTAL_ATC1_F

PP0V805_ATCRTMR01_VDD_FIXED — RF151 10 5% 1/20W TK 0201 — VOLTAGE=0.805V — CF151 4UF 20% 2.5V X6S 0201 — 117S00094 — 138S00329

ATCRTMR1_CFP_RCAL_NEG / ATCRTMR1_SFP_RCAL_NEG

CF111 10PF 5% 25V C0G 0201 — RF111 200 1% 1/20W TK 0201-1 — ATCRTMR1_CFP_RCAL_POS

CF110 10PF 5% 25V C0G 0201 — RF110 200 1% 1/20W TK 0201-1 — ATCRTMR1_SFP_RCAL_POS

SPI_ATCRTMR1_R_DIO

RF197 33 5% 1/20W TK 0201 — SPI_ATCRTMR1_DIO<0> — SPI_ATCRTMR1_R_DIO<0>

RF198 33 5% 1/20W TK 0201 — SPI_ATCRTMR1_DIO<1> — SPI_ATCRTMR1_R_DIO<1>

RF190 3.3K 5% 1/20W TK 0201 — NOSTUFF RF191 3.3K 5% 1/20W TK 0201 — NOSTUFF RF192 3.3K 5% 1/20W TK 0201 — NOSTUFF RF193 3.3K 5% 1/20W TK 0201 — CF190 1UF 10% 6.3V CERM 402

PP1V2_ATCRTMR01_VDDIO

VCC OMIT_TABLE CRITICAL 998-22993

UF190 64MBIT-1.2V W25Q64NE XSON

SPI_ATCRTMR1_CLK	RF194 33 5% 1/20W TK 0201	SPI_ATCRTMR1_CLK_R	CLK
SPI_ATCRTMR1_CS_L		SPI_ATCRTMR1_CS_L	CS*
SPI_ATCRTMR1_DIO<2>	RF195 33 5% 1/20W TK 0201	SPI_ATCRTMR1_R_DIO<2>	WP*(IO2)
SPI_ATCRTMR1_DIO<3>	RF196 33 5% 1/20W TK 0201	SPI_ATCRTMR1_R_DIO<3>	HOLD*(IO3)
		SPI_ATCRTMR1_R_DIO<0>	DI(IO0)
		SPI_ATCRTMR1_R_DIO<1>	DO(IO1)

GND EPAD

47K RF147 5% 1/20W TK 0201	ATCRTMR1_JTAGL_SEL	
10K RF140 5% 1/20W TK 0201	ATCRTMR1_TESTMODE	
47K RF143 5% 1/20W TK 0201	CIO_ATC1_LSTX	89
47K RF144 5% 1/20W TK 0201	CIO_ATC1_LSRX	89

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C: High Speed ATC1

Apple Inc.

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SIZE	D
REVISION	3.0.0
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*** OK2PLACE ***

SPI Master Ace

PP3V3_UPC0_LDO

RF260 3.3K 5% 1/20W TK 0201
RF261 3.3K 5% 1/20W TK 0201
RF263 3.3K 5% 1/20W TK 0201
RF262 3.3K 5% 1/20W TK 0201
CF260 1UF 10% 6.3V CERM 402

UF260 8MBIT-3.0V W25Q80DVUXIE USON
VCC CLK CS* WP*(IO2) HOLD*(IO3) DI(IO0) DO(IO1) GND EPAD
OMIT_TABLE CRITICAL 335S00133

ROM_UPC0_WP_L
ROM_UPC0_HOLD_L
NOSTUFF RF264 3.3K 5% 1/20W TK 0201

RF289 15 5% 1/20W TK 0201 — SPI_UPC0_MOSI → SPI_UPC0_R_MOSI
RF288 15 5% 1/20W TK 0201 — SPI_UPC0_MISO → SPI_UPC0_R_MISO
RF284 100 5% 1/20W TK 0201 — SPI_UPC0_CLK_DBG
NO_XNET_CONNECTION=1
RF285 15 5% 1/20W TK 0201 — SPI_UPC0_CLK → SPI_UPC0_R_CLK
RF287 15 5% 1/20W TK 0201 — SPI_UPC0_CS_L → SPI_UPC0_R_CS_L

SPI Secondary Ace

PP3V3_UPC1_LDO

RF250 3.3K 5% 1/20W TK 0201
RF251 3.3K 5% 1/20W TK 0201
RF253 3.3K 5% 1/20W TK 0201
RF252 3.3K 5% 1/20W TK 0201
CF250 1UF 10% 6.3V CERM 402

UF250 8MBIT-3.0V W25Q80DVUXIE USON
VCC CLK CS* WP*(IO2) HOLD*(IO3) DI(IO0) DO(IO1) GND EPAD
OMIT_TABLE CRITICAL 335S00133

ROM_UPC1_WP_L
ROM_UPC1_HOLD_L
NOSTUFF RF259 3.3K 5% 1/20W TK 0201

RF254 15 5% 1/20W TK 0201 — SPI_UPC1_MOSI → SPI_UPC1_R_MOSI
RF255 15 5% 1/20W TK 0201 — SPI_UPC1_MISO → SPI_UPC1_R_MISO
RF256 100 5% 1/20W TK 0201 — SPI_UPC1_CLK_DBG
NO_XNET_CONNECTION=1
RF257 15 5% 1/20W TK 0201 — SPI_UPC1_CLK → SPI_UPC1_R_CLK
RF258 15 5% 1/20W TK 0201 — SPI_UPC1_CS_L → SPI_UPC1_R_CS_L

PACK_OPTION=ACTIVE_READY:LARGE_PITCH

PP1V2_S2 — CF230 0.1UF 10% 6.3V CERM-X5R 0201
PP3V3_S2 — CF231 0.1UF 10% 6.3V CERM-X5R 0201

UF230 SN74AXC1T45-S SOT-5X3
VCCA VCCB DIR A B
PMU_ACTIVE_READY → ATCRTMR_ACTIVE_READY_3V3
311S00337 GND

UF230 SN74AXC1T45 X2SON
PACK_IGNORE=TRUE
PACK_OPTION=ACTIVE_READY:SMALL_PITCH_CHECK_WITH_DFM
311S00212 GND

PP1V2_S2
RF212 1.5K 5% 1/20W TK 0201
RF213 1.5K 5% 1/20W TK 0201
NOSTUFF RF211 0 0% 1/20W TK 0201 — INT_I2C_EUSBLS0_L → INT_I2C_UPC0_ATCRTMR0_L
RF216 0 0% 1/20W TK 0201 — INT_I2C_EUSBLS1_L → INT_I2C_UPC1_ATCRTMR1_L
NOSTUFF

USBC_ATC1_AUX_P — CF236 0.1UF 10% 6.3V CERM-X5R 0201 — USBC_ATC1_AUX_C_P
USBC_ATC1_AUX_N — CF237 0.1UF 10% 6.3V CERM-X5R 0201 — USBC_ATC1_AUX_C_N

USBC_ATC0_AUX_P — CF275 0.1UF 10% 6.3V CERM-X5R 0201 — USBC_ATC0_AUX_C_P
USBC_ATC0_AUX_N — CF276 0.1UF 10% 6.3V CERM-X5R 0201 — USBC_ATC0_AUX_C_N

KIS pack options for UPC1

PACK_OPTION=DUAL_KIS:YES
PD_UPC1_GPIO7 — MAKE_BASE=TRUE — PD_UPC1_GPIO7
PACK_IGNORE=TRUE PACK_OPTION=DUAL_KIS:NO
RF373 100K 1/20W 5% TK 0201 — PD_UPC1_GPIO7 MAKE_BASE=TRUE
RF328 100K 1/20W 5% TK 0201 — PD_UPC1_USBP2_RP MAKE_BASE=TRUE
RF329 100K 1/20W 5% TK 0201 — PD_UPC1_USBP2_RN MAKE_BASE=TRUE
PD_UPC1_USBP2_RP
PD_UPC1_USBP2_RN
PACK_OPTION=DUAL_KIS:YES
PD_UPC1_USBP2_RP
PD_UPC1_USBP2_RN

I2C Translation

PP1V2_S2
RF280 200K 0201 5% 1/20W TK
VREFB_UPC_ARDV0
USBC_DBG
PP3V3_S2
CF281 0.1UF 10% 6.3V CERM-X5R 0201
CF280 0.1UF 10% 6.3V CERM-X5R 0201
RF282 5.1K 5% 1/20W TK 0201
RF283 5.1K 5% 1/20W TK 0201
PACK_IGNORE=TRUE PACK_OPTION=PKGS:SMALL_PITCH
UF280 LSF0102 X2SON-COMBO 311S00234
VREF_A VREF_B EN A1 A2 B1 B2 GND
I2C_UPC_SCL → I2C_UPC01_3V3_SCL
I2C_UPC_SDA → I2C_UPC01_3V3_SDA
PACK_IGNORE=TRUE PACK_OPTION=PKGS:LARGER_PITCH
UF280 LSF0102 VSSOP 311S00257
UF280 LSF0102 DSBGA 311S00256
PACK_OPTION=PKGS:BGA

HV POWER ALIASES

Fuses for laptop charging.
PACK_OPTION=USBC_LAPTOP
PACK_IGNORE=TRUE PACK_OPTION=USBC_DESKTOP
Desktops only need connection for programming OTP.

CRITICAL FF200 6A-32V 0603-1 740S00053
PPDCIN_AON → PPHV_INT0_AONSW
PLACE_NEAR=UF400:5MM
MAKE_BASE=TRUE VOLTAGE=20V
RF200 0 0% 1/20W TK 0201
PPHV_INT0_AONSW

CRITICAL FF201 6A-32V 0603-1 740S00053
PPHV_INT1_AONSW
PLACE_NEAR=UF500:5MM
RF201 0 0% 1/20W TK 0201
PPHV_INT1_AONSW

PPVBUS_USBC0 — MAKE_BASE=TRUE — PPVBUS_USBC0
PPVBUS_USBC1 — MAKE_BASE=TRUE — PPVBUS_USBC1

ATCRTMR_ACTIVE_READY_3V3
NO_XNET_CONNECTION=1
RF290 100K 5% 1/20W TK 0201
USBC0_AUX_N — CF290 0.1UF 10% 6.3V CERM-X5R 0201 — USBC0_AUX_C_N
USBC0_AUX_P — CF291 0.1UF 10% 6.3V CERM-X5R 0201 — USBC0_AUX_C_P
RF292 33K 5% 1/20W TK 0201
RF293 33K 5% 1/20W TK 0201
RF291 100K 5% 1/20W TK 0201

ATCRTMR_ACTIVE_READY_3V3
NO_XNET_CONNECTION=1
RF298 100K 5% 1/20W TK 0201
USBC1_AUX_N — CF292 0.1UF 10% 6.3V CERM-X5R 0201 — USBC1_AUX_C_N
USBC1_AUX_P — CF293 0.1UF 10% 6.3V CERM-X5R 0201 — USBC1_AUX_C_P
RF296 33K 5% 1/20W TK 0201
RF297 33K 5% 1/20W TK 0201
RF299 100K 5% 1/20W TK 0201

ACE ARKANOID CONN

JF200 USBC_DBG 505070-1222 M-ST-SM
PACK_OPTION=KEEP_SMALL_ARKANOID_CONN

SMC		SOC
ATCRTMR0_FORCE_DFU	1–2	UPC_I2C_INT_L
I2C_SMC_UPC_SCL	3–4	I2C_UPC_SDA
I2C_SMC_UPC_SDA	5–6	I2C_UPC_SCL
UPC_SMC_I2C_INT_L	7–8	UPC0_SER_DBG
SPI_UPC0_CLK_DBG	9–10	UPC1_SER_DBG
SPI_UPC1_CLK_DBG	11–12	NC

BRIDGE ARKANOID CONN

JF201 USBC_DBG 505070-1222 M-ST-SM
PACK_OPTION=KEEP_SMALL_ARKANOID_CONN

ATCRTMR0_RESET_L	1–2	INT_I2C_UPC0_ATCRTMR0_L
UPC0_ATCRTMR01_PWR_EN	3–4	I2C_UPC0_ATCRTMR0_SCL
PP1V2_ATCRTMR01_VDDIO	5–6	I2C_UPC0_ATCRTMR0_SDA
PP0V855_ATCRTMR01_VDD_CIO	7–8	UPC1_ATCRTMR01_PWR_EN
ATCRTMR1_RESET_L	9–10	INT_I2C_UPC1_ATCRTMR1_L
I2C_UPC1_ATCRTMR1_SDA	11–12	I2C_UPC1_ATCRTMR1_SCL

AARDVARKANOID CONN FOR UPC1

JF203 USBC_DBG 505070-1222 M-ST-SM

PP1V2_S2	1–2	SPI_UPC1_CS_L
SWD_UPC_SWDIO3	3–4	SPI_UPC1_CLK
SWD_UPC_SWCLK1	5–6	SPI_UPC1_MOSI
SPI_UPC1_MISO	7–8	NC
I2C_UPC01_3V3_SDA	9–10	NC
I2C_UPC01_3V3_SCL	11–12	PP1V2_S2

AARDVARKANOID CONN UPC0

JF202 USBC_DBG 505070-1222 M-ST-SM
PACK_OPTION=KEEP_SMALL_ARKANOID_CONN

PP1V2_S2	1–2	SPI_UPC0_CS_L
SWD_UPC_SWDIO0	3–4	SPI_UPC0_CLK
SWD_UPC_SWCLK1	5–6	SPI_UPC0_MOSI
SPI_UPC0_MISO	7–8	NC
I2C_UPC01_3V3_SDA	9–10	NC
I2C_UPC01_3V3_SCL	11–12	PP1V2_S2

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: Support 1 ATC01

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*** OK2PLACE ***

Ace 0 is Debug Port?

PACK_OPTION=USBC_DEBUG_UPC0

ATC0 / UPC0 / RTMR0

UART_DEBUGPRT_R2D	UART_DEBUGPRT_R2D	UART_DEBUGPRT_R2D
UART_DEBUGPRT_D2R	UART_DEBUGPRT_D2R	UART_DEBUGPRT_D2R
SWD_SOC_SWCLK	SWD_SOC_SWCLK	SWD_SOC_SWCLK
SWD_SOC_SWDIO	SWD_SOC_SWDIO	SWD_SOC_SWDIO
UART_SMC_DEBUGPRT_R2D	UART_SMC_DEBUGPRT_R2D	UART_SMC_DEBUGPRT_R2D
UART_SMC_DEBUGPRT_D2R	UART_SMC_DEBUGPRT_D2R	UART_SMC_DEBUGPRT_D2R
USB_DBG_LS_P	USB_DBG_LS_P	USB_DBG_LS_N
USB_DBG_LS_N		

Ace 1 is Debug Port?

PACK_OPTION=USBC_DEBUG_UPC1

ATC1 / UPC1 / RTMR1

PD_UPC1_DBG0_R	UART_DEBUGPRT_R2D
PD_UPC1_DBG1_R	UART_DEBUGPRT_D2R
PD_UPC1_DBG2_R	SWD_SOC_SWCLK
PD_UPC1_DBG3_R	SWD_SOC_SWDIO
PD_UPC1_DBG4_R	UART_SMC_DEBUGPRT_R2D
PD_UPC1_DBG5_R	UART_SMC_DEBUGPRT_D2R
PD_UPC1_USBP2_RP	USB_DBG_LS_P
PD_UPC1_USBP2_RN	USB_DBG_LS_N

Main Debug Port

Ace2 GPIOs

SOC_DOCK_CONNECT_DBG_UPC	SOC_DOCK_CONNECT_DBG_UPC	PD_UPC1_GPIO7
SOC_DFU_STATUS	SOC_DFU_STATUS	PD_UPC1_GPIO9
SOC_FORCE_DFU	SOC_FORCE_DFU	PD_UPC1_GPIO10

PACK_OPTION=USBC_DEBUG_UPC0

Ace 1 is non-debug Port?

ATC1 / UPC1 / RTMR1

RF320	PD_UPC1_DBG0_R	PD_UPC1_DBG0_R
RF321	PD_UPC1_DBG1_R	PD_UPC1_DBG1_R
RF322	PD_UPC1_DBG2_R	PD_UPC1_DBG2_R
RF323	PD_UPC1_DBG3_R	PD_UPC1_DBG3_R
RF324	PD_UPC1_DBG4_R	PD_UPC1_DBG4_R
RF325	PD_UPC1_DBG5_R	PD_UPC1_DBG5_R
RF328 (NOSTUFF)	PD_UPC1_USBP2_RP	PD_UPC1_USBP2_RP
RF329 (NOSTUFF)	PD_UPC1_USBP2_RN	PD_UPC1_USBP2_RN

Ace2 GPIOs

RF373	PD_UPC1_GPIO7	PD_UPC1_GPIO7
RF374	PD_UPC1_GPIO9	PD_UPC1_GPIO9
RF375	PD_UPC1_GPIO10	PD_UPC1_GPIO10

CKPLUS_WAIVE=SINGLE_NODENET on all nets above.

Ace 0 is non-debug Port?

PACK IGNORE=TRUE
PACK_OPTION=USBC_DEBUG_UPC1

ATC0 / UPC0 / RTMR0

RF310	PD_UPC0_DBG0_R	UART_DEBUGPRT_R2D
RF311	PD_UPC0_DBG1_R	UART_DEBUGPRT_D2R
RF312	PD_UPC0_DBG2_R	SWD_SOC_SWCLK
RF313	PD_UPC0_DBG3_R	SWD_SOC_SWDIO
RF314	PD_UPC0_DBG4_R	UART_SMC_DEBUGPRT_R2D
RF315	PD_UPC0_DBG5_R	UART_SMC_DEBUGPRT_D2R
RF318	PD_UPC0_USBP2_RP	USB_DBG_LS_P
RF319	PD_UPC0_USBP2_RN	USB_DBG_LS_N

Ace2 GPIOs

RF363	PD_UPC0_GPIO7	SOC_DOCK_CONNECT_DBG_UPC
RF364	PD_UPC0_GPIO9	SOC_DFU_STATUS
RF365	PD_UPC0_GPIO10	SOC_FORCE_DFU

CKPLUS_WAIVE=SINGLE_NODENET on all nets above.

Non-debug Port

Unused ports

RF397	PD_UPC0_GPIO1	PD_UPC0_GPIO1
RF398	PD_UPC0_GPIO6	PD_UPC0_GPIO6
RF31A	PD_UPC0_USBP3_RP	PD_UPC0_USBP3_RP
RF31B	PD_UPC0_USBP3_RN	PD_UPC0_USBP3_RN

RF396	PD_UPC1_GPIO1	PD_UPC1_GPIO1
RF399	PD_UPC1_GPIO6	PD_UPC1_GPIO6
RF32A	PD_UPC1_USBP3_RP	PD_UPC1_USBP3_RP
RF32B	PD_UPC1_USBP3_RN	PD_UPC1_USBP3_RN

Connections for Laptops (USBC power in)

PACK_OPTION=USBC_LAPTOP

USBC0_CC1	USBC0_CC1
USBC0_CC2	USBC0_CC2

Connections for Desktops (No USBC power in)

PACK_OPTION=USBC_DESKTOP

MAKE_BASE=TRUE

Connections for Laptops (USBC power in)

PACK_OPTION=USBC_LAPTOP

USBC1_CC1	USBC1_CC1
USBC1_CC2	USBC1_CC2

Connections for Desktops (No USBC power in)

PACK_OPTION=USBC_DESKTOP

MAKE_BASE=TRUE

USBC0 PP_CABLE Protection

PP3V3_UPC0_LDO — CF300 1UF 10% 6.3V CERM 402

USBC0_VBIAS_PRT — CF301 0.1UF 10% 50V CERM-X7R 0402

MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

UF300 TPD4S311A BGA

NC_USBC0_CC_FLT_L (NO_TEST=1) — FLT*

USBC0_CC1 — CC1

USBC0_CC2 — CC2

C_SBU1 — C_SBU2 — C_CC1 — C_CC2 — RPD_G1 — RPD_G2

338S00753

USBC0_CC1_CONN — USBC0_CC2_CONN

MAKE_BASE=TRUE

PACK_OPTION=USBC_DESKTOP

PACK_OPTION=USBC_LAPTOP_CC_PRT
pack option for all component
PLACE_SIDE=TOP

USBC1 PP_CABLE Protection

PP3V3_UPC1_LDO — CF350 1UF 10% 6.3V CERM 402

USBC1_VBIAS_PRT — CF351 0.1UF 10% 50V CERM-X7R 0402

MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

UF350 TPD4S311A BGA

NC_USBC1_CC_FLT_L (NO_TEST=1) — FLT*

USBC1_CC1 — CC1

USBC1_CC2 — CC2

C_SBU1 — C_SBU2 — C_CC1 — C_CC2 — RPD_G1 — RPD_G2

338S00753

USBC1_CC1_CONN — USBC1_CC2_CONN

MAKE_BASE=TRUE

PACK_OPTION=USBC_DESKTOP

PACK_OPTION=USBC_LAPTOP_CC_PRT
pack option for all component
PLACE_SIDE=TOP

ATC0: I2C_ADDR=GND, I2CM_*_CNFG=1M\u03a9 3V3_LDO_X pull-ups
ATC1: I2C_ADDR=Float, I2CM_*_CNFG=1M\u03a9 3V3_LDO_X pull-ups
ATC2: I2C_ADDR=GND, I2CM_*_CNFG=1M\u03a9 pull-downs
ATC3: I2C_ADDR=Float, I2CM_*_CNFG=1M\u03a9 pull-downs

GND — NC_UPC1_I2C_ADDR — NC_UPC1_I2C_ADDR (NO_TEST=1)

Configure to enable VDDIO and use it for SWD.

GND — GND

Is UPCx_5V_EN being used?

UPC01_5V_EN — UPC01_5V_EN

RF350 100K 5% 1/20W TK 0201
RF351 100K 5% 1/20W TK 0201

PACK_IGNORE=TRUE
PACK_OPTION=USBC01_VR5V_LOCAL_NO

BOM_COST_GROUP=USB-C

ATCRTMR Boot Config

[2:0] = [011] 30Mhz QSPI and Test Mode Enabled
POR config should be [010] Test Mode Disabed

RF380 10K	ATCRTMR0_BOOT_CONFIG2	
RF381 10K	ATCRTMR0_BOOT_CONFIG1	NOSTUFF
RF382 10K	ATCRTMR0_BOOT_CONFIG0	LFKA_TEST_MODE:NO
RF383 10K	ATCRTMR1_BOOT_CONFIG2	
RF384 10K	ATCRTMR1_BOOT_CONFIG1	NOSTUFF
RF385 10K	ATCRTMR1_BOOT_CONFIG0	LFKA_TEST_MODE:NO

5% 1/20W TK 0201

LFKA_TEST_MODE:YES
RF386 10K
RF387 10K
RF388 10K NOSTUFF
PP1V2_ATCRTMR01_VDDIO
ATCRTMR0_BOOT_CONFIG2
ATCRTMR0_BOOT_CONFIG1
ATCRTMR0_BOOT_CONFIG0

LFKA_TEST_MODE:YES
RF389 10K
RF390 10K
RF391 10K NOSTUFF
PP1V2_ATCRTMR01_VDDIO
ATCRTMR1_BOOT_CONFIG2
ATCRTMR1_BOOT_CONFIG1
ATCRTMR1_BOOT_CONFIG0

ATCRTMR0 CHIP 0X00

RF392 10K ATCRTMR0_CHIPID_0
RF393 10K ATCRTMR0_CHIPID_1

ATCRTMR1 CHIP 0X01

PP1V2_ATCRTMR01_VDDIO
RF395 47K
ATCRTMR1_CHIPID_0

RF394 10K ATCRTMR1_CHIPID_1

ATCRTMR0_RESET_1V2_L — RF330 0 — ATCRTMR0_COLD_RESET_L
RF331 0 — ATCRTMR0_CFSB
RF332 0 NOSTUFF — P1V2_ATC01_PGOOD

ATCRTMR1_RESET_1V2_L — RF333 0 — ATCRTMR1_COLD_RESET_L
RF334 0 — ATCRTMR1_CFSB
RF335 0 NOSTUFF — P1V2_ATC01_PGOOD

0% 1/20W TK 0201

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USB-C: Support 2 ATC01

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*** OK2PLACE ***


PPHV_INT0_AONSW
MAX 100uF TOTAL ON RAIL
PP5V_S2SW_USBC01
PP5V_S2SW_USBC01
138S00070
CF406
4.7UF
20%
25V
X5R
0402
PP_5V0
PP_CABLE
PP_HV
VBUS
UF400
CD3217B12GACER
FCBGA
353S02742
CRITICAL
OMIT_TABLE
PPVBUS_USBC0
CF401
1UF
10%
35V
X5R
0402
CRITICAL
DF400
X3-WLB1608
SDM2U40CSPN-_-55
PP3V3_S2
CF400
10UF
20%
6.3V
CERM
0402
PP1V2_S2
CF402
1.0UF
20%
6.3V
X5R
0201-1
MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V
PP3V3_UPC0_LDO
CF408
10UF
20%
6.3V
CERM
0402
PP1V8_S2
CF403
0.1UF
10%
6.3V
CERM-X5R
0201
UPC0_ATCRTMR01_PWR_EN
(cap needed when used as power source)
PACK_OPTION=ACE2_SS_CAP
UPC0_SS
PP1V5_UPC0_LDO_CORE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.0750
CF405
10UF
20%
6.3V
CERM
0402
CF409
0.68UF
5%
6.3V
X6S
0402
PACK_OPTION=ACE2_SS_GND
GND
MAKE_BASE=TRUE
PPVBUS_USBC0
PPHV_INT0_AONSW
USBC0_CC1
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
USBC0_CC2
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
CF414
220PF
5%
50V
C0G
0201-1
CF413
220PF
5%
50V
C0G
0201-1
USBC0_CC1
USBC0_CC2
USBC0_USB_TOP_P
USBC0_USB_TOP_N
USBC0_USB_BOT_P
USBC0_USB_BOT_N
USBC0_SBU1
USBC0_SBU2
VIN_3V3
VDDIO
VDDIO_CFG
GND
LDO_3V3
VIN_LV
VOUT_LV
VRET
SS
LDO_CORE
VBUS_OPT
PP_HV_OPT
C_CC1
C_CC2
RPD_G1
RPD_G2
C_USB_TP
C_USB_TN
C_USB_BP
C_USB_BN
C_SBU1
C_SBU2
GND_OPT
GND_OPT
GND_OPT
GND_OPT
POWER
TYPE-C
GND
DIGITAL CORE I/O & CONTROL
PORT_MUX
PP3V3_UPC0_LDO
Internal Pull-ups
Enabled after reading straps
470K
RF409
5% 1/20W TK 0201
I2C_UPC0_ATCRTMR0_SCL
CKPLUS_WAIVE=I2C_PULLUP
470K
RF408
5% 1/20W TK 0201
I2C_UPC0_ATCRTMR0_SDA
CKPLUS_WAIVE=I2C_PULLUP
1M
RF405
5% 1/20W TK 0201
PD_UART_UPC0_RX_TX
100K
RF406
5% 1/20W TK 0201
PD_UPC0_MRESET
100K
RF407
5% 1/20W TK 0201
PD_UPC0_HPD
0
RF412
0% 1/20W TK 0201
PD_UPC0_HRESET
Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)
CRITICAL
RF403
15K
0.1%
1/20W
TK
0201
GND I2C ADDR
PRIMARY ONLY
REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI
PD_UPC0_HRESET
PD_UPC0_MRESET
ATCRTMR0_RESET_L
UPC0_SER_DBG
PD_UPC0_GPIO1
INT_I2C_UPC0_ATCRTMR0_L
UPC01_5V_EN
ATCRTMR0_FORCE_DFU
UPC0_CHGR_AUX_DET_SHORT
PD_UPC0_GPIO6
SOC_DOCK_CONNECT_DBG_UPC
UPC_PMU_RESET_1V2_R
SOC_DFU_STATUS
SOC_FORCE_DFU
GND
GND
UPC0_R_OSC
I2C_UPC0_ATCRTMR0_SDA
I2C_UPC0_ATCRTMR0_SCL
I2C_UPC_SDA
I2C_UPC_SCL
UPC_I2C_INT_L
I2C_SMC_UPC_SDA
I2C_SMC_UPC_SCL
UPC_SMC_I2C_INT_L
SPI_UPC0_R_CLK
SPI_UPC0_R_MOSI
SPI_UPC0_R_MISO
SPI_UPC0_R_CS_L
SWD_UPC_SWDIO0
SWD_UPC_SWCLK1
PD_UART_UPC0_RX_TX
USB2_UPC0_P1_P
USB2_UPC0_P1_N
USB_DBG_LS_P
USB_DBG_LS_N
PD_UPC0_USBP3_RP
PD_UPC0_USBP3_RN
USBC0_AUX_C_P
USBC0_AUX_C_N
PD_UPC0_HPD
UART_DEBUGPRT_R2D
UART_DEBUGPRT_D2R
SWD_SOC_SWCLK
SWD_SOC_SWDIO
UART_SMC_DEBUGPRT_R2D
UART_SMC_DEBUGPRT_D2R
USBC0_CIO_LSTX_3V3
USBC0_CIO_LSRX_3V3
HRESET
MRESET
RESET* 3V3
GPIO0
GPIO1
GPIO2 1V2
GPIO3 3V3
GPIO4 1V2
GPIO5 3V3
GPIO6
GPIO7
GPIO8 1V2
GPIO9
GPIO10
BUSPOWER
I2C_ADDR IPU-BOOT
R_OSC
I2CM_SDA_CNFG IPU-AFTER-BOOT
I2CM_SCL_CNFG IPU-AFTER-BOOT
I2C_SDA1
I2C_SCL1
I2C_IRQ1*
I2C_SDA2
I2C_SCL2
I2C_IRQ2*
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SSZ
SWD_DATA IPU
SWD_CLK IPU
UART_RX
UART_TX
USB_RP1_P
USB_RP1_N
USB_RP2_P
USB_RP2_N
USB_RP3_P
USB_RP3_N
AUX_P
AUX_N
HPD
DEBUG0
DEBUG1
DEBUG2
DEBUG3
DEBUG4
DEBUG5
DEBUG6
DEBUG7
GND

BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: Port Controller ATC0

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PPHV_INT1_AONSW
MAX 100uF TOTAL ON RAIL
PP5V_S2SW_USBC01
PP5V_S2SW_USBC01
138S00070
CF506
4.7UF
20% 25V X5R 0402
PP_5V0
PP_CABLE
PP_HV
VBUS
353S02742
CRITICAL
OMIT_TABLE
UF500
CD3217B12GACER
FCBGA
PPVBUS_USBC1
CF501
1UF
10% 35V X5R 0402
CRITICAL
DF500
X3-WLB1608
SDM2U40CSPN-_-55
PP3V3_S2
CF500
10UF
20% 6.3V CERM 0402
PP1V2_S2
CF502
1.0UF
20% 6.3V X5R 0201-1
MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V
PP3V3_UPC1_LDO
CF508
10UF
20% 6.3V CERM 0402
PP1V8_S2
CF503
0.1UF
10% 6.3V CERM-X5R 0201
UPC1_ATCRTMR01_PWR_EN
(cap needed when used as power source)
PACK_OPTION=ACE2_SS_CAP
UPC1_SS
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.0750
PP1V5_UPC1_LDO_CORE
CF509
0.68UF
5% 6.3V X6S 0402
PACK_OPTION=ACE2_SS_GND
GND
MAKE_BASE=TRUE
CF505
10UF
20% 6.3V CERM 0402
PPVBUS_USBC1
PPHV_INT1_AONSW
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
USBC1_CC1
USBC1_CC2
CF514
220PF
5% 50V C0G 0201-1
CF513
220PF
5% 50V C0G 0201-1
USBC1_CC1
USBC1_CC2
USBC1_USB_TOP_P
USBC1_USB_TOP_N
USBC1_USB_BOT_P
USBC1_USB_BOT_N
USBC1_SBU1
USBC1_SBU2
VIN_3V3
VDDIO
VDDIO_CFG
LDO_3V3
VIN_LV
VOUT_LV
VRET
SS
LDO_CORE
VBUS_OPT
PP_HV_OPT
C_CC1
C_CC2
RPD_G1
RPD_G2
C_USB_TP
C_USB_TN
C_USB_BP
C_USB_BN
C_SBU1
C_SBU2
GND_OPT
POWER
TYPE-C
GND
PORT_MUX
DIGITAL CORE I/O & CONTROL
PP3V3_UPC1_LDO
470K RF509
5% 1/20W TK 0201
I2C_UPC1_ATCRTMR1_SCL
CKPLUS_WAIVE=I2C_PULLUP
470K RF508
5% 1/20W TK 0201
I2C_UPC1_ATCRTMR1_SDA
CKPLUS_WAIVE=I2C_PULLUP
1M RF505
5% 1/20W TK 0201
PD_UART_UPC1_RX_TX
100K RF506
5% 1/20W TK 0201
PD_UPC1_MRESET
100K RF507
5% 1/20W TK 0201
PD_UPC1_HPD
0 RF512
0% 1/20W TK 0201
PD_UPC1_HRESET
Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)
CRITICAL
RF503
15K
0.1% 1/20W TK 0201
GND I2C ADDR
PRIMARY ONLY
REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI
PD_UPC1_HRESET
PD_UPC1_MRESET
ATCRTMR1_RESET_L
UPC1_SER_DBG
PD_UPC1_GPIO1
INT_I2C_UPC1_ATCRTMR1_L
UPC01_5V_EN
ATCRTMR1_FORCE_DFU
UPC1_CHGR_AUX_DET_SHORT
PD_UPC1_GPIO6
PD_UPC1_GPIO7
UPC_PMU_RESET_1V2_R
PD_UPC1_GPIO9
PD_UPC1_GPIO10
GND
NC_UPC1_I2C_ADDR
UPC1_R_OSC
I2C_UPC1_ATCRTMR1_SDA
I2C_UPC1_ATCRTMR1_SCL
I2C_UPC_SDA
I2C_UPC_SCL
UPC_I2C_INT_L
I2C_SMC_UPC_SDA
I2C_SMC_UPC_SCL
UPC_SMC_I2C_INT_L
SPI_UPC1_R_CLK
SPI_UPC1_R_MOSI
SPI_UPC1_R_MISO
SPI_UPC1_R_CS_L
SWD_UPC_SWDIO3
SWD_UPC_SWCLK1
PD_UART_UPC1_RX_TX
USB2_UPC1_P1_P
USB2_UPC1_P1_N
PD_UPC1_USBP2_RP
PD_UPC1_USBP2_RN
PD_UPC1_USBP3_RP
PD_UPC1_USBP3_RN
USBC1_AUX_C_P
USBC1_AUX_C_N
PD_UPC1_HPD
PD_UPC1_DBG0_R
PD_UPC1_DBG1_R
PD_UPC1_DBG2_R
PD_UPC1_DBG3_R
PD_UPC1_DBG4_R
PD_UPC1_DBG5_R
USBC1_CIO_LSTX_3V3
USBC1_CIO_LSRX_3V3
HRESET
MRESET
RESET* 3V3
GPIO0
GPIO1
GPIO2 1V2
GPIO3 3V3
GPIO4 1V2
GPIO5 3V3
GPIO6
GPIO7
GPIO8 1V2
GPIO9
GPIO10
BUSPOWER
I2C_ADDR IPU-BOOT
R_OSC
I2CM_SDA_CNFG IPU-AFTER-BOOT
I2CM_SCL_CNFG IPU-AFTER-BOOT
I2C_SDA1
I2C_SCL1
I2C_IRQ1*
I2C_SDA2
I2C_SCL2
I2C_IRQ2*
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SSZ
SWD_DATA IPU
SWD_CLK IPU
UART_RX
UART_TX
USB_RP1_P
USB_RP1_N
USB_RP2_P
USB_RP2_N
USB_RP3_P
USB_RP3_N
AUX_P
AUX_N
HPD
DEBUG0
DEBUG1
DEBUG2
DEBUG3
DEBUG4
DEBUG5
DEBUG6
DEBUG7

BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: Port Controller ATC1

Apple Inc.

DRAWING NUMBER 051-08156 SIZE D
REVISION 3.0.0
BRANCH evt-1
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*** OK2INTEGRATE ***
MACAW 0
PP1V2_S2
CF612 1.0UF 20% 6.3V X5R 0201-1
CF613 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF600.A4:5MM
PP1V8_S2
CF604 0.1UF 10% 10V X5R-CERM 0201
CF602 0.1UF 10% 10V X5R-CERM 0201
CF603 4.7UF 20% 4V CER-X5R 0201
CF600 1.0UF 20% 6.3V X5R 0201-1
CF615 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF600.B5:5MM
PP1V1_MACAW0_VCCD
VOLTAGE=1.1V
CF606 4.7UF 20% 6.3V X6S 0402
PP3V3_S2
CF607 0.1UF 10% 10V X5R-CERM 0201
CF608 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF600.C6:5MM
UF600
CYUSB2405A2
CSP
338S00851
OMIT_TABLE
CRITICAL
VCCD VDDD VDDIO VDD3V3
RESET* INT SDA SCL EDP0 EDN0 EDP1 EDN1 CROSS GPIO_0/SWDCLK GPIO_1/SWDDAT
DP0 DN0 DP1 DN1 XIP XOP RESREF VSS VSSQ
MACAW_I2C_MASK
VREFB_ATC0
QF601
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2
RF603 47K 5% 1/20W TK 0201
ATCRTMR0_RESET_1V2_1V8_MCW_L
INT_I2C_EUSBLS0_L
I2C_UPC0_ATCRTMR0_SDA_1V2
I2C_UPC0_ATCRTMR0_SCL_1V2
EUSB_ATC0_P
EUSB_ATC0_N
EUSB_ATC0_DBG_P
EUSB_ATC0_DBG_N
TP_MACAW0_DEBUG_SWDCLK
TP_MACAW0_DEBUG_SWDDAT
USB2_ATC0_LS_MUX_P
USB2_ATC0_LS_MUX_N
USB_DBG_LS_MUX_P
USB_DBG_LS_MUX_N
MACAW0_CLK24M_IN
MACAW0_CLK24M_OUT_R
RF600 0 1/20W 0% TK 0201
MACAW0_CLK24M_OUT
YF600 1.60X1.20MM
197S0591
131S00077
CF611 9.5PF +/-0.1PF 50V CER-C0G 0201
CF610 9.5PF +/-0.1PF 50V CER-C0G 0201
MACAW0_RESREF
RF601 6.04K 1% 1/20W TK 0201
USBC_DUAL_KIS:NO
PLACE_NEAR=UF690.1:2MM
EUSB_DBG_P
RF690 0 1/20W 0% TK 0201
EUSB_DBG_N
RF691 0 1/20W 0% TK 0201
PLACE_NEAR=UF690.2:2MM
PP3V3_S2
CF690 1.0UF 20% 6.3V X5R 0201-1
USBC_DUAL_KIS:YES
UF690
PI3USB102EZLE
TQFN
353S4037
VCC Y+ Y- SEL GND M+ M- D+ D- OE*
EUSB_ATC1_DBG_P
EUSB_ATC1_DBG_N
PD_UPC1_GPIO7
RF692 100K 5% 1/20W TK 0201
LOW --> UPC0 Default KIS
HIGH --> UPC1 KIS
MACAW 1
PP1V2_S2
CF662 1.0UF 20% 6.3V X5R 0201-1
CF663 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF650.A4:5MM
PP1V8_S2
CF654 0.1UF 10% 10V X5R-CERM 0201
CF651 0.1UF 10% 10V X5R-CERM 0201
CF652 4.7UF 20% 4V CER-X5R 0201
138S00138
CF653 1.0UF 20% 6.3V X5R 0201-1
CF665 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF650.B5:5MM
PP1V1_MACAW1_VCCD
VOLTAGE=1.1V
CF656 4.7UF 20% 6.3V X6S 0402
PP3V3_S2
CF657 0.1UF 10% 10V X5R-CERM 0201
CF658 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF650.C6:5MM
UF650
CYUSB2405A2
CSP
338S00851
OMIT_TABLE
CRITICAL
MACAW_I2C_MASK
VREFB_ATC1
QF651
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2
RF653 47K 5% 1/20W TK 0201
ATCRTMR1_RESET_1V2_L
INT_I2C_EUSBLS1_L
I2C_UPC1_ATCRTMR1_SDA_1V2
I2C_UPC1_ATCRTMR1_SCL_1V2
EUSB_ATC1_P
EUSB_ATC1_N
EUSB_ATC1_DBG_P
EUSB_ATC1_DBG_N
PACK_OPTION=DUAL_KIS:YES
TP_MACAW1_DEBUG_SWDCLK
TP_MACAW1_DEBUG_SWDDAT
USB2_ATC1_LS_P
USB2_ATC1_LS_N
PD_UPC1_USBP2_RP
PD_UPC1_USBP2_RN
MACAW1_CLK24M_IN
MACAW1_CLK24M_OUT_R
RF650 0 1/20W 0% TK 0201
MACAW1_CLK24M_OUT
YF660 1.60X1.20MM
197S0591
131S00077
CF661 9.5PF +/-0.1PF 50V CER-C0G 0201
CF660 9.5PF +/-0.1PF 50V CER-C0G 0201
MACAW1_RESREF
RF651 6.04K 1% 1/20W TK 0201
USBC_DUAL_KIS:NO
RF697 0 1/20W 0% TK 0201
SOC_DOCK_CONNECT_DBG_UPC
SOC_DOCK_CONNECT_UPC
PP1V2_S2
USBC_DUAL_KIS:YES
CF695 0.1UF 10% 10V X5R-CERM 0201
RF695 0 1/20W 0% TK 0201
PD_UPC1_GPIO7
SOC_DOCK_CONNECT_DUAL_KIS_R
SOC_DOCK_CONNECT_DBG_UPC
UF695
SN74AUP1G32
SOT553
311S00301
SOC_DOCK_CONNECT_UPC
USBC_DUAL_KIS:YES
RF696 100K 5% 1/20W TK 0201
NOSTUFF
CF696 0.1UF 10% 10V X5R-CERM 0201
BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: USB2 RPT

Apple Inc.

DRAWING NUMBER 051-08156
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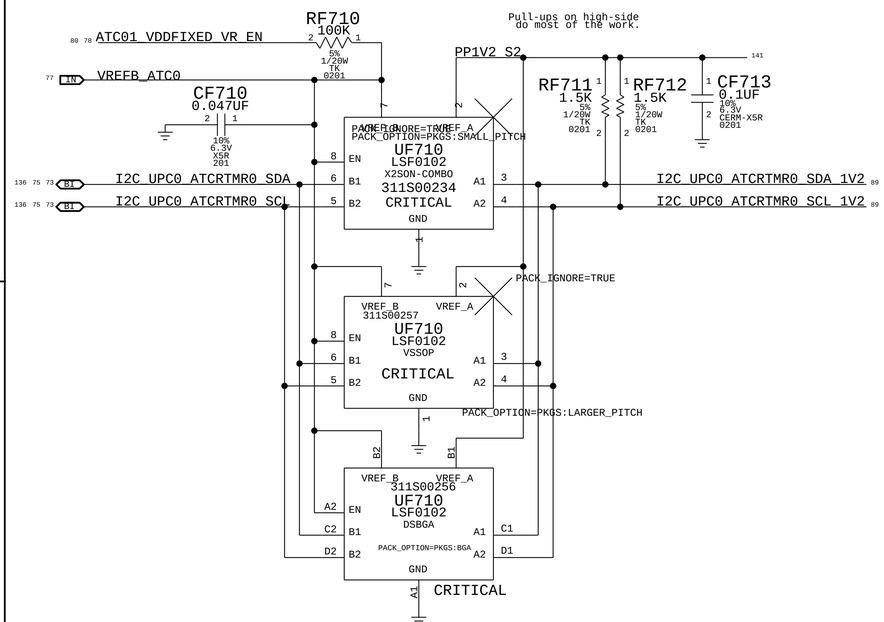
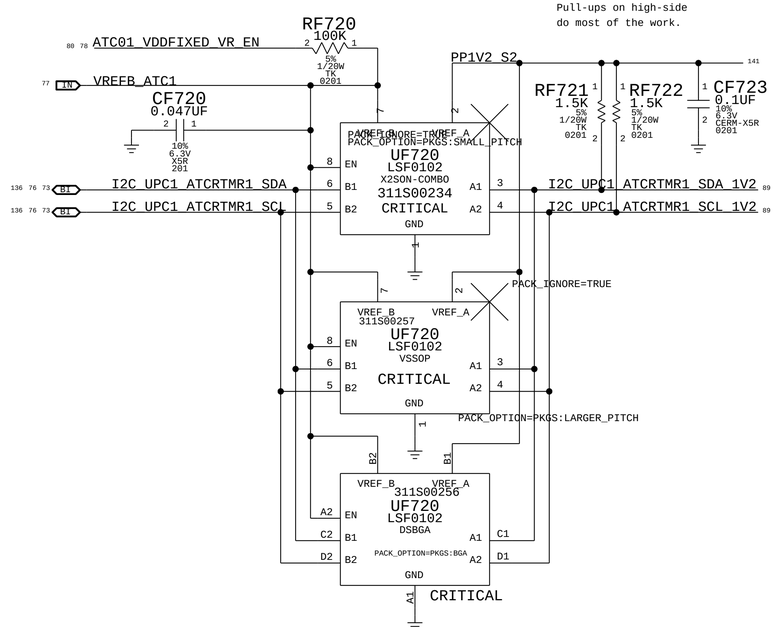
*** OK2INTEGRATE ***

Sequencing Requirements: 3.3V to UF790 --> system 1.2V (UF710,UF720) same time or before system 1.8V (UF400&UF500 VIN_LV pin)

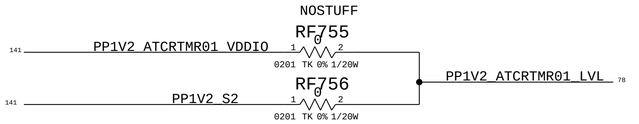
ATC0 RE-TIMER I2C LEVEL SHIFTERS



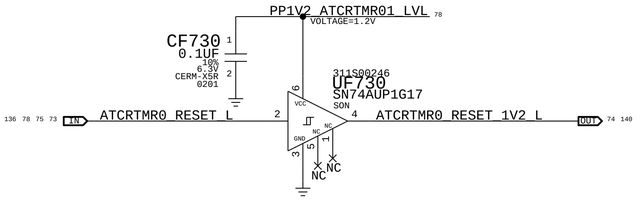
ATC1 RE-TIMER I2C LEVEL SHIFTERS



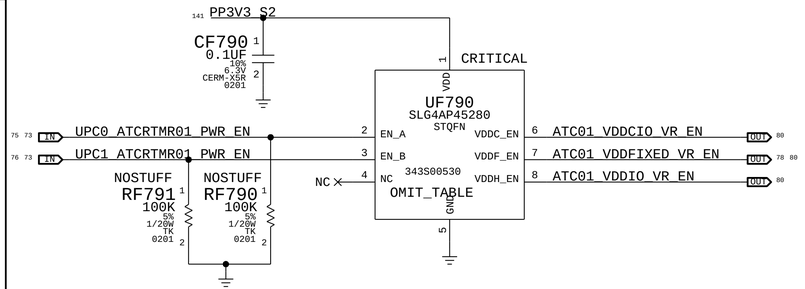
NOSTUFF

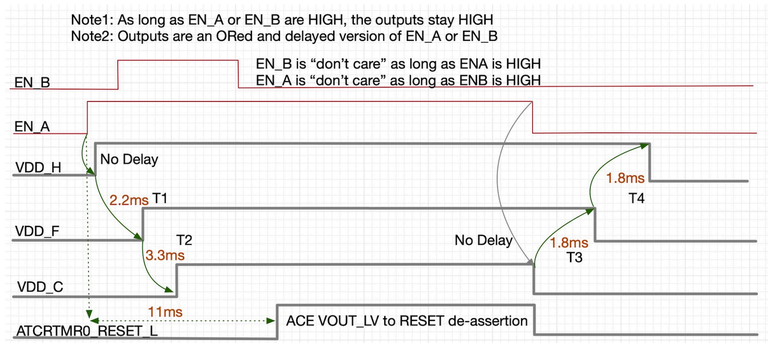


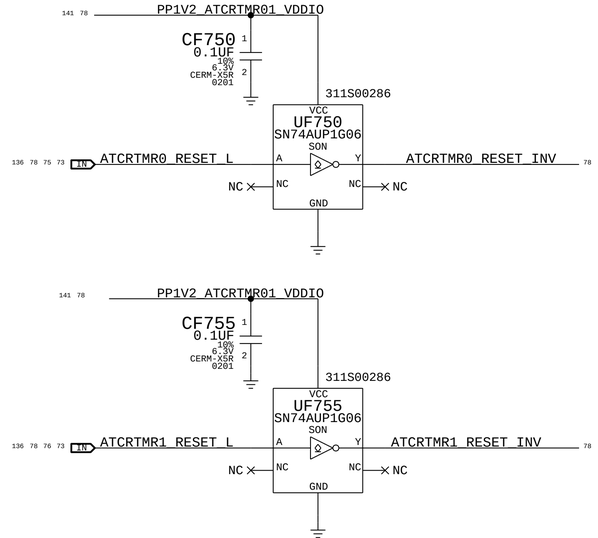
ATC0/1 AND MACAW RESET LEVEL SHIFTERS

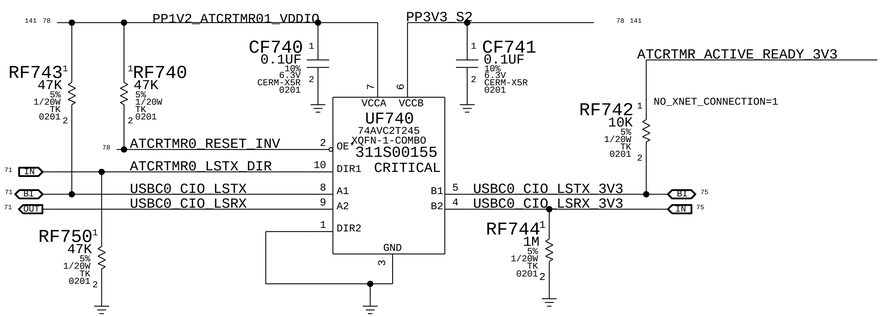


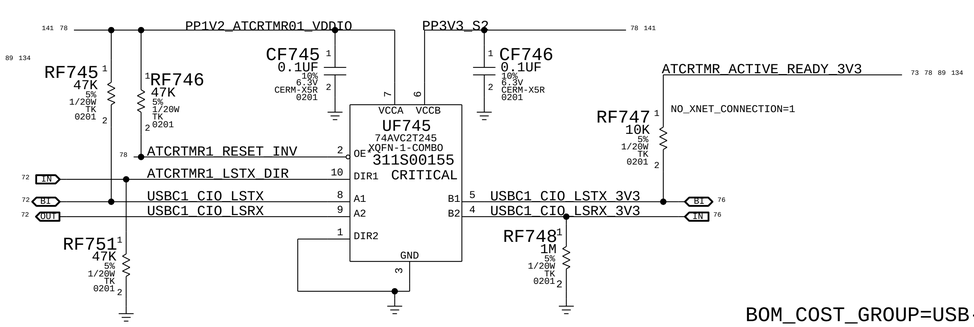
The 3.3V needs to be HIGH before VIN_LV of Aces











BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: HS Level Shifters ATC01

Apple Inc.

DRAWING NUMBER	051-08156
SIZE	D
REVISION	3.0.0
BRANCH	evt-1
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*** OK2INTEGRATE ***

SET ONE OPTION FOR THE PBUS CAPS

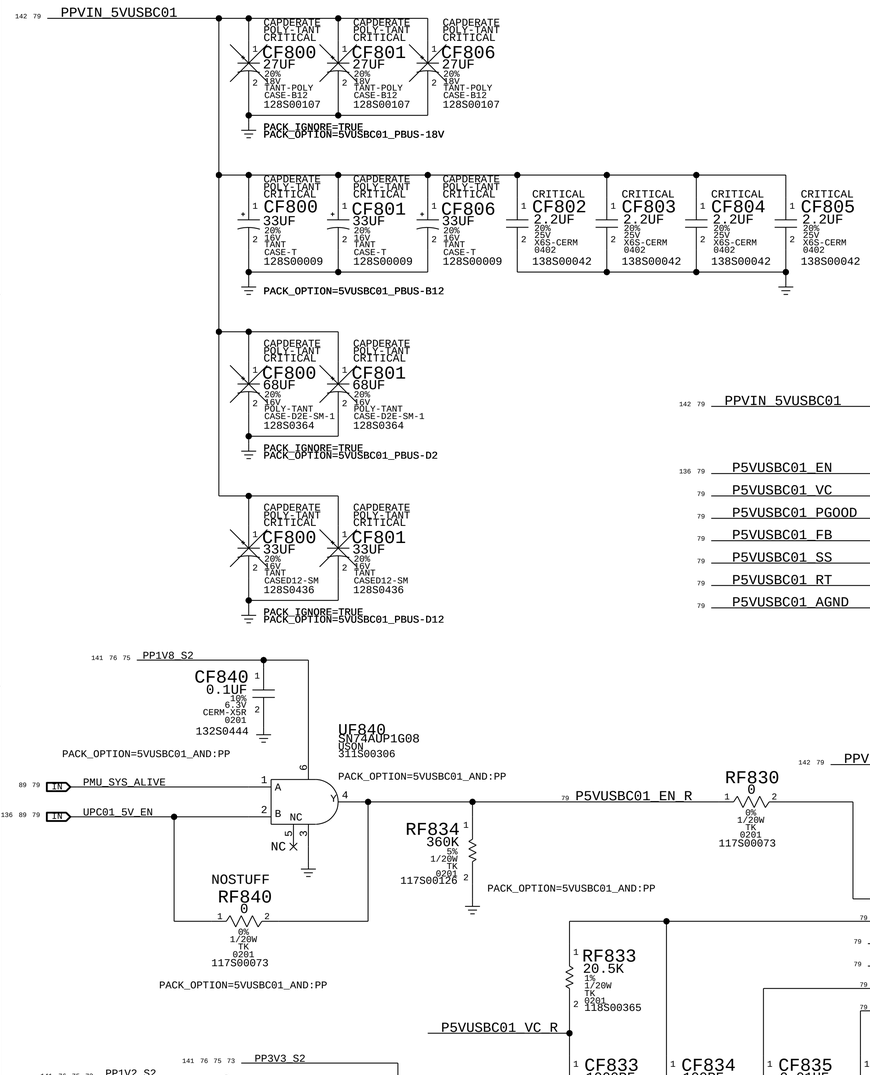
PACK_OPTION=5VUSBC01_PBUS-B12
PACK_OPTION=5VUSBC01_PBUS-D2
PACK_OPTION=5VUSBC01_PBUS-D12
PACK_OPTION=5VUSBC01_PBUS-18V

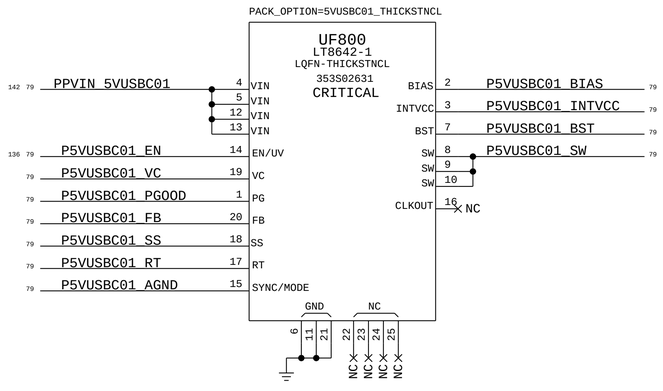
SET ONE OPTION FOR UF800

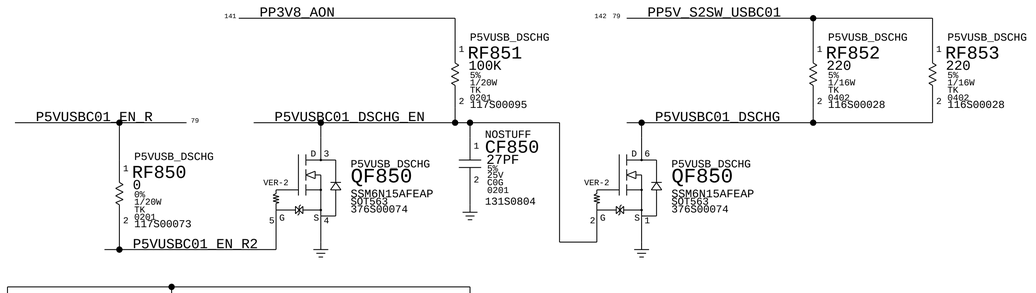
PACK_OPTION=5VUSBC01_THINSTNCL
PACK_OPTION=5VUSBC01_THICKSTNCL

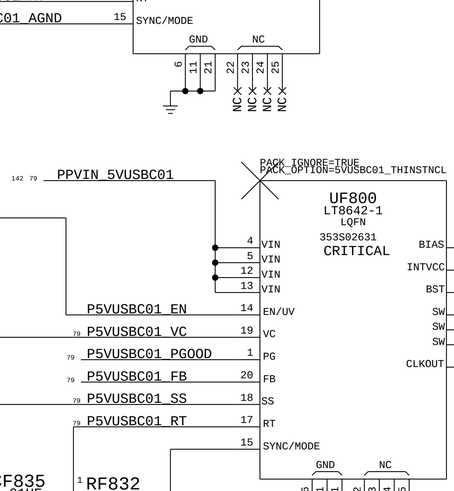
SET ONE OPTION FOR UF840 BUFFER

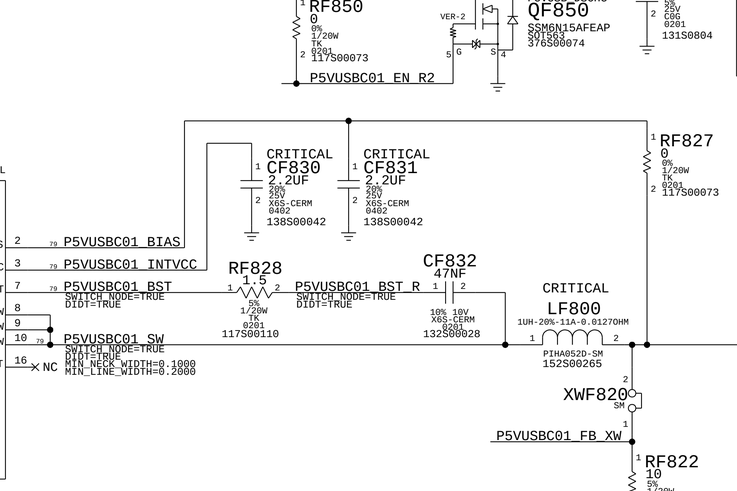
PACK_OPTION=5VUSBC01_AND:PP
PACK_OPTION=5VUSBC01_AND:OD

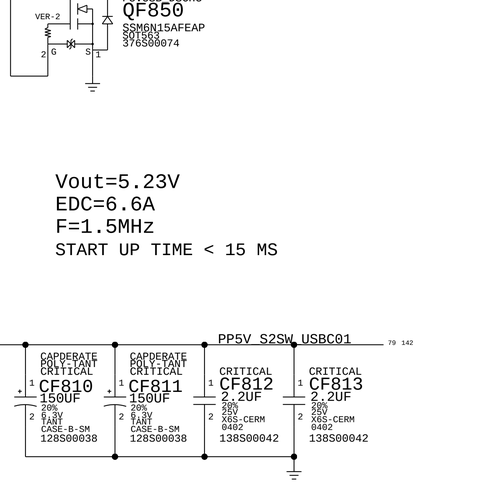












Vout=5.23V
EDC=6.6A
F=1.5MHz
START UP TIME < 15 MS

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: 5V Regulator

Apple Inc.

DRAWING NUMBER: 051-08156
SIZE: D
REVISION: 3.0.0
BRANCH: evt-1
PAGE: 158 OF 700
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*** OK2INTEGRATE ***

*** OK2INTEGRATE ***

No lane swapping is allowed
Re-timer to SOC connections are set

Re-timer to connector connections are set

PP1V2_ATCRTMR2_VDDIO 81 83 141

2 47K 1 RG045 5% 1/20W TK 0201 ATCRTMR2_JTAG_TDO 81

USBC HIGH-SPEED AC COUPLING

147 IN	USBC_ATC2_R2D_LS_C_P<1>	GND_VOID=TRUE	CG020 0.22UF	20% 6.3V X5R 0201	USBC_ATC2_R2D_T_P<1>	81
147 IN	USBC_ATC2_R2D_LS_C_N<1>	GND_VOID=TRUE	CG021 0.22UF	20% 6.3V X5R 0201	USBC_ATC2_R2D_T_N<1>	81
147 IN	USBC_ATC2_R2D_LS_C_P<2>	GND_VOID=TRUE	CG024 0.22UF	20% 6.3V X5R 0201	USBC_ATC2_R2D_T_P<2>	81
147 IN	USBC_ATC2_R2D_LS_C_N<2>	GND_VOID=TRUE	CG025 0.22UF	20% 6.3V X5R 0201	USBC_ATC2_R2D_T_N<2>	81
147 BI	USBC_ATC2_D2R_LS_P<1>	GND_VOID=TRUE	CG022 0.22UF	20% 6.3V X5R 0201	USBC_ATC2_D2R_TC_P<1>	81
147 BI	USBC_ATC2_D2R_LS_N<1>	GND_VOID=TRUE	CG023 0.22UF	20% 6.3V X5R 0201	USBC_ATC2_D2R_TC_N<1>	81
147 BI	USBC_ATC2_D2R_LS_P<2>	GND_VOID=TRUE	CG026 0.22UF	20% 6.3V X5R 0201	USBC_ATC2_D2R_TC_P<2>	81
147 BI	USBC_ATC2_D2R_LS_N<2>	GND_VOID=TRUE	CG027 0.22UF	20% 6.3V X5R 0201	USBC_ATC2_D2R_TC_N<2>	81

ATCRTMR2_XTAL24M_OUT 81

RG060 499 1% 1/20W TK 0201

197S0591 CRITICAL YG000 1.60X1.20MM 24.000MHZ-20PPM-9.5PF-60OHM

ATCRTMR2_XTAL24M_IN 81

ATC2_24M_O_R

CRITICAL CG060 15PF 5% 50V C0G 0201

CRITICAL CG061 15PF 5% 50V C0G 0201

141 PP0V855_ATCRTMR2_VDD_CIO

CG030 14UF 20% 4V X5R 0402-D2X-1 138S00149

CG031 14UF 20% 4V X5R 0402-D2X-1

CG032 0.1UF 10% 6.3V X6S 0201

CG033 0.1UF 10% 6.3V X6S 0201

PP0V805_ATCRTMR2_VDD_FIXED 141 81

CG040 0.1UF 10% 6.3V X6S 0201

CG041 0.1UF 10% 6.3V X6S 0201

CG042 2.2UF 20% 4V X6S-CERM 0201

CG043 2.2UF 20% 4V X6S-CERM 0201

CG044 2.2UF 20% 4V X6S-CERM 0201

CG045 14UF 20% 4V X5R 0402-D2X-1

CG046 14UF 20% 4V X5R 0402-D2X-1

PP0V805_ATCRTMR2_VDD_FIXED 141 81

CG050 0.1UF 10% 6.3V X6S 0201

PLACE_NEAR=UG000.G7:5MM

VDD_FIXED_XTAL_ATC2_F

141 PP0V805_ATCRTMR2_VDD_FIXED

RG051 10 5% 1/20W TK 0201 VOLTAGE=0.805V

CG051 4UF 20% 2.5V X6S 0201 117S00094 138S00329

UG000 TMNB25B0-C1 FCCSP

OMIT_TABLE CRITICAL SYM 2 OF 2

J4	VDD_CIO_0	VDDIO12_CIO_0	K5
J6	VDD_CIO_0	VDDIO12_CIO_0	K7
J8	VDD_CIO_0	VDDIO12_CIO_0	L6
F4	VDD_CIO_1	VDDIO12_CIO_1	D6
F6	VDD_CIO_1	VDDIO12_CIO_1	E5
F8	VDD_CIO_1	VDDIO12_CIO_1	E7
		VDDIO12_PLL_SOC0	K8
		VDDIO12_PLL_SOC1	H8
		VDDIO12_XTAL	H9
		VDDIO12	E9
		VDDIO12	H3
		VDDIO12	K9
G4	VDD_FIXED	VDDIO12_EFUSE1	F3
G5	VDD_FIXED	VDDIO12_AMUX	F7
H5	VDD_FIXED		
H6	VDD_FIXED		
G7	VDD_FIXED_PLL		
G9	VDD_FIXED_XTAL		
A1	VSS	VSS	H4
A2	VSS	VSS	H7
A4	VSS	VSS	J2
A6	VSS	VSS	J3
A8	VSS	VSS	J5
A10	VSS	VSS	J7
A11	VSS	VSS	J10
B2	VSS	VSS	K4
B4	VSS	VSS	K6
B6	VSS	VSS	L1
B8	VSS	VSS	L5
B10	VSS	VSS	L7
C3	VSS	VSS	L11
C5	VSS	VSS	M3
C6	VSS	VSS	M5
C7	VSS	VSS	M6
C9	VSS	VSS	M7
D1	VSS	VSS	M9
D5	VSS	VSS	N2
D7	VSS	VSS	N4
D11	VSS	VSS	N6
E3	VSS	VSS	N8
E4	VSS	VSS	N10
E6	VSS	VSS	P1
E8	VSS	VSS	P2
F2	VSS	VSS	P4
F5	VSS	VSS	P6
F10	VSS	VSS	P8
G3	VSS	VSS	P10
G6	VSS	VSS	P11
G8	VSS		

CG034 0.1UF 10% 6.3V X6S 0201

CG035 2.2UF 20% 4V X6S-CERM 0201

PP1V2_ATCRTMR2_VDDIO 81 83 141

CG036 14UF 20% 4V X5R 0402-D2X-1

CG037 14UF 20% 4V X5R 0402-D2X-1

PP1V2_ATCRTMR2_VDDIO 141

CG052 2.2UF 20% 4V X6S-CERM 0201

PLACE_NEAR=UG000.K8:5MM

PP1V2_ATCRTMR2_VDDIO_XTAL_F VOLTAGE=1.2V

155S0644 FLG000 240-OHM-0.2A-0.9-OHM 0201

PP1V2_ATCRTMR2_VDDIO 141

CG062 0.1UF 10% 6.3V X6S 0201

CG063 2.2UF 20% 4V X6S-CERM 0201

Connect to GND directly or via a resistor

GND 141

PP1V2_ATCRTMR2_VDDIO 141

CG064 0.1UF 10% 6.3V X6S 0201

CG011 10PF 5% 25V C0G 0201

ATCRTMR2_CFP_RCAL_NEG 81

RG011 200 1% 1/20W TK 0201-1

ATCRTMR2_CFP_RCAL_POS 81

CG010 10PF 5% 25V C0G 0201

ATCRTMR2_SFP_RCAL_NEG 81

RG010 200 1% 1/20W TK 0201-1

ATCRTMR2_SFP_RCAL_POS 81

UG000 TMNB25B0-C1 FCCSP

OMIT_TABLE CRITICAL 998-25504 SYM 1 OF 2

81	USBC_ATC2_D2R_TC_P<1>	GND_VOID=TRUE	P9	SFP_PHY_RXTX_0_P	SFP PHY	CFP PHY	CFP_PHY_RXTX_0_P A9 USBC2_R2D_CR_P<1> GND_VOID=TRUE OUT 70
81	USBC_ATC2_D2R_TC_N<1>	GND_VOID=TRUE	N9	SFP_PHY_RXTX_0_N			CFP_PHY_RXTX_0_N B9 USBC2_R2D_CR_N<1> GND_VOID=TRUE OUT 70
81	USBC_ATC2_D2R_TC_P<2>	GND_VOID=TRUE	P5	SFP_PHY_RXTX_2_P			CFP_PHY_RXTX_2_P A5 USBC2_R2D_CR_P<2> GND_VOID=TRUE OUT 70
81	USBC_ATC2_D2R_TC_N<2>	GND_VOID=TRUE	N5	SFP_PHY_RXTX_2_N			CFP_PHY_RXTX_2_N B5 USBC2_R2D_CR_N<2> GND_VOID=TRUE OUT 70
81	USBC_ATC2_R2D_T_P<1>	GND_VOID=TRUE	P7	SFP_PHY_RXTX_1_P			CFP_PHY_RXTX_1_P A7 USBC2_D2R_P<1> GND_VOID=TRUE BI 70
81	USBC_ATC2_R2D_T_N<1>	GND_VOID=TRUE	N7	SFP_PHY_RXTX_1_N			CFP_PHY_RXTX_1_N B7 USBC2_D2R_N<1> GND_VOID=TRUE BI 70
81	USBC_ATC2_R2D_T_P<2>	GND_VOID=TRUE	P3	SFP_PHY_RXTX_3_P			CFP_PHY_RXTX_3_P A3 USBC2_D2R_P<2> GND_VOID=TRUE BI 70
81	USBC_ATC2_R2D_T_N<2>	GND_VOID=TRUE	N3	SFP_PHY_RXTX_3_N			CFP_PHY_RXTX_3_N B3 USBC2_D2R_N<2> GND_VOID=TRUE BI 70
95 82 BI	USBC_ATC2_AUX_C_P		L4	SFP_LPDP_AUX_P			CFP_LPDP_AUX_P D4 USBC2_AUX_P BI 82
95 82 BI	USBC_ATC2_AUX_C_N		M4	SFP_LPDP_AUX_N			CFP_LPDP_AUX_N C4 USBC2_AUX_N TR 82
89 81 IN	CIO_ATC2_LSTX		G1	USB4_SFP_SB_RX			USB4_CFP_SB_RX F1 USBC2_CIO_LSRX IN 86
89 81 OUT	CIO_ATC2_LSRX		G2	USB4_SFP_SB_TX			USB4_CFP_SB_TX E1 USBC2_CIO_LSTX BI 86
							USB4_CFP_SB_TX_DIR H1 ATCRTMR2_LSTX_DIR OUT 86
81	ATCRTMR2_SFP_RCAL_POS		M8	SFP_PHY_RCAL_P			CFP_PHY_RCAL_P C8 ATCRTMR2_CFP_RCAL_POS 81
81	ATCRTMR2_SFP_RCAL_NEG		L8	SFP_PHY_RCAL_N			CFP_PHY_RCAL_N D8 ATCRTMR2_CFP_RCAL_NEG 81
83 IN	ATCRTMR2_CHIPID_0		M1	CHIP_ID_0	GPIO	PERIPHERAL	
83 IN	ATCRTMR2_CHIPID_1		N1	CHIP_ID_1			
83 IN	ATCRTMR2_BOOT_CONFIG0		H2	BOOT_CONFIG0			
83 IN	ATCRTMR2_BOOT_CONFIG1		J1	BOOT_CONFIG1			
83 IN	ATCRTMR2_BOOT_CONFIG2		K1	BOOT_CONFIG2			
84 82 IN	ATCRTMR2_FORCE_DFU		C1	FORCE_DFU			
	TP_ATCRTMR2_GPIO0		K2	GPIO0			
	NC_ATCRTMR2_GPIO1	NO_TEST=1	L3	GPIO1			
	TP_ATCRTMR2_GPIO2		K3	GPIO2			
	TP_ATCRTMR2_GPIO3		L10	GPIO3			
							QSPI_CS* N11 SPI_ATCRTMR2_CS_L 81
							QSPI_SCLK M11 SPI_ATCRTMR2_CLK 81
							QSPI_DQ0 K10 SPI_ATCRTMR2_DIO<0> 81
							QSPI_DQ1 K11 SPI_ATCRTMR2_DIO<1> 81
							QSPI_DQ2 J9 SPI_ATCRTMR2_DIO<2> 81
							QSPI_DQ3 J11 SPI_ATCRTMR2_DIO<3> 81
							I2C0_SCL C2 I2C_ATCRTMR_SCL IN 148
							I2C0_SDA D3 I2C_ATCRTMR_SDA BI 148
							I2C1_SCL E2 I2C_UPC2_ATCRTMR2_SCL_1V2 IN 89
							I2C1_SDA D2 I2C_UPC2_ATCRTMR2_SDA_1V2 BI 89
							I2C1_INT B1 INT_I2C_UPC2_ATCRTMR2_L OUT 82 84
83 IN	ATCRTMR2_COLD_RESET_L		L2	COLD_RESET*	CLOCKS AND RESET	TEST AND DEBUG	TESTMODE L9 ATCRTMR2_TESTMODE 81
83 IN	ATCRTMR2_CFSB		M2	CFSB			JTAG_SEL C11 ATCRTMR2_JTAGL_SEL 81
81	ATCRTMR2_XTAL24M_IN		F11	XI0			JTAG_TCK B11 SWD_NUB_ATCRTMR1_SWCLK BI 148
81	ATCRTMR2_XTAL24M_OUT		E11	XO0			JTAG_TMS D10 SWD_NUB_ATCRTMR1_SWDIO BI 148
							JTAG_TDI D9 TP_ATCRTMR2_JTAG_TDI
							JTAG_TDO C10 ATCRTMR2_JTAG_TDO 81
							JTAG_TRST* E10 TP_ATCRTMR2_JTAG_TRESET
							ANALOGMUX_OUT F9 TP_ATCRTMR2_ANALOGMUX_OUT
							TST_CLKOUT M10 TP_ATCRTMR2_TST_CLKOUT
							TST_CLK_LVDS_0_P H10 NC_ATCRTMR2_CLK_LVDS_P<0> NO_TEST=1
							TST_CLK_LVDS_0_N H11 NC_ATCRTMR2_CLK_LVDS_N<0> NO_TEST=1
							TST_CLK_LVDS_1_P G11 NC_ATCRTMR2_CLK_LVDS_P<1> NO_TEST=1
							TST_CLK_LVDS_1_N G10 NC_ATCRTMR2_CLK_LVDS_N<1> NO_TEST=1

RG097 33 1/20W 5% TK 0201 81 SPI_ATCRTMR2_DIO<0> SPI_ATCRTMR2_R_DIO<0> 81

RG098 33 1/20W 5% TK 0201 81 SPI_ATCRTMR2_DIO<1> SPI_ATCRTMR2_R_DIO<1> 81

PP1V2_ATCRTMR2_VDDIO 141

RG090 3.3K 5% 1/20W TK 0201

NOSTUFF RG091 3.3K 5% 1/20W TK 0201

NOSTUFF RG092 3.3K 5% 1/20W TK 0201

NOSTUFF RG093 3.3K 5% 1/20W TK 0201

CG090 1UF 10% 6.3V CERM 402

OMIT_TABLE CRITICAL 998-22093

UG090 64MBIT-1.2V W25Q64NE XSON

81	SPI_ATCRTMR2_CLK	RG094 33 1/20W 5% TK 0201	SPI_ATCRTMR2_CLK_R	6 CLK
81	SPI_ATCRTMR2_DIO<2>	RG095 33 1/20W 5% TK 0201	SPI_ATCRTMR2_CS_L	1 CS*
			SPI_ATCRTMR2_R_DIO<2>	3 WP*(IO2)
81	SPI_ATCRTMR2_DIO<3>	RG096 33 1/20W 5% TK 0201	SPI_ATCRTMR2_R_DIO<3>	7 HOLD*(IO3)

DI(IO0) 5 SPI_ATCRTMR2_R_DIO<0> 81

DO(IO1) 2 SPI_ATCRTMR2_R_DIO<1> 81

GND 4 EPAD 9

47K RG047 5% 0201 TK 1/20W ATCRTMR2_JTAGL_SEL 81

10K RG040 5% 1/20W TK 0201 ATCRTMR2_TESTMODE 81

47K RG043 5% 1/20W TK 0201 CIO_ATC2_LSTX 81 89

47K RG044 5% 1/20W TK 0201 CIO_ATC2_LSRX 81 89

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C: High Speed ATC2

Apple Inc.

DRAWING NUMBER 051-08156 SIZE D

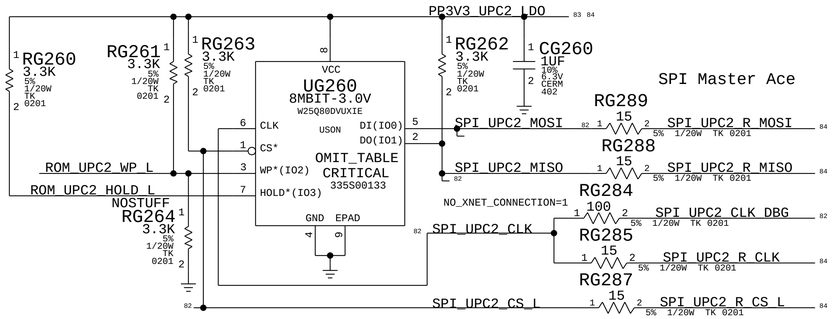
REVISION 3.0.0

BRANCH evt-1

PAGE 160 OF 700

SHEET 81 OF 159

*** OK2PLACE ***



ACE ARKANOID CONN

JG200 — USBC_DBG — 505070-1222 — M-ST-SM — PACK_OPTION=KEEP_SMALL_ARKANOID_CONN

SMC			SOC
ATCRTMR2_FORCE_DFU	1	2	UPC_I2C_INT_L
I2C_SMC_UPC_SCL	3	4	I2C_UPC_SDA
I2C_SMC_UPC_SDA	5	6	I2C_UPC_SCL
UPC_SMC_I2C_INT_L	7	8	UPC2_SER_DBG
SPI_UPC2_CLK_DBG	9	10	DP2HDMI_RESET_R_L
I2C_HDMI_DEBUG_SDA	11	12	I2C_HDMI_DEBUG_SCL

BRIDGE ARKANOID CONN

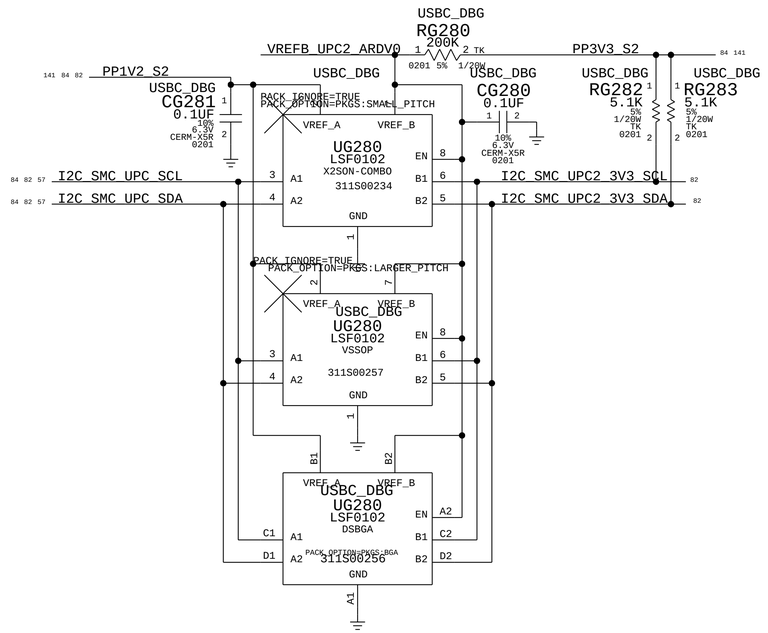
JG201 — USBC_DBG — 505070-1222 — M-ST-SM — PACK_OPTION=KEEP_SMALL_ARKANOID_CONN

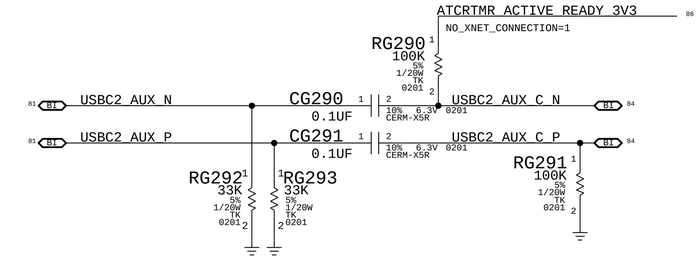
ATCRTMR2_RESET_L	1	2	INT_I2C_UPC2_ATCRTMR2_L
UPC2_ATCRTMR2_PWR_EN	3	4	I2C_UPC2_ATCRTMR2_SCL
PP1V2_ATCRTMR2_VDDIO	5	6	I2C_UPC2_ATCRTMR2_SDA
PP0V855_ATCRTMR2_VDD_CIO	7	8	HDMI_HPD_IN
UART_DP2HDMI_D2R	9	10	DPRX_INT_HPD
DPRX_AUX_P	11	12	DPRX_AUX_N

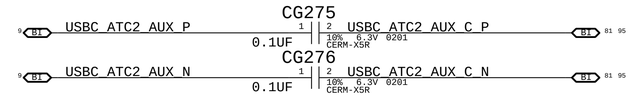
AARDVARKANOID CONN

JG202 — USBC_DBG — 505070-1222 — M-ST-SM — PACK_OPTION=KEEP_SMALL_ARKANOID_CONN

PP1V2_S2	1	2	SPI_UPC2_CS_L
SWD_UPC_SWDIO1	3	4	SPI_UPC2_CLK
SWD_UPC_SWCLK0	5	6	SPI_UPC2_MOSI
SPI_UPC2_MISO	7	8	HDMI_DDC_5V_SDA
I2C_SMC_UPC2_3V3_SDA	9	10	HDMI_DDC_5V_SCL
I2C_SMC_UPC2_3V3_SCL	11	12	PP1V2_S2







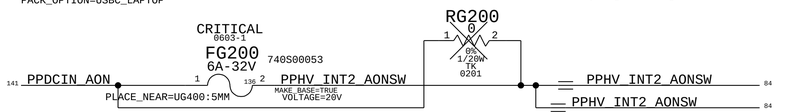
HV POWER ALIASES

Fuses for laptop charging.

PACK_OPTION=USBC_LAPTOP

PACK_IGNORE=TRUE
PACK_OPTION=USBC_DESKTOP

Desktops only need connection for programming OTP.



PPVBUS_USBC2 — MAKE_BASE=TRUE — PPVBUS_USBC2

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: Support 1 ATC2

Apple Inc.

DRAWING NUMBER: 051-08156 | SIZE: D
REVISION: 3.0.0
BRANCH: evt-1
PAGE: 162 OF 700
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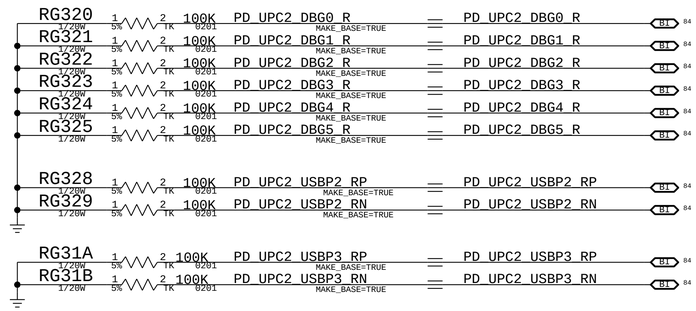
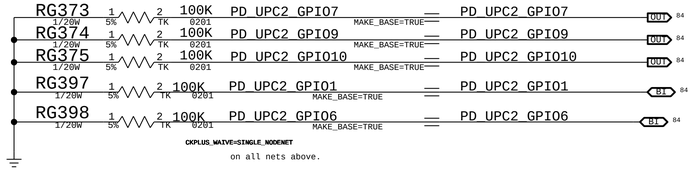
*** OK2PLACE ***

Ace 2 unused GPIOs and Ports



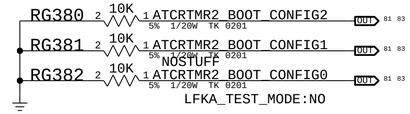
Ace2 GPIOs

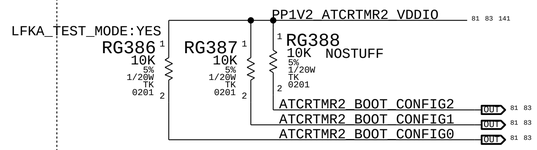


CKPLUS_WAIVE=SINGLE_NODENET
on all nets above.

ATCRTMR Boot Config

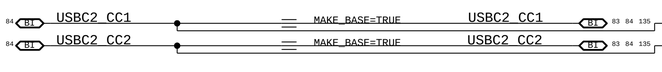
[2:0] = [011] 30Mhz QSPI and Test Mode Enabled
POR config should be [010] Test Mode Disabed





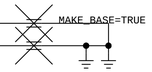
Connections for Laptops (USBC power in)

PACK_OPTION=USBC_LAPTOP

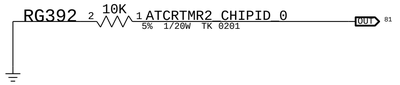


Connections for Desktops (No USBC power in)

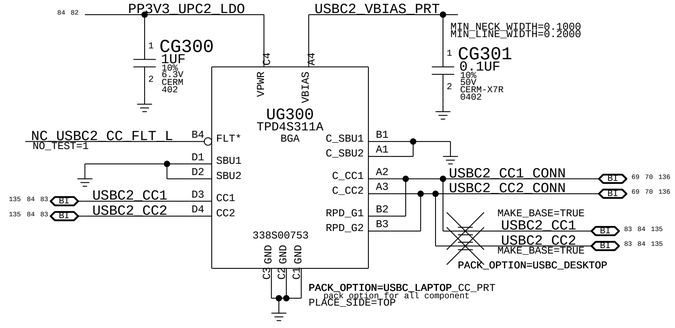
PACK_OPTION=USBC_DESKTOP



ATCRTMR0 CHIP 0X2

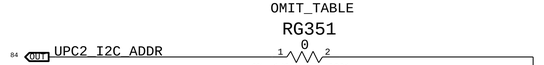


USBC0 PP_CABLE Protection

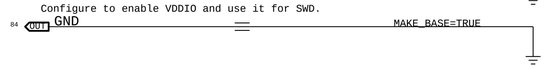


ATC0: I2C_ADDR=GND, I2CM_*_CNFG=1M\u03a9 3V3_LDO_X pull-ups
ATC1: I2C_ADDR=Float, I2CM_*_CNFG=1M\u03a9 3V3_LDO_X pull-ups
ATC2: I2C_ADDR=GND, I2CM_*_CNFG=1M\u03a9 pull-downs
ATC3: I2C_ADDR=Float, I2CM_*_CNFG=1M\u03a9 pull-downs

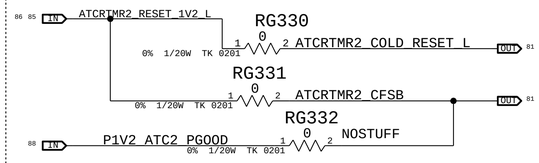
OMIT_TABLE



Configure to enable VDDIO and use it for SWD.



Is UPCx_5V_EN being used?



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00073	1	RES,TK,0 OHM,1A MAX,1/20W,0201	RG351	CRITICAL	ACE_WILL_BE_OTPED:YES
118S00466	1	RES,TK,140KOHM,1%,1/20W,0201	RG351	CRITICAL	ACE_WILL_BE_OTPED:NO

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: Support 2 ATC2

Apple Inc.

DRAWING NUMBER: 051-08156 SIZE: D
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*** OK2INTEGRATE ***

ACE BOM_OPTION NOTES: The BOM_OPTIONs are meant to resolve ACE I2C address conflict when ACEs do not go through the OTP flow. It can happen at early P0 local builds or even at factory builds when the stations are not brought up

PP3V3_UPC2_LDO 82 83 84

ACE_WILL_BE_OTPED:NO
ACE_WILL_BE_OTPED:NO

RG410 20.5K 0201 1% 1/20W TK
RG411 20.5K 0201 1% 1/20W TK

Internal Pull-ups Enabled after reading straps

RG409 470K 5% 1/20W TK 0201 I2C_UPC2_ATCRTMR2_SCL 82 84 86 136 147 CKPLUS_WAIVE=I2C_PULLUP
RG408 470K 5% 1/20W TK 0201 I2C_UPC2_ATCRTMR2_SDA 82 84 86 136 147 CKPLUS_WAIVE=I2C_PULLUP

ACE_WILL_BE_OTPED:YES
ACE_WILL_BE_OTPED:YES

RG405 1M 5% 1/20W TK 0201 PD_UART_UPC2_RX_TX 84
RG406 100K 5% 1/20W TK 0201 PD_UPC2_MRESET 84
RG407 100K 5% 1/20W TK 0201 PD_UPC2_HPD 84
Formerly Mistakenly RG507
RG412 0 0% 1/20W TK 0201 PD_UPC2_HRESET 84

Either a Testpoint or Arkanoid connector must be present for GPI0 (EVEN IN PRODUCTION)

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

CRITICAL RG403 15K 0.1% 1/20W TK 0201

GND_I2C_ADDR PRIMARY ONLY

PPHV_INT2_AONSW 82

MAX 100uF TOTAL ON RAIL

PP5V_S2SW_USBC23 142
PP5V_S2SW_USBC23 142

138S00070 CG406 4.7UF 20% 25V X5R 0402

PP_5V0 PP_CABLE PP_HV VBUS

UG400 CD3217B12GACER FCBGA
353S02742 CRITICAL OMIT_TABLE

	PD_UPC2_HRESET	B13	HRESET	
84	PD_UPC2_MRESET	A14	MRESET	
136 86 82 OUT	ATCRTMR2_RESET_L	B17	RESET*	3V3
136 82 OUT	UPC2_SER_DBG	A2	GPIO0	
		B1		
83 OUT	PD_UPC2_GPIO1	D1	GPIO1	
82 81 IN	INT_I2C_UPC2_ATCRTMR2_L	F1	GPIO2	1V2
136 87 83 OUT	UPC23_5V_EN	C2	GPIO3	3V3
82 81 OUT	ATCRTMR2_FORCE_DFU	E2	GPIO4	1V2
89 OUT	UPC2_CHGR_AUX_DET_SHORT	B3	GPIO5	3V3
83 IN	PD_UPC2_GPIO6	C4	GPIO6	DIGITAL CORE I/O & CONTROL
83 OUT	PD_UPC2_GPIO7	D3	GPIO7	
140 138 136 76 75 45 OUT	UPC_PMU_RESET_1V2_R	E4	GPIO8	1V2
83 IN	PD_UPC2_GPIO9	F3	GPIO9	
83 OUT	PD_UPC2_GPIO10	F7	GPIO10	
	GND	A18	BUSPOWER	
83	UPC2_I2C_ADDR	M19	I2C_ADDR	IPU-BOOT
	UPC2_R_OSC	M21	R_OSC	
147 136 86 84 82 BI	I2C_UPC2_ATCRTMR2_SDA	A16	I2CM_SDA_CNFG	IPU-AFTER-BOOT
147 136 86 84 82 BI	I2C_UPC2_ATCRTMR2_SCL	B15	I2CM_SCL_CNFG	IPU-AFTER-BOOT
82 56 BI	I2C_UPC_SDA	B5	I2C_SDA1	
82 56 BI	I2C_UPC_SCL	A4	I2C_SCL1	
82 56 OUT	UPC_I2C_INT_L	D7	I2C_IRQ1*	
82 57 BI	I2C_SMC_UPC_SDA	B7	I2C_SDA2	
82 57 BI	I2C_SMC_UPC_SCL	A6	I2C_SCL2	
82 57 OUT	UPC_SMC_I2C_INT_L	C8	I2C_IRQ2*	
82 OUT	SPI_UPC2_R_CLK	B9	SPI_CLK	
82 OUT	SPI_UPC2_R_MOSI	B11	SPI_MOSI	
82 IN	SPI_UPC2_R_MISO	A10	SPI_MISO	
82 OUT	SPI_UPC2_R_CS_L	A8	SPI_SSZ	
89 82 BI	SWD_UPC_SWDIO1	E20	SWD_DATA	IPU
89 82 BI	SWD_UPC_SWCLK0	E16	SWD_CLK	IPU
84	PD_UART_UPC2_RX_TX	B19	UART_RX	
		A20	UART_TX	
89 BI	USB2_UPC2_P1_P	H19	USB_RP1_P	
89 BI	USB2_UPC2_P1_N	H21	USB_RP1_N	
83 BI	PD_UPC2_USBP2_RP	G20	USB_RP2_P	
83 BI	PD_UPC2_USBP2_RN	G22	USB_RP2_N	
83 BI	PD_UPC2_USBP3_RP	F19	USB_RP3_P	
83 BI	PD_UPC2_USBP3_RN	F21	USB_RP3_N	
82 BI	USBC2_AUX_C_P	J12	AUX_P	
82 BI	USBC2_AUX_C_N	H11	AUX_N	
84	PD_UPC2_HPD	C12	HPD	
83 IN	PD_UPC2_DBG0_R	G12	DEBUG0	
83 OUT	PD_UPC2_DBG1_R	F11	DEBUG1	
83 OUT	PD_UPC2_DBG2_R	E8	DEBUG2	
83 BI	PD_UPC2_DBG3_R	E12	DEBUG3	
83 IN	PD_UPC2_DBG4_R	G16	DEBUG4	
83 OUT	PD_UPC2_DBG5_R	F15	DEBUG5	
86 BI	USBC2_CIO_LSTX_3V3	D15	DEBUG6	
86 OUT	USBC2_CIO_LSRX_3V3	D19	DEBUG7	

PORT_MUX

POWER

TYPE-C

GND

VIN_3V3	C20		
VDDIO	A12		
VDDIO_CFG	D11	GND	83
LDO_3V3	C22		
	D21		
VIN_LV	L20		
VOUT_LV	L18		
VRET	C16		
SS	L22	UPC2_SS	
LDO_CORE	E22	PP1V5_UPC2_LDO_CORE	
VBUS_OPT	D5	PPVBUS_USBC2	82
PP_HV_OPT	F5	PPHV_INT2_AONSW	82
C_CC1	M15	USBC2_CC1	
	N16		
C_CC2	M17	USBC2_CC2	
	N18		
RPD_G1	L14	USBC2_CC1	BI 83
RPD_G2	L16	USBC2_CC2	BI 83
C_USB_TP	K19	USBC2_USB_TOP_P	BI 69 70
C_USB_TN	K21	USBC2_USB_TOP_N	BI 69 70
C_USB_BP	J20	USBC2_USB_BOT_P	BI 69 70
C_USB_BN	J22	USBC2_USB_BOT_N	BI 69 70
C_SBU1	J16	USBC2_SBU1	BI 69 70 136
C_SBU2	H15	USBC2_SBU2	BI 69 70 136

GND_OPT C18
GND_OPT E18
GND_OPT D17
GND_OPT G18

GND
A22 H9 N20 B21 K15 N22

PPVBUS_USBC2 69 70 82 135 136
CG401 1UF 10% 35V X5R 0402
CRITICAL DG400 X3-WLB1608 SDM2U40CSPN-_-55

PP3V3_S2 82 141
CG400 10UF 20% 6.3V CERM 0402

PP1V2_S2 82 141
CG402 1.0UF 20% 6.3V X5R 0201-1

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V
PP3V3_UPC2_LDO 82 83 84
CG408 10UF 20% 6.3V CERM 0402

PP1V8_S2 141
CG403 0.1UF 10% 6.3V CERM-X5R 0201

UPC2_ATCRTMR2_PWR_EN 82 86
(cap needed when used as power source)

PACK_OPTION=ACE2_SS_CAP
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
CG409 0.68UF 5% 6.3V X6S 0402
CG405 10UF 20% 6.3V CERM 0402
PACK_OPTION=ACE2_SS_GND
GND
MAKE_BASE=TRUE

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
BI 83 135
CG414 220PF 5% 50V C0G 0201-1
CG413 220PF 5% 50V C0G 0201-1

BOM_COST_GROUP=USB-C

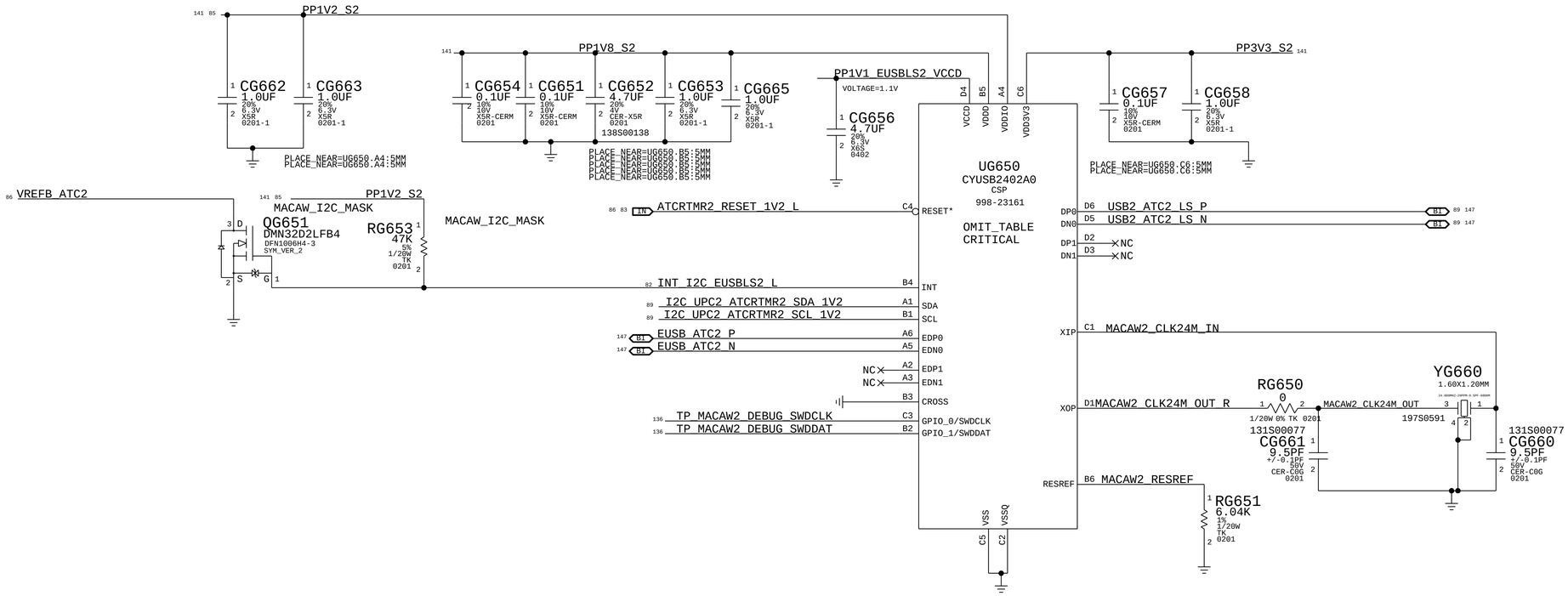
PAGE TITLE: USB-C: Port Controller ATC2

Apple Inc.

DRAWING NUMBER: 051-08156
SIZE: D
REVISION: 3.0.0
BRANCH: evt-1
PAGE: 164 OF 700
SHEET: 84 OF 159

*** OK2INTEGRATE ***

MACAW 2



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: USB2 RPT2

Apple Inc.

DRAWING NUMBER 051-08156
SIZE D
REVISION 3.0.0
BRANCH evt-1
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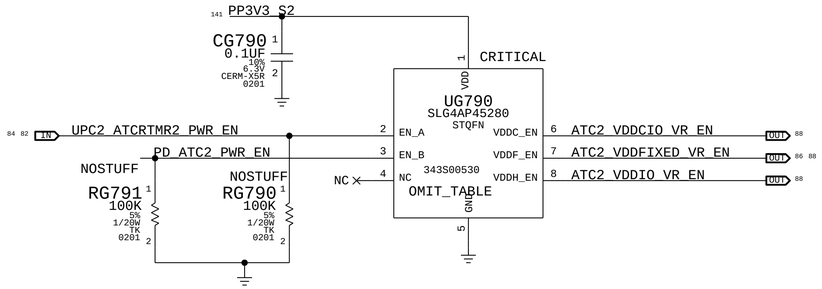
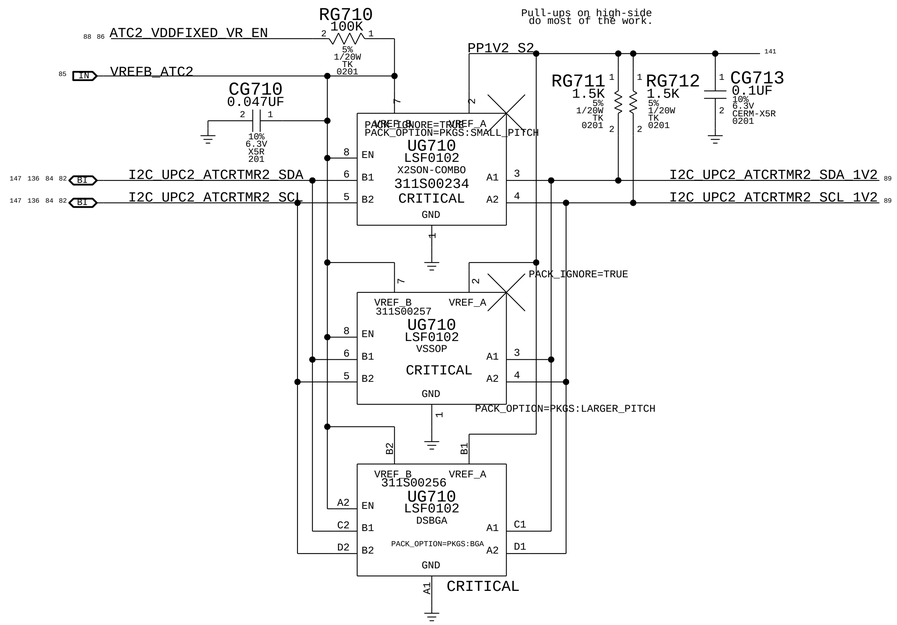
*** OK2INTEGRATE ***

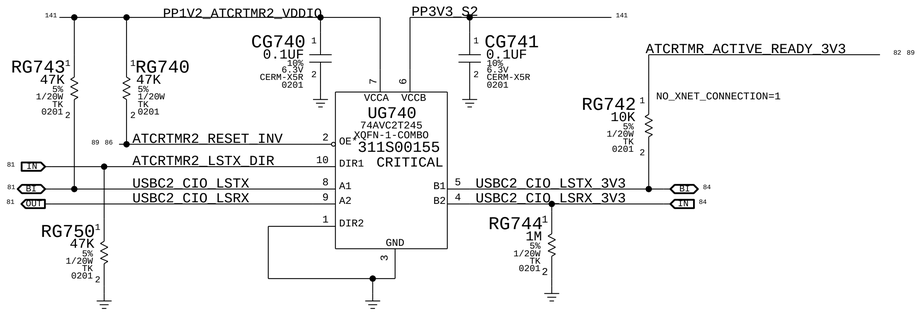
Sequencing Requirements: 3.3V to UG790 --> system 1.2V (UG710) same time or before system 1.8V (UG400 VIN_LV pin)

The 3.3V needs to be HIGH before VIN_LV of Aces

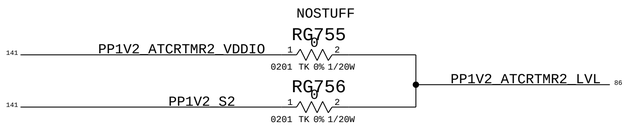


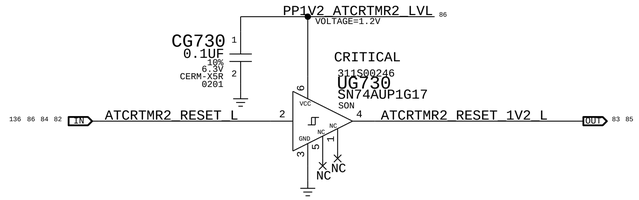
ATC2 RE-TIMER I2C LEVEL SHIFTERS

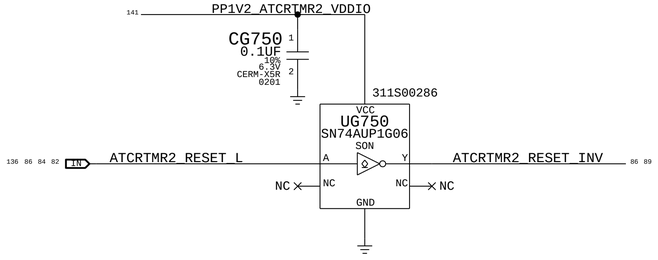




ATC2 AND MACAW RESET LEVEL SHIFTERS







BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: HS Level Shifters ATC2

Apple Inc.

DRAWING NUMBER: 051-08156 | SIZE: D
REVISION: 3.0.0
BRANCH: evt-1
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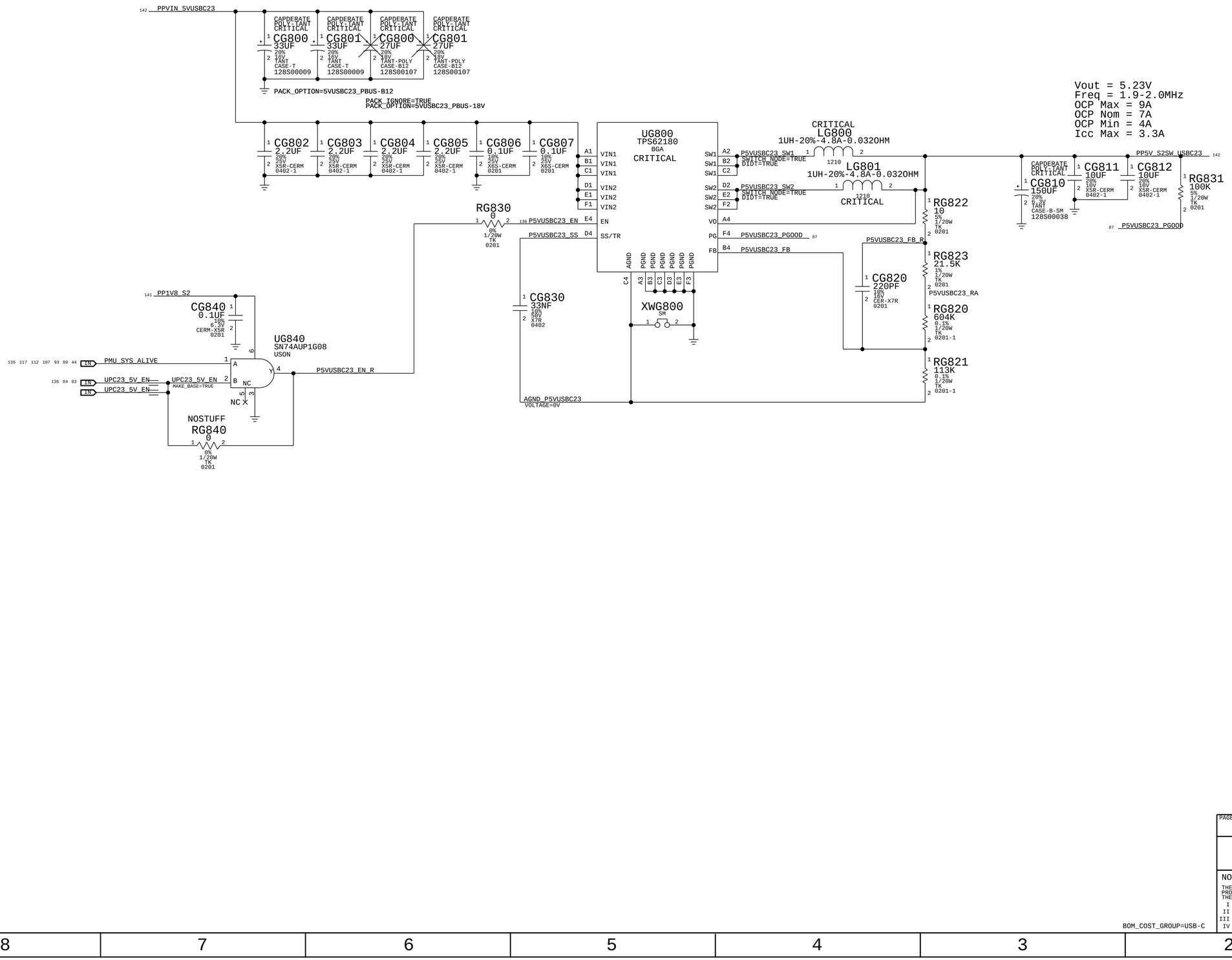
SHEET: 86 OF 159

*** OK2INTEGRATE ***

Set one option for the PBUS caps

PACK_OPTION=5VUSBC23_PBUS-B12

PACK_OPTION=5VUSBC23_PBUS-18V



BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: 5V Regulator

Apple Inc.

DRAWING NUMBER: 051-08156 SIZE: D

REVISION: 3.0.0

BRANCH: evt-1

PAGE: 168 OF 700

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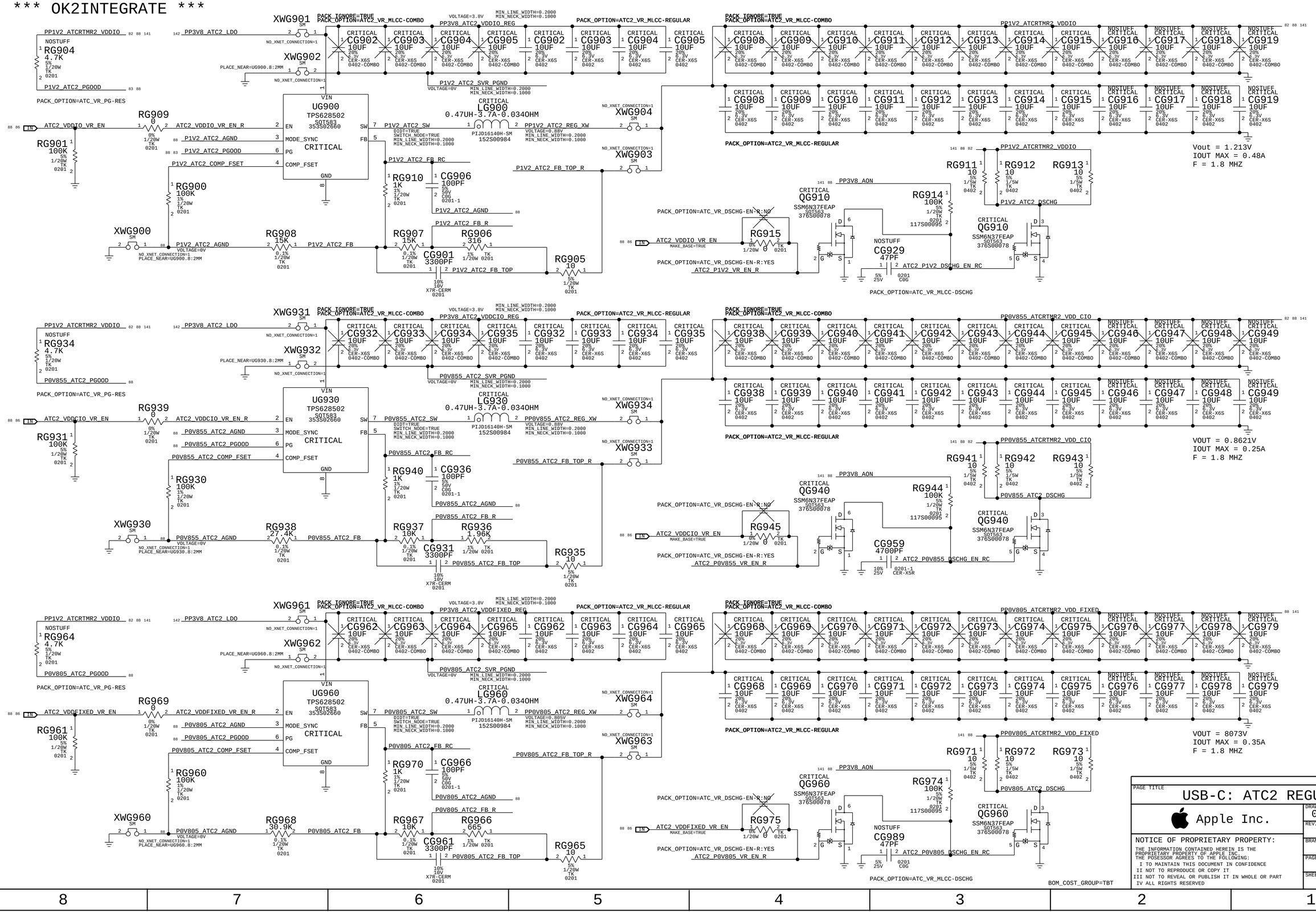
*** OK2INTEGRATE ***



PAGE TITLE

USB-C: ATC2 REGULATORS

Apple Inc.

DRAWING NUMBER	051-08156
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BRANCH	evt-1
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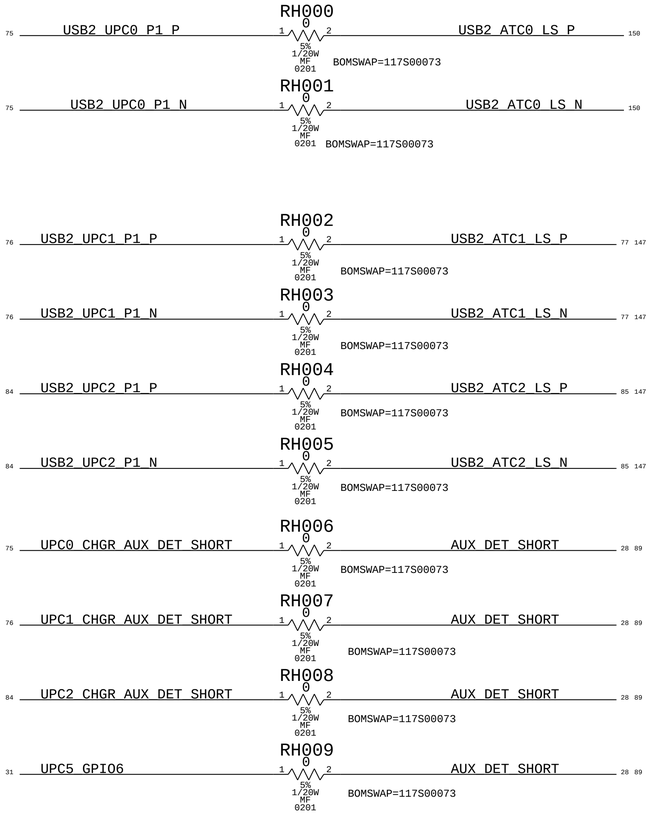
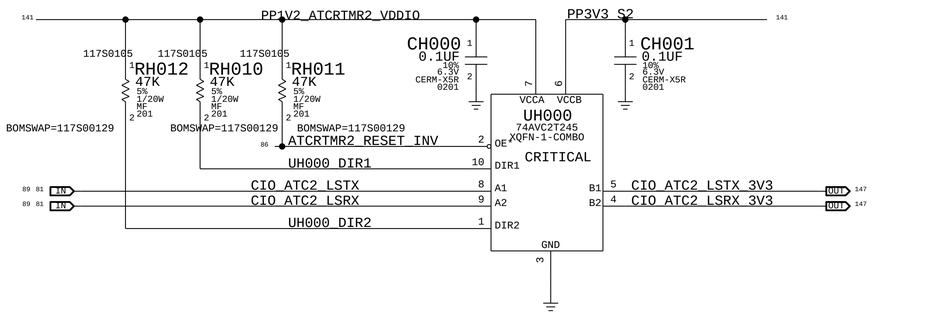
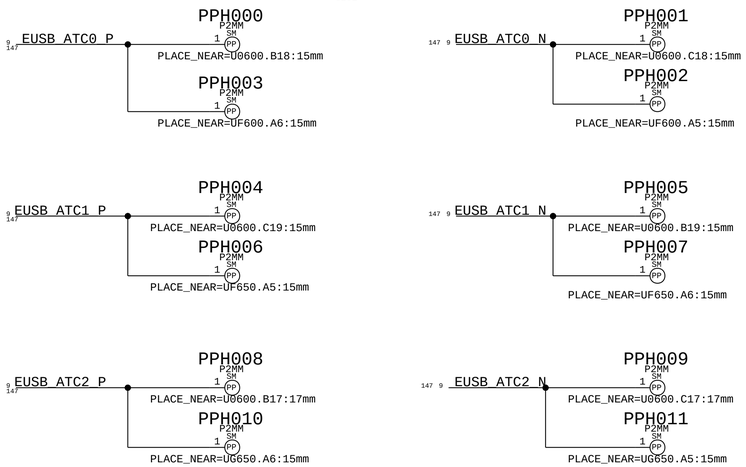
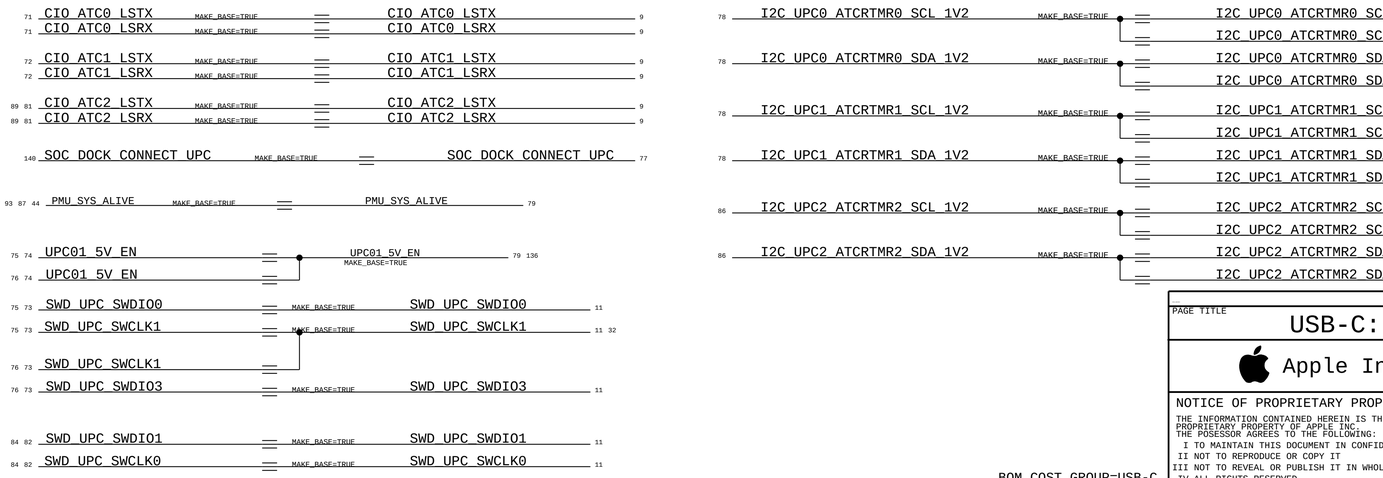
LEVEL SHIFTER FOR COLUMBUS









BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: SUPPORT

Apple Inc.

DRAWING NUMBER 051-08156 | SIZE D
REVISION 3.0.0
BRANCH evt-1
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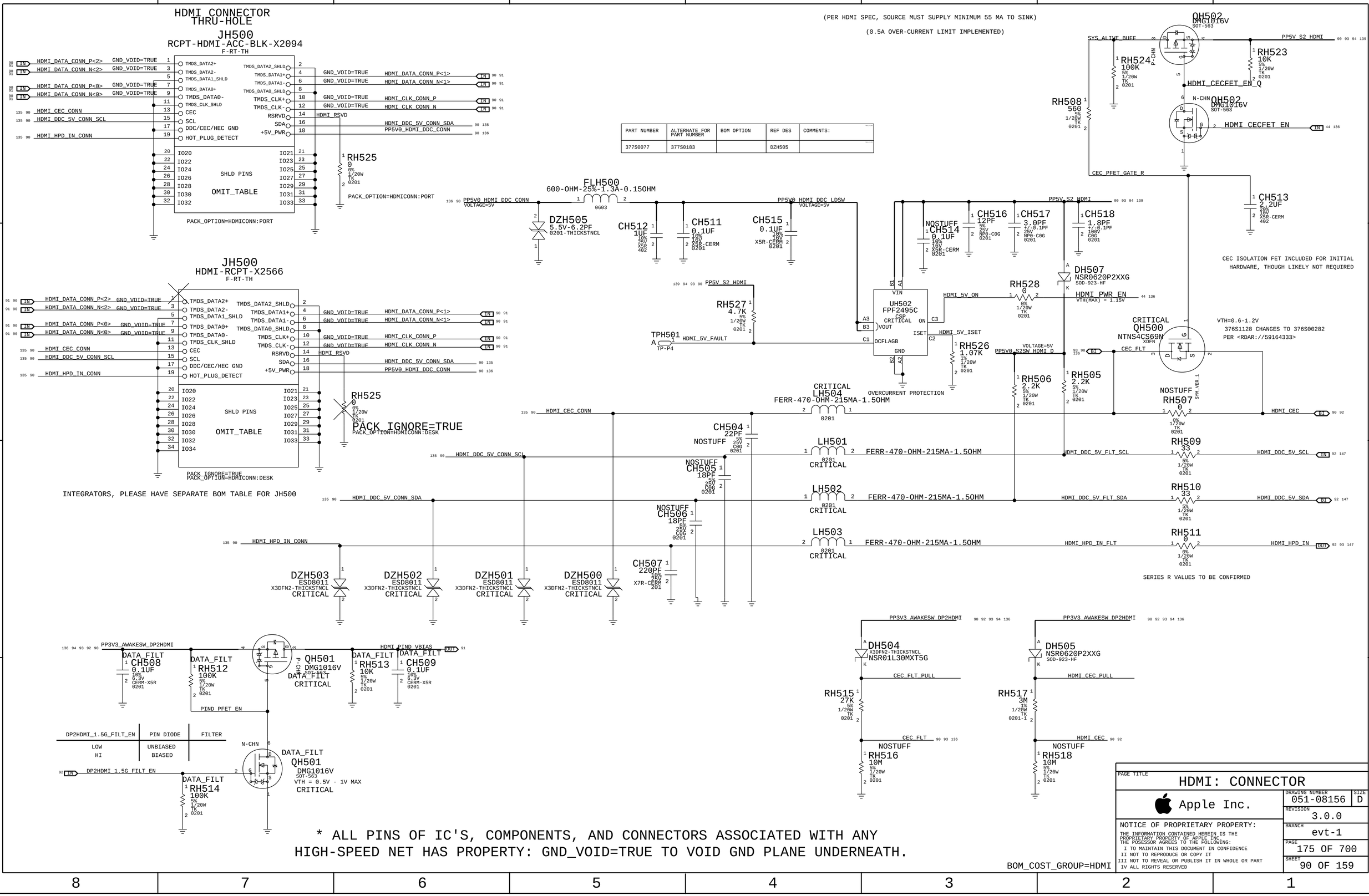
HDMI CONNECTOR
THRU-HOLE
JH500
RCPT-HDMI-ACC-BLK-X2094
F-RT-TH
HDMI_DATA_CONN_P<2>
HDMI_DATA_CONN_N<2>
HDMI_DATA_CONN_P<0>
HDMI_DATA_CONN_N<0>
HDMI_CEC_CONN
HDMI_DDC_5V_CONN_SCL
HDMI_HPD_IN_CONN
TMDS_DATA2+
TMDS_DATA2-
TMDS_DATA1_SHLD
TMDS_DATA0+
TMDS_DATA0-
TMDS_CLK_SHLD
CEC
SCL
DDC/CEC/HEC GND
HOT_PLUG_DETECT
TMDS_DATA2_SHLD
TMDS_DATA1+
TMDS_DATA1-
TMDS_DATA0_SHLD
TMDS_CLK+
TMDS_CLK-
RSRVD
SDA
+5V_PWR
IO20
IO22
IO24
IO26
IO28
IO30
IO32
IO21
IO23
IO25
IO27
IO29
IO31
IO33
SHLD PINS
OMIT_TABLE
PACK_OPTION=HDMICONN:PORT
RH525
0
0%
1/20W
TK
0201
PACK_OPTION=HDMICONN:PORT
(PER HDMI SPEC, SOURCE MUST SUPPLY MINIMUM 55 MA TO SINK)
(0.5A OVER-CURRENT LIMIT IMPLEMENTED)
QH502
DMG1016V
SOT-563
SYS_ALIVE_BUFF
PP5V_S2_HDMI
RH524
100K
P-CHN
RH523
10K
HDMI_CECFET_EN_Q
RH508
560
N-CHN
QH502
HDMI_CECFET_EN
CEC_PFET_GATE_R
CH513
2.2UF
PART NUMBER
ALTERNATE FOR PART NUMBER
BOM OPTION
REF DES
COMMENTS:
377S0077
377S0183
DZH505
FLH500
600-OHM-25%-1.3A-0.15OHM
0603
PP5V0_HDMI_DDC_CONN
VOLTAGE=5V
PP5V0_HDMI_DDC_LDSW
DZH505
5.5V-6.2PF
0201-THICKSTNCL
CH512
1UF
CH511
0.1UF
CH515
0.1UF
NOSTUFF
CH514
0.1UF
CH516
12PF
CH517
3.0PF
CH518
1.8PF
DH507
NSR0620P2XXG
SOD-923-HF
HDMI_PWR_EN
VTH(MAX) = 1.15V
CEC ISOLATION FET INCLUDED FOR INITIAL
HARDWARE, THOUGH LIKELY NOT REQUIRED
JH500
HDMI-RCPT-X2566
F-RT-TH
RH525
0
PACK_IGNORE=TRUE
PACK_OPTION=HDMICONN:DESK
PACK_IGNORE=TRUE
PACK_OPTION=HDMICONN:DESK
INTEGRATORS, PLEASE HAVE SEPARATE BOM TABLE FOR JH500
PP5V_S2_HDMI
RH527
4.7K
TPH501
TP-P4
HDMI_5V_FAULT
UH502
FPF2495C
CSP
CRITICAL
VIN
VOUT
OCFLAGB
ON
ISET
GND
HDMI_5V_ON
HDMI_5V_ISET
RH528
0
RH526
1.07K
OVERCURRENT PROTECTION
CRITICAL
QH500
NTNS4CS69N
XDFN
VTH=0.6-1.2V
376S1128 CHANGES TO 376S00282
PER <RDAR://59164333>
CEC_FLT
VOLTAGE=5V
PP5V0_S2SW_HDMI_D
RH506
2.2K
RH505
2.2K
NOSTUFF
RH507
0
SYM_VER_1
HDMI_CEC
RH509
33
RH510
33
RH511
0
HDMI_DDC_5V_FLT_SCL
HDMI_DDC_5V_FLT_SDA
HDMI_HPD_IN_FLT
HDMI_DDC_5V_SCL
HDMI_DDC_5V_SDA
HDMI_HPD_IN
SERIES R VALUES TO BE CONFIRMED
LH504
FERR-470-OHM-215MA-1.5OHM
LH501
LH502
LH503
CH504
22PF
CH505
18PF
CH506
18PF
CH507
220PF
DZH503
DZH502
DZH501
DZH500
ESD8011
X3DFN2-THICKSTNCL
CRITICAL
PP3V3_AWAKESW_DP2HDMI
QH501
DMG1016V
SOT-563
DATA_FILT
CH508
0.1UF
RH512
100K
RH513
10K
CH509
0.1UF
PIND_PFET_EN
HDMI_PIND_VBIAS
DP2HDMI_1.5G_FILT_EN
PIN DIODE
FILTER
LOW
HI
UNBIASED
BIASED
RH514
100K
VTH = 0.5V - 1V MAX
DH504
NSR01L30MXT5G
CEC_FLT_PULL
RH515
27K
RH516
10M
DH505
NSR0620P2XXG
HDMI_CEC_PULL
RH517
3M
RH518
10M
* ALL PINS OF IC'S, COMPONENTS, AND CONNECTORS ASSOCIATED WITH ANY
HIGH-SPEED NET HAS PROPERTY: GND_VOID=TRUE TO VOID GND PLANE UNDERNEATH.
BOM_COST_GROUP=HDMI
PAGE TITLE
HDMI: CONNECTOR
Apple Inc.
DRAWING NUMBER
051-08156
SIZE
D
REVISION
3.0.0
BRANCH
evt-1
PAGE
175 OF 700
SHEET
90 OF 159
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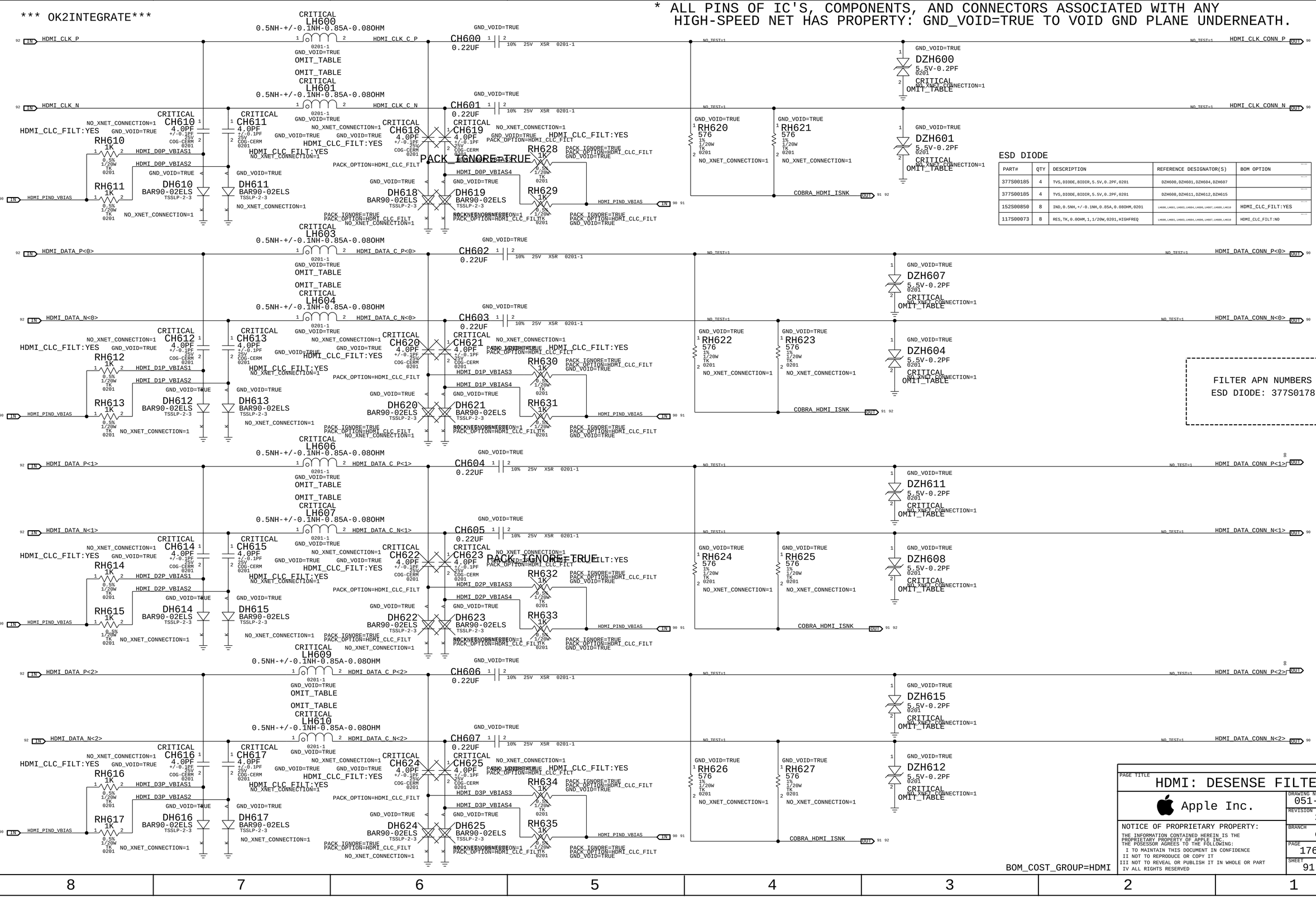
*** OK2INTEGRATE***

* ALL PINS OF IC'S, COMPONENTS, AND CONNECTORS ASSOCIATED WITH ANY HIGH-SPEED NET HAS PROPERTY: GND_VOID=TRUE TO VOID GND PLANE UNDERNEATH.



ESD DIODE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
377S00185	4	TVS,DIODE,BIDIR,5.5V,0.2PF,0201	DZH600,DZH601,DZH604,DZH607	
377S00185	4	TVS,DIODE,BIDIR,5.5V,0.2PF,0201	DZH608,DZH611,DZH612,DZH615	
152S00850	8	IND,0.5NH,+/-0.1NH,0.85A,0.08OHM,0201	LH600,LH601,LH603,LH604,LH606,LH607,LH609,LH610	HDMI_CLC_FILT:YES
117S00073	8	RES,TK,0.00HM,1,1/20W,0201,HIGHFREQ	LH600,LH601,LH603,LH604,LH606,LH607,LH609,LH610	HDMI_CLC_FILT:NO

FILTER APN NUMBERS
ESD DIODE: 377S0178

BOM_COST_GROUP=HDMI

PAGE TITLE: HDMI: DESENSE FILTERS

Apple Inc.

DRAWING NUMBER: 051-08156 | SIZE: D
REVISION: 3.0.0
BRANCH: evt-1
PAGE: 176 OF 700
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*** IN PROGRESS ***

RH780 0 5% 1/16W MF 0402 — PP3V3_AWAKESW_DP2HDMI (136 94 93 92 90) → PP3V3_DP2HDMI VOLTAGE=3.3V
BYPASS=CH753.1::5MM
CH753 10UF 20% 6.3V X5R 0402-8 — BYPASS=UH700.A6::5MM
CH721 1.8PF +/-0.1PF 100V C0G 0201 — BYPASS=UH700.A6::5MM
CH754 1.0UF 20% 6.3V X5R 0201-1 — BYPASS=UH700.A6::5MM
CH755 0.1UF 10% 6.3V CERM-X5R 0201 — BYPASS=UH700.B6::5MM
CH715 12PF 5% 25V NP0-C0G 0201
CH716 3.0PF +/-0.1PF 25V NP0-C0G 0201
92

RH781 0 5% 1/16W MF 0402 — PP1V2_AWAKESW_DP2HDMI (136 94) → PP1V2_DP2HDMI VOLTAGE=1.2V
BYPASS=CH722.1::5MM
CH720 1.8PF +/-0.1PF 100V C0G 0201
CH711 4.7UF 20% 4V CER-X5R 0201 — BYPASS=UH700.B3::5MM
CH712 0.1UF 10% 6.3V CERM-X5R 0201 — BYPASS=UH700.B3::5MM
CH722 10UF 20% 6.3V X5R 0402-8 — BYPASS=UH700.L6::5MM
CH737 4.7UF 20% 4V CER-X5R 0201 — BYPASS=UH700.L7::5MM
CH751 0.1UF 10% 6.3V CERM-X5R 0201 — BYPASS=UH700.L6::5MM
CH739 12PF 5% 25V NP0-C0G 0201
CH738 3.0PF +/-0.1PF 25V NP0-C0G 0201

CH726 0.1UF 10% 6.3V CERM-X5R 0201 — BYPASS=UH700.H3::5MM
CH780 12PF 5% 25V NP0-C0G 0201
CH781 3.0PF +/-0.1PF 25V NP0-C0G 0201
CH782 1.8PF +/-0.1PF 100V C0G 0201
CH741 0.1UF 10% 6.3V CERM-X5R 0201 — BYPASS=UH700.E6::5MM
CH746 2.2UF 20% 4V X6S-CERM 0201 — BYPASS=UH700.H4::5MM
CH747 2.2UF 20% 4V X6S-CERM 0201 — BYPASS=UH700.F6::5MM
CH732 0.1UF 10% 6.3V CERM-X5R 0201 — BYPASS=UH700.H6::5MM
CH731 2.2UF 20% 4V X6S-CERM 0201 — BYPASS=UH700.H6::5MM

PACK_OPTION=HDMI14UF:THICK
CH756 14UF 20% 4V X5R 0402-THICKSTNCL
CH745 14UF 20% 4V X5R 0402-THICKSTNCL
CH725 14UF 20% 4V X5R 0402-THICKSTNCL
CH727 14UF 20% 4V X5R 0402-THICKSTNCL
PACK_OPTION=HDMI14UF:NORM
CH756 14UF 20% 4V X5R 0402-D2X-1
CH745 14UF 20% 4V X5R 0402-D2X-1
CH725 14UF 20% 4V X5R 0402-D2X-1
CH727 14UF 20% 4V X5R 0402-D2X-1
PACK_IGNORE=TRUE
PACK_OPTION=HDMI14UF:NORM
PLACE_NEAR=UH700.F6::5MM
PLACE_NEAR=UH700.H3::5MM
PLACE_NEAR=UH700.F8::5MM
PLACE_NEAR=UH700.E6::5MM
BYPASS=UH700.H3::5MM
BYPASS=UH700.F8::5MM
BYPASS=UH700.F6::5MM
BYPASS=UH700.E6::5MM
FLH710 FERR-18-OHM-4A 0402 — PP0V95_AWAKESW_DP2HDMI (92 94 135)
CH729 14UF 20% 4V X5R 0402-D2X-1
CH748 0.1UF 10% 6.3V CERM-X5R 0201 — BYPASS=UH700.D9::5MM
CH723 0.1UF 10% 6.3V CERM-X5R 0201 — BYPASS=UH700.H9::5MM
CH724 1.0UF 20% 6.3V X5R 0201-1 — BYPASS=UH700.K9::5MM
CH728 1.0UF 20% 6.3V X5R 0201-1 — BYPASS=UH700.B9::5MM
PLACE_NEAR=CH728.1::5MM
PACK_IGNORE=TRUE
PACK_OPTION=HDMI14UF:NORM
PACK_OPTION=HDMI14UF:THICK
FLH711 FERR-18-OHM-4A 0402 — PP0V95_AWAKESW_DP2HDMI (92 94 135)
PLACE_NEAR=UH700.F9::5MM
CH749 0.1UF 10% 6.3V CERM-X5R 0201 — BYPASS=UH700.D2::5MM
CH733 0.1UF 10% 6.3V CERM-X5R 0201 — BYPASS=UH700.H2::5MM
CH734 1.0UF 20% 6.3V X5R 0201-1 — BYPASS=UH700.K2::5MM
CH735 1.0UF 20% 6.3V X5R 0201-1 — BYPASS=UH700.B2::5MM
CH736 14UF 20% 4V X5R 0402-THICKSTNCL
CH736 14UF 20% 4V X5R 0402-D2X-1
PLACE_NEAR=UH735.1::5MM
PACK_IGNORE=TRUE
PACK_OPTION=HDMI14UF:NORM
PACK_OPTION=HDMI14UF:THICK
BYPASS=UH700.D2::5MM
FLH712 FERR-80-OHM-2.3A-0.038-MOHM 0402 — PP0V95_AWAKESW_DP2HDMI (92 94 135)
PLACE_NEAR=UH700.D2::5MM
CH742 0.1UF 10% 6.3V CERM-X5R 0201 — BYPASS=UH700.L9::5MM
CH743 1.0UF 20% 6.3V X5R 0201-1 — BYPASS=UH700.L9::5MM
CH744 14UF 20% 4V X5R 0402-THICKSTNCL
CH744 14UF 20% 4V X5R 0402-D2X-1
PLACE_NEAR=CH743.1::5MM
PACK_IGNORE=TRUE
PACK_OPTION=HDMI14UF:NORM
PACK_OPTION=HDMI14UF:THICK
PLACE_NEAR=UH700.L9::5MM

PP0V95_DP2HDMI_VDDTX VOLTAGE=0.95V
PP0V95_DP2HDMI_VDDRX VOLTAGE=0.95V
PP0V95_DP2HDMI_VDDA VOLTAGE=0.95V

UH700 PS190 BGA 338S00772

		DPRX_AUX_P	C3	DP_AUXP	1.2V
		DPRX_AUX_N	D3	DP_AUXN	
		DPRX_DATA_P<0> GND_VOID=TRUE	B1	DP_RX0P	0.9V
		DPRX_DATA_N<0> GND_VOID=TRUE	C1	DP_RX0N	
		DPRX_DATA_P<1> GND_VOID=TRUE	D1	DP_RX1P	0.9V
		DPRX_DATA_N<1> GND_VOID=TRUE	E1	DP_RX1N	
		DPRX_DATA_P<2> GND_VOID=TRUE	G1	DP_RX2P	0.9V
		DPRX_DATA_N<2> GND_VOID=TRUE	H1	DP_RX2N	
		DPRX_DATA_P<3> GND_VOID=TRUE	J1	DP_RX3P	0.9V
		DPRX_DATA_N<3> GND_VOID=TRUE	K1	DP_RX3N	
		DPRX_INT_HPD	L2	DP_HPD	1.2V
		UART_DP2HDMI_RXD_R	J7	UART_RX	1.2V
		UART_DP2HDMI_TXD_R	J8	UART_TX	
		I2C_HDMI_DEBUG_SCL	L8	I2C_CSCL	1.2V
		I2C_HDMI_DEBUG_SDA	M8	I2C_CSDA	
		NC_COBRA_TEST_OP	M1	TEST_OP	0.9V
		NC_COBRA_TEST_ON	M2	TEST_ON	
		NC_COBRA_TEST33	D4	TEST33	3.3V
		COBRA_TEST_MODE_L	H8	TEST_MODE	1.2V
		DP2HDMI_RESET_R_L	K8	RESET*	1.2V
		NC_HDMI_CEC_IRQ CKPLUS_WAIVE=SINGLE_NODENET	M9	CEC_IRQ	1.2V
		COBRA_XIN	A7	XIN	
		COBRA_XOUT	A8	XOUT	3.3V
		DP2HDMI_REXT	A3	REXT	3.3V
		DP2HDMI_CEXT	A4	CEXT	
		NC_COBRA_I2S_BCLK	F3	I2S_BCLK	
		NC_COBRA_I2S_FSYNC	E5	I2S_FSYNC	
		NC_COBRA_I2S_DOUT	E3	I2S_DOUT	
		NC_COBRA_I2S_MUTE	F2	I2S_MUTE	
		NC_COBRA_I2S_IRQ	E4	I2S_IRQ	
		TP_COBRA_VDD09_ON	M7	VDD09_ON	
3.3V		HDMI_DDC_SCL	D5	HDMI_DDC_5V_SCL	
3.3V		HDMI_DDC_SDA	D6	HDMI_DDC_5V_SDA	
		HDMI_HEACP	C8	NC_COBRA_HDMI_HEACP	
		HDMI_HEACN	D8	NC_COBRA_HDMI_HEACN	
0.9V		HDMI_TX0P	G10	HDMI_DATA_P<0> NO_TEST=1	
		HDMI_TX0N	H10	HDMI_DATA_N<0> NO_TEST=1	
0.9V		HDMI_TX1P	D10	HDMI_DATA_P<1> NO_TEST=1	
		HDMI_TX1N	E10	HDMI_DATA_N<1> NO_TEST=1	
0.9V		HDMI_TX2P	B10	HDMI_DATA_P<2> NO_TEST=1	
		HDMI_TX2N	C10	HDMI_DATA_N<2> NO_TEST=1	
0.9V		HDMI_TXCP	J10	HDMI_CLK_P NO_TEST=1	
		HDMI_TXCN	K10	HDMI_CLK_N NO_TEST=1	
3.3V		HDMI_HPD	B8	HDMI_HPD_IN_R	
3.3V		HDMI_CEC	D7	HDMI_CEC_R	
3.3V		HDMI_ISNK	C7	COBRA_HDMI_ISNK	
		GPIO0	J3	TP_COBRA_GPIO0	
		GPIO1	J4	DP2HDMI_1.5G_FILT_EN	
		GPIO2	J5	TP_COBRA_GPIO2	
		GPIO3	J6	TP_COBRA_GPIO3	
		GPIO4	K3	NC_COBRA_GPIO4	
		GPIO5	K4	COBRA_GPIO5	
		GPIO6	K5	TP_COBRA_GPIO6	
1.2V		GPIO7	K7	NC_COBRA_GPIO7	
		GPIO8	L3	COBRA_GPIO8	
		GPIO9	L4	COBRA_GPIO9	
		GPIO10	L5	COBRA_GPIO10	
		GPIO11	M3	COBRA_GPIO11	
		GPIO12	M4	NC_COBRA_GPIO12	
		GPIO13	M5	NC_COBRA_GPIO13	
		GPIO14	M6	NC_COBRA_GPIO14	
3.3V		SPI_SCLK	A5	SPI_DP2HDMI_CLK	
3.3V		SPI_MOSI	B5	SPI_DP2HDMI_DI	
		SPI_MISO	B4	SPI_DP2HDMI_DO	
3.3V		SPI_CS*	C5		
		SPI_BUS_GNT*	C6	COBRA_SPI_GNT	
		SPI_WR_PROT*	C4	COBRA_SPI_WR_PROT	
		GND	A1 A2 A9 A10 B7 C2 C9 E2 E7 E9 F1 F5 F7 F10 G2 G5 G7 G9 H5 H7 J2 J9 K6 L1 L10 M10		

SW GPIO TPS PER <RDAR://74536924>,<RDAR://79172907>,<RDAR://77622534>

SPI ROM APN: 335S0915 - WINBOND W25X40CL 512KB USON PACKAGE

RH715 0 0% 1/20W — HDMI_HPD_IN (90 93 147)
RH762 0 0% 1/20W — HDMI_CEC (90)
RH708 20K 5% 1/20W TK 0201
CH706 0.1UF 10% 16V X5R-CERM 0201
RH711 100K 5% 1/20W TK 0201
RH712 100K 5% 1/20W TK 0201
RH714 100K 5% 1/20W TK 0201
RH704 4.7K 5% 1/20W TK 0201
PP3V3_AWAKESW_DP2HDMI (90 92 93 94 136)
UH701 4MBIT W25X40CLXIG USON OMIT_TABLE
CH705 0.1UF 10% 16V X5R-CERM 0201 — BYPASS=UH701.8::5MM
RH713 100K 5% 1/20W TK 0201
SPI_DP2HDMI_CS_L (136)
SPI_DP2HDMI_HOLD_L_3V3 (93)
RH705 100K 5% 1/20W TK 0201

PP1V2_DP2HDMI (92) → RH726 4.7K 5% 1/10W TK 0201 → COBRA_TEST_MODE_L (92)
PP1V2_DP2HDMI (92) → RH701 47K 5% 1/20W TK 0201
TPH701 A TP-P4 — UART_DP2HDMI_R2D (6) NET/TP NOT USED ON POR PROGRAMS
RH730 0 0% 1/20W NOSTUFF 0201 TK
RH731 0 0% 1/20W NOSTUFF 0201 TK
UART_DP2HDMI_D2R (82 6 OUT)
TPH702 A TP-P4
CH702 1UF 20% 16V CER-X5R 0201 NOSTUFF
DP2HDMI_RESET_R_L (147 93 92 IN)
HOOKUP TO I2C8
RH737 10K 5% 1/20W TK 0201
RH734 10K 5% 1/20W TK 0201
RH735 10K 5% 1/20W TK 0201
TP_COBRA_GPIO2 (92)
COBRA_GPIO8 (92)
COBRA_GPIO5 (92)

COBRA_XIN
COBRA_XOUT
RH702 0 0% 1/20W TK 0201
RH703 0 0% 1/20W TK 0201
197S00036 CRITICAL YH700 2.00X1.60-SM 25MHZ-25PPM-20PF-50OHM
COBRA_XIN_R_R
COBRA_XOUT_R_L
GND_VOID=TRUE
GND_VOID=TRUE
CRITICAL CH700 33PF 5% 25V C0G 0201
CRITICAL CH701 33PF 5% 25V C0G 0201
RH770 1K 0.5% 1/20W TK 0201
CH775 1.0UF 10% 6.3V X5R-CERM 0201-1
RH771 47K 5% 1/20W TK 0201 — PP1V2_DP2HDMI (92)

PP1V2_DP2HDMI (92) → COBRAPART:1 RH727 10K 5% 1/20W TK 0201
COBRA_GPIO9 (92)
COBRA_GPIO10 (92)
COBRA_GPIO11 (92)
COBRAPART:0
RH723 10K 5% 1/20W TK 0201
RH724 10K 5% 1/20W TK 0201
RH725 10K 5% 1/20W TK 0201
PP3V3_DP2HDMI (92) → RH706 4.7K 5% 1/20W TK 0201
COBRA_SPI_GNT (92)

BOM_COST_GROUP=HDMI

PAGE TITLE	HDMI: COBRA
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*** IN PROGRESS ***

LPDP AC Caps

From SOC

To HDMI

LPDP_INT_DATA_C_N<0>	PACK_OPTION=HDMI2SOC:LPDP	CH820	0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_N<0>
DP_DP2HDMI_DATA_N<0>					
LPDP_INT_DATA_C_P<0>	PACK_OPTION=HDMI2SOC:LPDP	CH821	0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_P<0>
DP_DP2HDMI_DATA_P<0>					
LPDP_INT_DATA_C_N<1>	PACK_OPTION=HDMI2SOC:LPDP	CH822	0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_N<1>
DP_DP2HDMI_DATA_N<1>					
LPDP_INT_DATA_C_P<1>	PACK_OPTION=HDMI2SOC:LPDP	CH823	0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_P<1>
DP_DP2HDMI_DATA_P<1>					
LPDP_INT_DATA_C_N<2>	PACK_OPTION=HDMI2SOC:LPDP	CH824	0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_N<2>
DP_DP2HDMI_DATA_N<2>					
LPDP_INT_DATA_C_P<2>	PACK_OPTION=HDMI2SOC:LPDP	CH825	0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_P<2>
DP_DP2HDMI_DATA_P<2>					
LPDP_INT_DATA_C_N<3>	PACK_OPTION=HDMI2SOC:LPDP	CH826	0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_N<3>
DP_DP2HDMI_DATA_N<3>					
LPDP_INT_DATA_C_P<3>	PACK_OPTION=HDMI2SOC:LPDP	CH827	0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_P<3>
DP_DP2HDMI_DATA_P<3>					
LPDP_INT_AUX_C_N	PACK_OPTION=HDMI2SOC:LPDP	CH828	0.1UF	10% 6.3V CERM-X5R 0201	DPRX_AUX_N
DP_DP2HDMI_AUX_N					
LPDP_INT_AUX_C_P	PACK_OPTION=HDMI2SOC:LPDP	CH829	0.1UF	10% 6.3V CERM-X5R 0201	DPRX_AUX_P
DP_DP2HDMI_AUX_P					

DP2HDMI_RESET_L → RH801 0 (0% 1/20W TK 0201) → DP2HDMI_RESET_R_L

HDMI ROM BOM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0915	1	IC,SRL SPI FLASH ROM,4MBIT,50MHZ,USON8	UH701	HDMI_ROM:512
335S00133	1	IC,SPI SERIAL FLASH,4MBITS,3.0V,USON8	UH701	HDMI_ROM:1M
341S02145	1	ROM,HDMI,CBR (V02.55.00) P1-A/B,X2293	UH701	HDMI_ROM:PREP

LEVEL SHIFTERS

PP1V2_S2 → CH842 0.1UF (10% 6.3V CERM-X5R 0201) → GND

PP1V2_S2 — NO_XNET_CONNECTION=1 — RH822 47K (1% 1/20W TK 0201) → SPI_DP2HDMI_HOLD_L

PP3V3_AWAKESW_DP2HDMI → CH841 0.1UF (10% 6.3V CERM-X5R 0201) → GND

UH840 SN74AXC1T45-S SOT-5X3: VCCA, VCCB, DIR, A, B, GND

SPI_DP2HDMI_HOLD_L → A; B → SPI_DP2HDMI_HOLD_L_3V3

PP3V3_S2 → CH802 0.1UF (10% 16V X5R-CERM 0201) → GND

UH802 74LVC1G07 SOT886: VCC, A, Y, NC, NC, NC, GND

HDMI_HPD_IN → A; Y → HDMI_AOP_HPD_R → RH804 100 (1% 1/20W TK 0201-1) → HDMI_HPD_AOP

PP1V2_S2 — NOSTUFF → RH803 47K (1% 1/20W TK 0201)

PP1V2_S2 — NO_XNET_CONNECTION=1 → RH815 47K (1% 1/20W TK 0201)

CH801 0.1UF (10% 16V X5R-CERM 0201) → GND

NO_XNET_CONNECTION=1 → RH816 27K (5% 1/20W TK 0201)

HDMI_CEC_AOP_TX → RH806 0 (0% 1/20W TK 0201) → AOP_HDMI_CEC_R

UH801 74AUP2G07GM SOT886: VCC, 1A, 1Y, 2A, 2Y, GND

CEC_FLT_R → RH810 187 (1% 1/20W TK 0201) → CEC_FLT

HDMI_AOP_CEC_R → RH805 100 (1% 1/20W TK 0201-1) → HDMI_CEC_AOP_RX

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0536	311S0341		UH802	RDAR://64195790

CONNECT THIS NET TO 5V_S2_MAIN

PLACE THIS NEAR 5V_S2_MAIN_VR_OUTPUT
PLACE_NEAR=CH917:10mm

XWH801 SM: PP5V_S2_MAIN → PP5V_S2_HDMI_LDO (VOLTAGE=5)

PP5V_S2_HDMI (MAKE_BASE=TRUE) → PP5V_S2_HDMI (VOLTAGE=5)

THIS IS USED FOR CONTROLLING HDMI PORT POWER VIA THE PMU SYS ALIVE NET

USE THE BYPASS BOMOPTION TO NOT STUFF THESE
OR NO STUFF ALL OF THESE FOR DESKTOPS

HDMI_SPF_AND:STUFF

PP1V8_S2 → CH805 0.1UF (10% 6.3V CERM-X5R 0201) → GND

UH805 SN74AUP1G08 USON (HDMI_SPF_AND:STUFF): A, B, Y, NC

PMU_SYS_ALIVE → A

DP2HDMI_PWR_EN_PMU → B

Y → DP2HDMI_PWR_EN_R → RH807 0 (0% 1/20W TK 0201) → DP2HDMI_PWR_EN

RH808 0 (0% 1/20W TK 0201) NOSTUFF

RH809 0 (0% 1/20W TK 0201)

INTEGRATORS NEED TO UPDATE UPSTREAM
PMU GPIO NETNAMES TO ACCOMODATE THIS ENABLE NET

HDMI_SPF_AND:BYPASS

RH908/RH909 intended for potential
resistor divider need after AND gate

SAK BYPASS OPTIONS (INCLUDING RESET ABOVE)

THESE REQUIRE UH805 OR RH809 TO BE STUFFED

DP2HDMI_PWR_EN → RH811 0 (HDMI_SAK:BYPASS) → P0V95_HDMI_EN

CH807 0.1UF (HDMI_SAK:BYPASS)

RH812 0 (HDMI_SAK:BYPASS) → P1V2_HDMI_PWR_EN

CH808 0.1UF (HDMI_SAK:BYPASS)

RH813 0 (HDMI_SAK:BYPASS) → P3V3_HDMI_PWR_EN

CH809 0.1UF (HDMI_SAK:BYPASS)

THIS SAK IS USED FOR COBRA POWER SEQUENCING

PP1V8_S2 → CH806 0.1UF (10% 6.3V CERM-X5R 0201) → GND

UH806 SLG4AP45256 STQFN 343S00528: VDD, GND

PMU_SYS_ALIVE	SYS_ACTIVE	DISCHARGE_EN	P0V95_DSCHG_EN_RC
DP2HDMI_PWR_EN_PMU	HDMI_ENABLE	PP0V95V_EN	P0V95_HDMI_EN
NC_UH805_5	NC	PP1V2_EN	P1V2_HDMI_PWR_EN
NC_UH805_11	NC	PP3V3_EN	P3V3_HDMI_PWR_EN
		RESETB	DP2HDMI_RESET_R_L
		RESETB_2	TP_UH805_6

BOM_COST_GROUP=HDMI

PAGE TITLE: HDMI: Project Support 1

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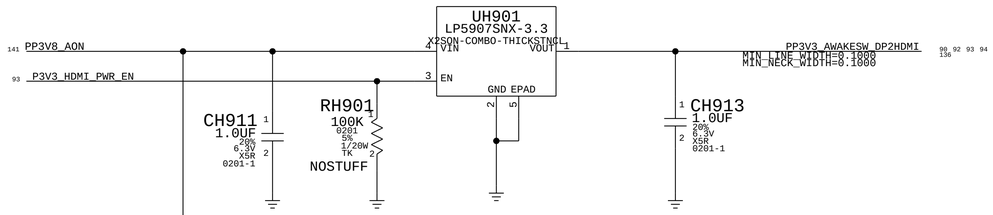
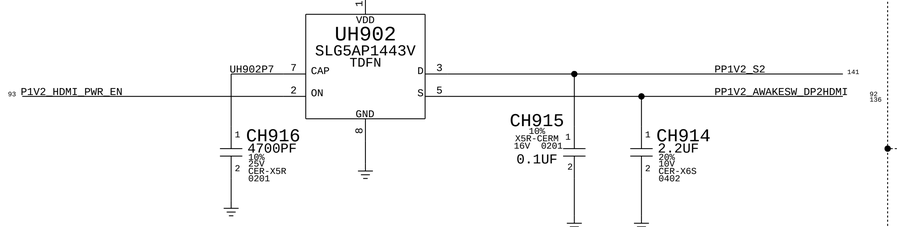
3.3V LDO



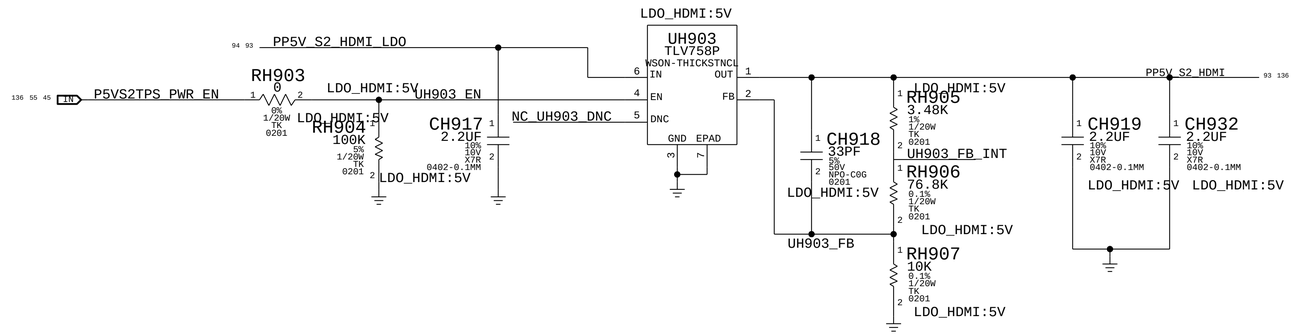
1.2V LOAD SW



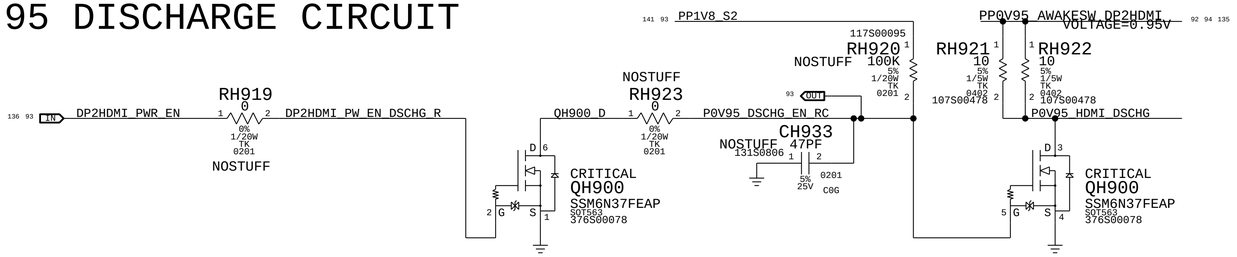
THIS IS USED FOR LONGER 5V POWER PATHS TO ENSURE GOOD 5V REGULATION

Enable BOMOPTION LDO_HDMI:NONE to disable the LDO use

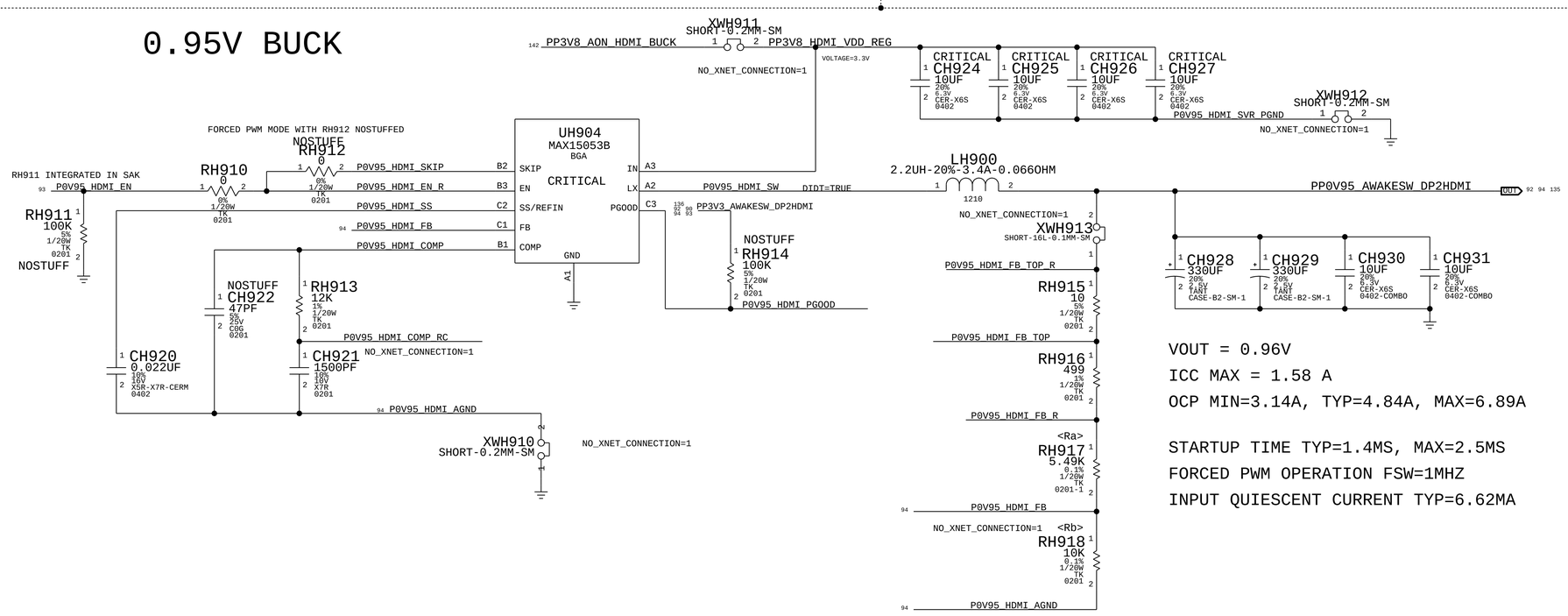
Enable BOMOPTION LDO_HDMI:5V to test HDMI 5V limit to 5.3V



0.95 DISCHARGE CIRCUIT



0.95V BUCK



VOUT = 0.96V

ICC MAX = 1.58 A

OCP MIN=3.14A, TYP=4.84A, MAX=6.89A

STARTUP TIME TYP=1.4MS, MAX=2.5MS

FORCED PWM OPERATION FSW=1MHZ

INPUT QUIESCENT CURRENT TYP=6.62MA

PAGE TITLE

HDMI: Project Support 2

Apple Inc.

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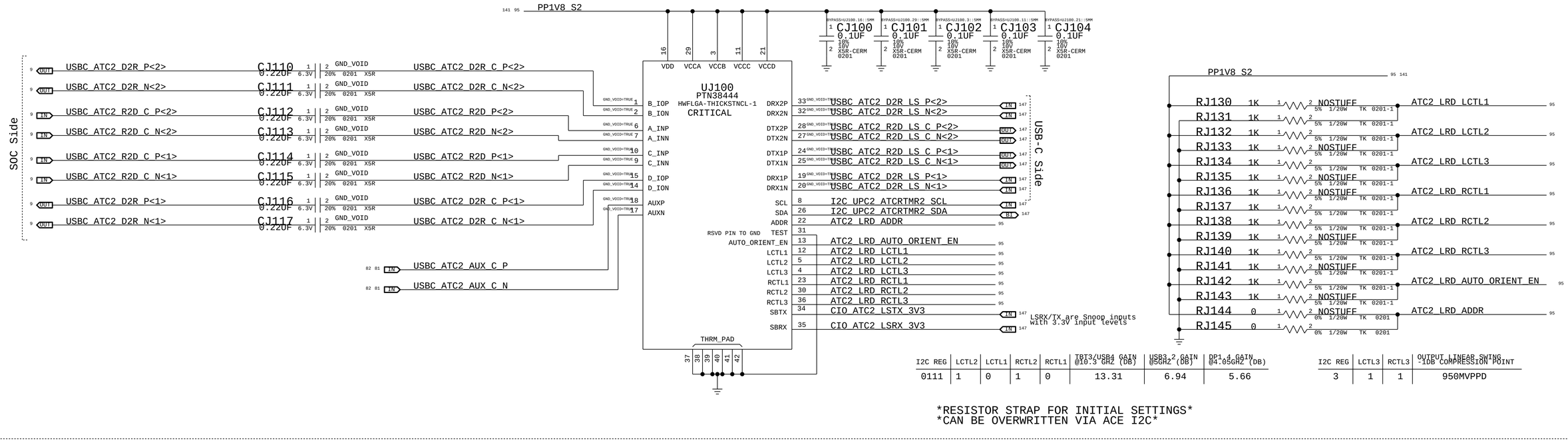
*** In Progress ***



I2C REG	LCTL2	LCTL1	RCTL2	RCTL1	TBT3/USB4 GAIN @10.3 GHZ (DB)	USB3.2 GAIN @5GHZ (DB)	DP1.4 GAIN @4.05GHZ (DB)
0111	1	0	1	0	13.31	6.94	5.66

I2C REG	LCTL3	RCTL3	OUTPUT LINEAR SWING -1DB COMPRESSION POINT
3	1	1	950MVPPD

RESISTOR STRAP FOR INITIAL SETTINGS
CAN BE OVERWRITTEN VIA ACE I2C

ATC3 Redriver still in progress
Circuit will be identical to that of ATC2

BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: CIO Redrivers 2/3

Apple Inc.

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BOM_COST_GROUP=SECURE ELEMENT

PAGE TITLE
USB-C: CIO Redrivers 4/5

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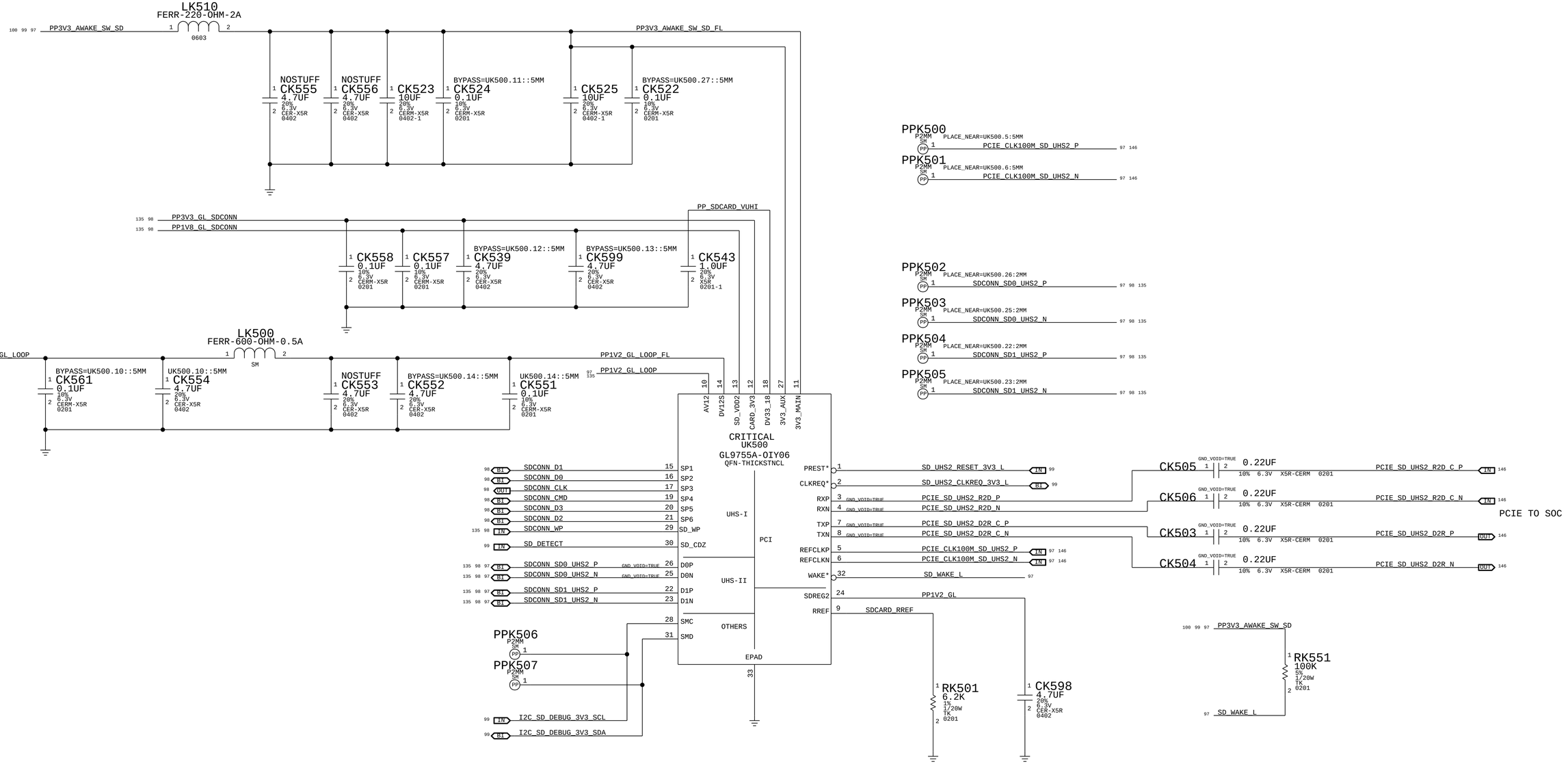

BOM_COST_GROUP=SDCARD

PAGE TITLE: SDCARD CONTROLLER

Apple Inc.

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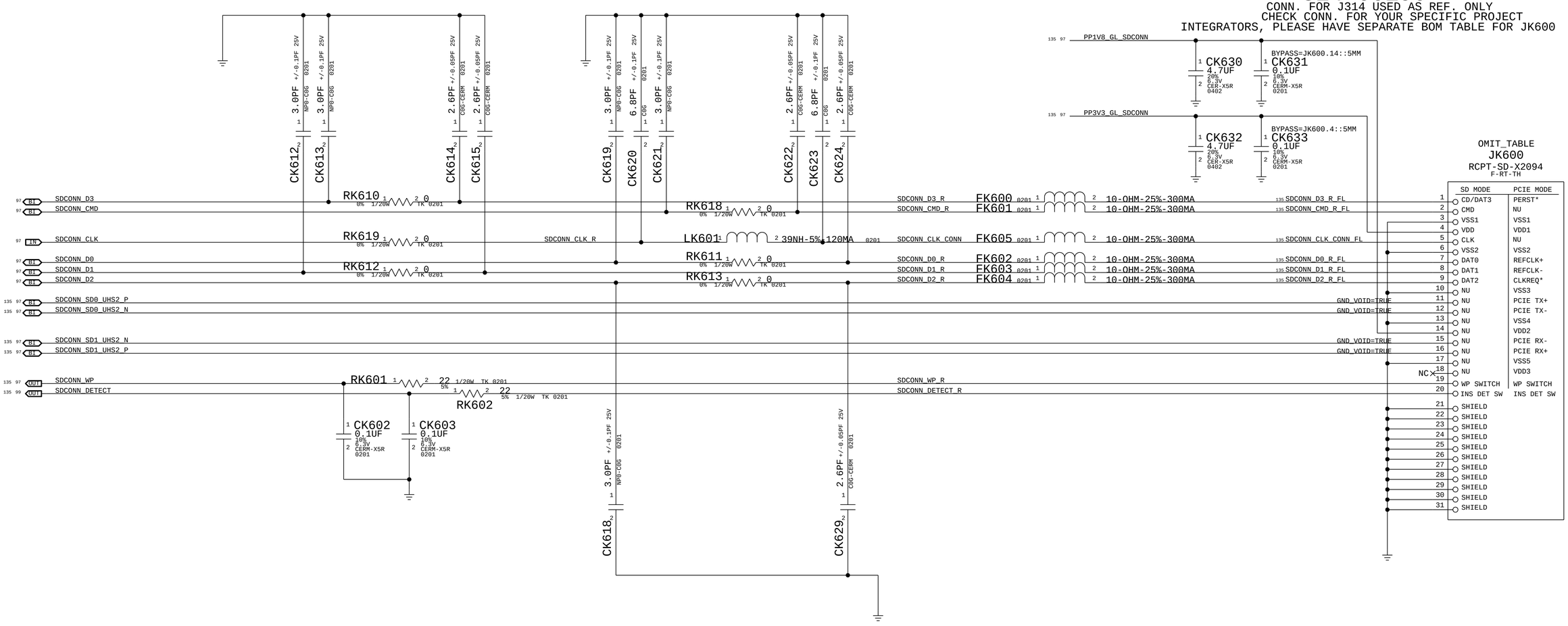
SD CARD CONNECTOR
514-00196

CONN. FOR J314 USED AS REF. ONLY
CHECK CONN. FOR YOUR SPECIFIC PROJECT
INTEGRATORS, PLEASE HAVE SEPARATE BOM TABLE FOR JK600



BOM_COST_GROUP=SDCARD

PAGE TITLE	SDCARD CONNECTOR
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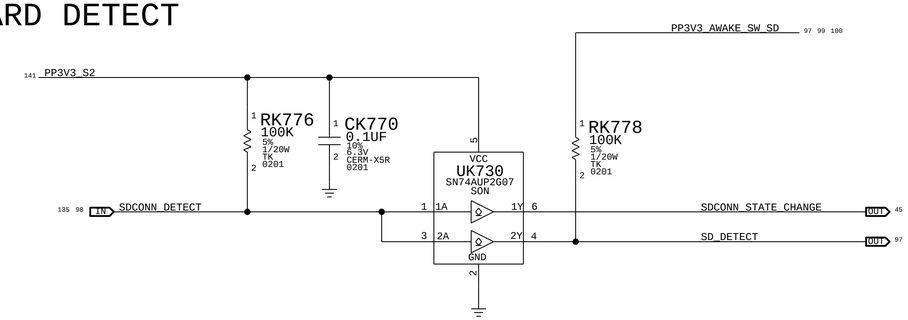
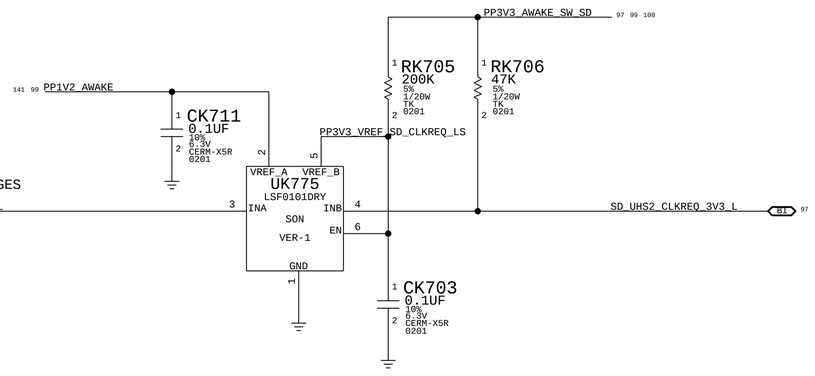
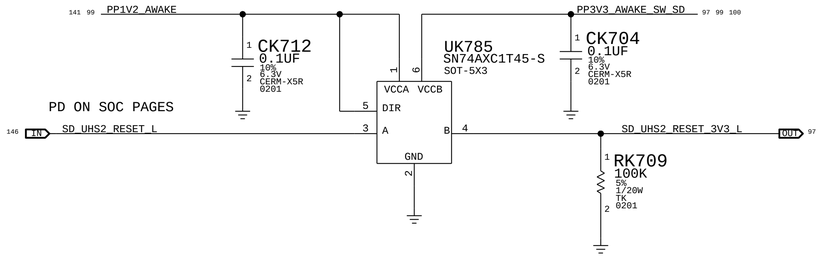
Apple Inc.

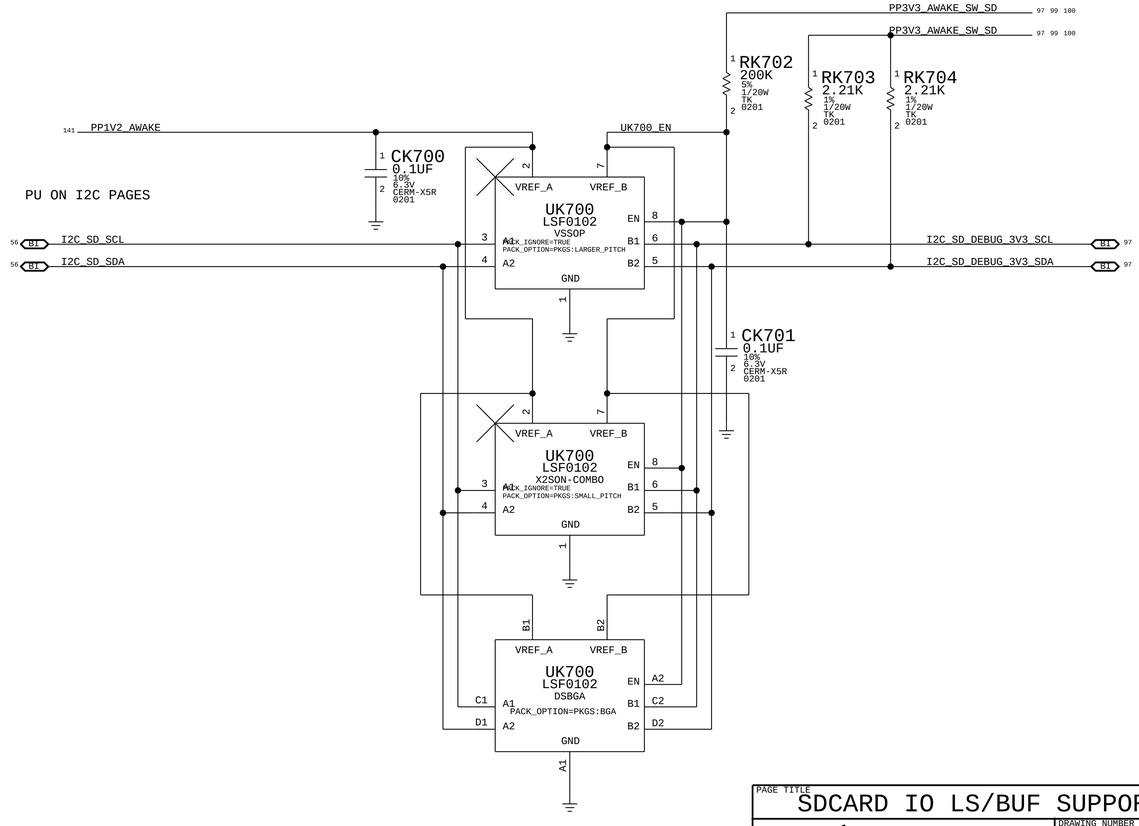
CARD DETECT



CONTROLLER IO







BOM_COST_GROUP=SDCARD

PAGE TITLE
SDCARD IO LS/BUF SUPPORT

Apple Inc.

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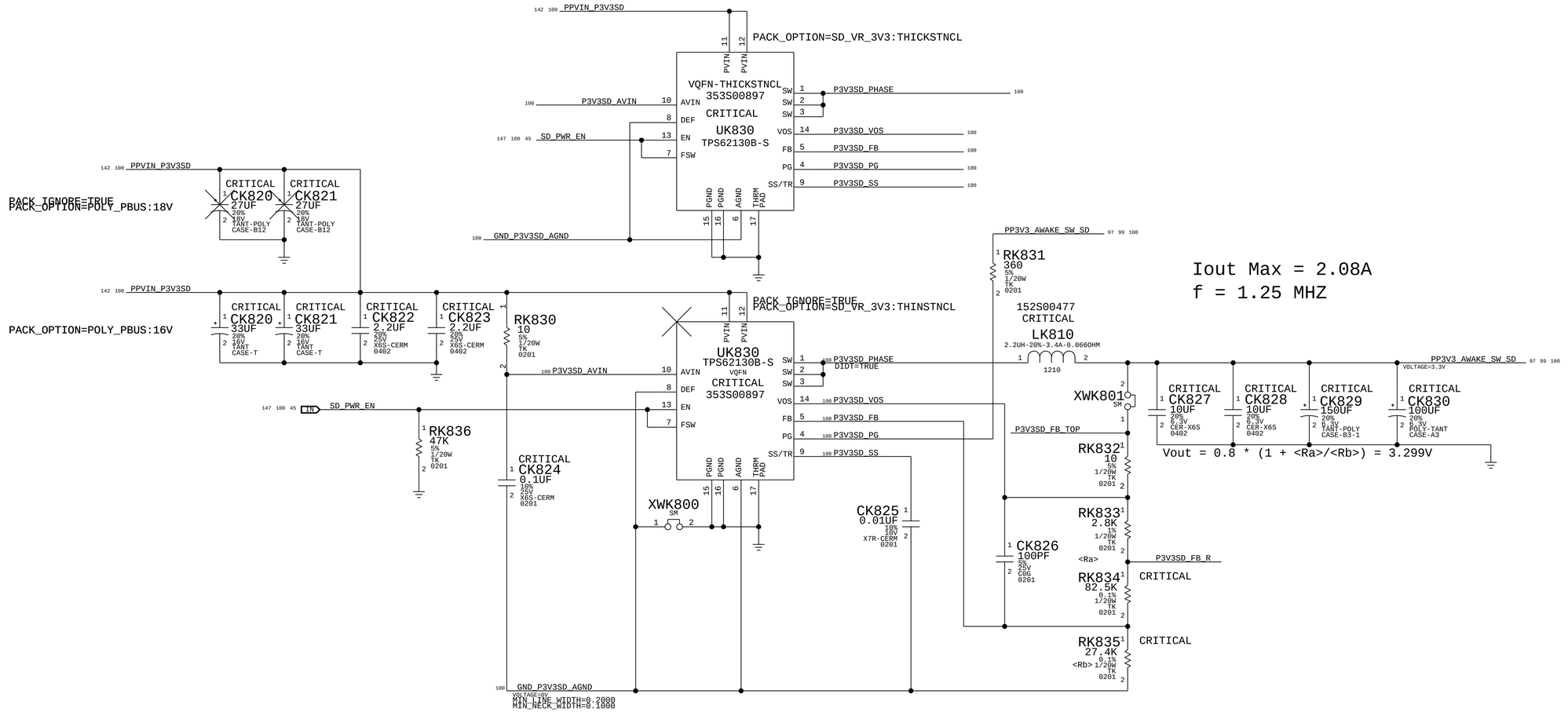

PAGE TITLE: SDCARD POWER SUPPORT

Apple Inc.

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*** OK2INTEGRATE ***

FOR SYSTEM INTEGRATION INFORMATION OF WILLAMETTE REFER TO
RDAR://PROBLEM/72432057

WILLAMETTE WIFI/BT MODULE

PLACE_NEAR=UL000.48:4MM
PLACE_NEAR=UL000.48:3MM
PLACE_NEAR=UL000.48:3MM
PP3V8_AON_WLBT 101 139 142
CL005 10UF 20% 10V X5R-CERM 0402-8
CL030 3PF +/-0.1PF 25V C0G 0201
CRITICAL
CL020 12PF 5% 25V NP0-C0G 0201
VBAT

PLACE_NEAR=UL000.37:4MM
PLACE_NEAR=UL000.37:3MM
PLACE_NEAR=UL000.37:3MM
PP3V8_AON_WLBT 101 139 142
CL006 10UF 20% 10V X5R-CERM 0402-8
CL031 3PF +/-0.1PF 25V C0G 0201
CRITICAL
CL021 12PF 5% 25V NP0-C0G 0201
2GFEM_C0

PLACE_NEAR=UL000.79:4MM
PLACE_NEAR=UL000.79:3MM
PLACE_NEAR=UL000.79:3MM
PP3V8_AON_WLBT 101 139 142
CL007 10UF 20% 10V X5R-CERM 0402-8
CL032 3PF +/-0.1PF 25V C0G 0201
CRITICAL
CL022 12PF 5% 25V NP0-C0G 0201
2GFEM_C1

PLACE_NEAR=UL000.12:4MM
PLACE_NEAR=UL000.12:3MM
PLACE_NEAR=UL000.12:3MM
PP3V8_AON_WLBT 101 139 142
CL008 10UF 20% 10V X5R-CERM 0402-8
CL033 3PF +/-0.1PF 25V C0G 0201
CRITICAL
CL023 12PF 5% 25V NP0-C0G 0201
5GFEM

PLACE_NEAR=UL000.31:4MM
PLACE_NEAR=UL000.31:3MM
PP1V8_S2 101 139 141
CL010 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL
CL024 12PF 5% 25V NP0-C0G 0201
2GFEM_C0

PLACE_NEAR=UL000.86:4MM
PLACE_NEAR=UL000.86:3MM
PP1V8_S2 101 139 141
CL011 10UF 20% 10V X5R-CERM 0402-8
CRITICAL
CL025 12PF 5% 25V NP0-C0G 0201
2GFEM_C1

PLACE_NEAR=UL000.22:3MM
PLACE_NEAR=UL000.22:4MM
PP1V8_S2 101 139 141
CL012 0.1UF 10% 6.3V CERM-X5R 0201
CL034 3PF +/-0.1PF 25V C0G 0201
5GFEM_C0

PLACE_NEAR=UL000.4:4MM
PLACE_NEAR=UL000.4:3MM
PP1V8_S2 101 139 141
CL013 0.1UF 10% 6.3V CERM-X5R 0201
CL035 3PF +/-0.1PF 25V C0G 0201
5GFEM_C1

PP1V8_S2 141 139 101
PP3V8_AON_WLBT 142 139 101
PP1V2_S2
PLACE_NEAR=UL000.51:4MM 142
CL014 0.1UF 10% 6.3V CERM-X5R 0201

VDD_5G_C0C1 11
VDD_5G_C0C1 12
VDD_5G_C0C1 13
VDD_5G_C0C1 14
VDD_2G_C0 37
VDD_2G_C0 38
VDD_2G_C1 79
VDD_2G_C1 80
VDD_BT 69
VBAT 48
VBAT 49
VBAT 50
VBAT 133
VBAT 134
VBAT 135
VDD1V8_2G_C0 31
VDD1V8_2G_C1 86
VDD1V8_5G_C0 22
VDD1V8_5G_C1 4
VDDIO_RF 66
VDDIO1P8 67
VDDIO1P2 52

UL000
2103-602102-10
LGA
SYM 1 OF 4

102 BT	RF_ANT_0	NO_TEST=1	28	ANT_0
102 BT	RF_ANT_1	NO_TEST=1	89	ANT_1
102 BT	RF_BT_DED	NO_TEST=1	73	BT_DEDICATED
	NC_BT_GPIO_2	NO_TEST=1	413	BT_GPIO_2
136 102 101 6 OUT	BT_TIME_SYNC		435	BT_GPIO_3
	NC_BT_GPIO_4	NO_TEST=1	129	BT_GPIO_4
	NC_BT_GPIO_5	NO_TEST=1	41	BT_GPIO_5
101 13 IN	SPMI_WLBT_CLK		126	SPMI_HEB_CLK
101 13 BT	SPMI_WLBT_DATA		391	SPMI_HEB_DAT
101 BT	BT_LHL_GPIO2		523	LHL_GPIO2
	NC_SPMI_IDC_CLK		40	SPMI_IDC_CLK
	NC_SPMI_IDC_DATA		127	SPMI_IDC_DAT
136 102 101 45 44 IN	WLBT_PWR_EN		130	WLBT_REG_ON
136 102 101 45 IN	PMU_CLK32K_WLBT		479	WLBT_CLK_32K
101	WLAN_JTAG_SEL		540	JTAG_SEL
			131	PACKAGEOPTION_2

RL002 10K 5% 1/20W TK 0201

WL_GPIO_0	542	WLBT_WAKE	OUT 44 101 102
WL_GPIO_1	528	WLAN_TIME_SYNC	OUT 6 101 102
WL_GPIO_2	526	TP_WLAN_JTAG_TCK	101 102
WL_GPIO_3	525	TP_WLAN_JTAG_TMS	101 102
WL_GPIO_4	75	TP_WLAN_JTAG_TDI	101
WL_GPIO_5	76	TP_WLAN_JTAG_TDO	101
WL_GPIO_6	158	TP_WLAN_JTAG_TRSTN	101
WL_GPIO_7	538	WL_GPIO_7	101
WL_GPIO_8	153	NC_WL_GPIO_8 NO_TEST=1	
WL_GPIO_9	527	NC_WL_GPIO_9 NO_TEST=1	
WL_GPIO_10	159	NC_WL_GPIO_10 NO_TEST=1	
WL_GPIO_11	140	NC_WL_GPIO_11 NO_TEST=1	
WL_GPIO_12	138	NC_WL_GPIO_12 NO_TEST=1	
WL_GPIO_13	42	NC_WL_GPIO_13 NO_TEST=1	
WL_GPIO_14	539	NC_WL_GPIO_14 NO_TEST=1	
WL_GPIO_15	139	NC_WL_GPIO_15 NO_TEST=1	
WL_GPIO_16	541	NC_WL_GPIO_16 NO_TEST=1	
WL_GPIO_18	44	NC_WL_GPIO_18 NO_TEST=1	
WL_GPIO_19	43	NC_WL_GPIO_19 NO_TEST=1	
WLBT_PCIE_PERST_L	534	WLBT_RESET_L	IN 8 101 102 136
WLBT_PCIE_CLKREQ_L	531	WLBT_CLKREQ_R_L	101
WLBT_PCIE_RXD_P	143	PCIE_WLBT_R2D_P	101
WLBT_PCIE_RXD_N	142	PCIE_WLBT_R2D_N	101
WLBT_PCIE_TXD_P	146	PCIE_WLBT_D2R_C_P	101
WLBT_PCIE_TXD_N	145	PCIE_WLBT_D2R_C_N	101
WLBT_PCIE_REFCLK_P	148	PCIE_CLK100M_WLBT_P	IN 8 101
WLBT_PCIE_REFCLK_N	149	PCIE_CLK100M_WLBT_N	IN 8 101

OMIT_TABLE

GND_VOID=TRUE
PLACE_NEAR=UL000.143:4MM
8 IN PCIE_WLBT_R2D_C_P — CL001 0.1UF 6.3V 10% 0201 CERM-X5R — PCIE_WLBT_R2D_P 101
8 IN PCIE_WLBT_R2D_C_N — CL002 0.1UF 6.3V 10% 0201 CERM-X5R — PCIE_WLBT_R2D_N 101
PLACE_NEAR=UL000.142:4MM
GND_VOID=TRUE

GND_VOID=TRUE
PLACE_NEAR=UL000.146:4MM
101 PCIE_WLBT_D2R_C_P — CL003 0.1UF 6.3V 10% 0201 CERM-X5R — PCIE_WLBT_D2R_P OUT 8 101
101 PCIE_WLBT_D2R_C_N — CL004 0.1UF 6.3V 10% 0201 CERM-X5R — PCIE_WLBT_D2R_N OUT 8 101
PLACE_NEAR=UL000.145:4MM
GND_VOID=TRUE

101 13 SPMI_WLBT_CLK — RL003 200K 1/20W 5% 0201 TK
101 13 SPMI_WLBT_DATA — RL004 200K 1/20W 5% 0201 TK

101 WLBT_CLKREQ_R_L — RL001 1K 1/20W 5% 0201-1 TK — WLBT_CLKREQ_L BI 8 101 102

BOM_COST_GROUP=WIRELESS

TPL001 A TP-P4 PMU_CLK32K_WLBT 45 101 102 136
TPL002 A TP-P4 WLBT_PWR_EN 44 45 101 102 136
TPL003 A TP-P4 WLBT_WAKE 44 101 102
TPL004 A TP-P4 TP_WLAN_JTAG_TCK 101 102
TPL005 A TP-P4 TP_WLAN_JTAG_TMS 101 102
TPL006 A TP-P4 TP_WLAN_JTAG_TDI 101
TPL007 A TP-P4 TP_WLAN_JTAG_TDO 101
TPL008 A TP-P4 TP_WLAN_JTAG_TRSTN 101
TPL009 A TP-P4 WLAN_JTAG_SEL 101
TPL010 A TP-P4 BT_TIME_SYNC 6 101 102 136
TPL011 A TP-P4 WLAN_TIME_SYNC 6 101 102
TPL018 A TP-P4 SPMI_WLBT_CLK 13 101
TPL019 A TP-P4 SPMI_WLBT_DATA 13 101
TPL020 A TP-P4 BT_LHL_GPIO2 101
PPL021 P2MM 3M PP 1 PCIE_CLK100M_WLBT_P 8 101
PPL022 P2MM 3M PP 1 PCIE_CLK100M_WLBT_N 8 101
TPL023 A TP-P4 WLBT_RESET_L 8 101 102 136
TPL024 A TP-P4 WLBT_CLKREQ_L 8 101 102
TPL025 A TP-P4 WL_GPIO_7 101
PPL026 P2MM 3M PACK_IGNORE=TRUE PACK_OPTION=WLBT_PP_D2R PCIE_WLBT_D2R_P 8 101
PPL027 P2MM 3M PACK_IGNORE=TRUE PACK_OPTION=WLBT_PP_D2R PCIE_WLBT_D2R_N 8 101

WILLAMETTE BOM TABLE:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S01093	1	MODULE,WLAN/BT,WILLAMETTE, ES4.7	UL000	CRITICAL	

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WILLAMETTE WIFI/BT MODULE GND

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1	GND	GND	110
2	GND	GND	111
3	GND	GND	112
5	GND	GND	113
6	GND	GND	114
7	GND	GND	115
8	GND	GND	116
9	GND	GND	117
10	GND	GND	118
15	GND	GND	119
16	GND	GND	120
17	GND	GND	121
18	GND	GND	122
19	GND	GND	123
20	GND	GND	124
21	GND	GND	125
23	GND	GND	128
24	GND	GND	132
25	GND	GND	136
26	GND	GND	137
27	GND	GND	141
29	GND	GND	144
30	GND	GND	147
32	GND	GND	150
33	GND	GND	151
34	GND	GND	152
35	GND	GND	154
36	GND	GND	155
39	GND	GND	156
45	GND	GND	157
46	GND	GND	160
47	GND	GND	161
51	GND	GND	162
53	GND	GND	163
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100	GND	GND	200
101	GND	GND	201
102	GND	GND	202
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104	GND	GND	204
105	GND	GND	205
106	GND	GND	206
107	GND	GND	207
108	GND	GND	208
109	GND	GND	209

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LGA
SYM 3 OF 4

210	GND	GND	290
211	GND	GND	291
212	GND	GND	292
213	GND	GND	293
214	GND	GND	294
215	GND	GND	295
216	GND	GND	296
217	GND	GND	297
218	GND	GND	298
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223	GND	GND	303
224	GND	GND	304
225	GND	GND	305
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227	GND	GND	307
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284	GND	GND	364
285	GND	GND	365
286	GND	GND	366
287	GND	GND	367
288	GND	GND	368
289	GND	GND	369

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LGA
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370	GND	GND	453
371	GND	GND	454
372	GND	GND	455
373	GND	GND	456
374	GND	GND	457
375	GND	GND	458
376	GND	GND	459
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380	GND	GND	463
381	GND	GND	464
382	GND	GND	465
383	GND	GND	466
384	GND	GND	467
385	GND	GND	468
386	GND	GND	469
387	GND	GND	470
388	GND	GND	471
389	GND	GND	472
390	GND	GND	473
392	GND	GND	474
393	GND	GND	475
394	GND	GND	476
395	GND	GND	477
396	GND	GND	478
397	GND	GND	480
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402	GND	GND	485
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412	GND	GND	495
414	GND	GND	496
415	GND	GND	497
416	GND	GND	498
417	GND	GND	499
418	GND	GND	500
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421	GND	GND	503
422	GND	GND	504
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441	GND	GND	522
442	GND	GND	524
443	GND	GND	529
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445	GND	GND	532
446	GND	GND	533
447	GND	GND	535
448	GND	GND	536
449	GND	GND	537
450	GND	GND	543
451	GND	GND	544
452	GND	GND	545

ANTENNA CONNECTORS

2G_C0
5G_C0
BT_C0

JL120
IR050D15010C
F-ST-SM
1 RF_ANT_0 NO_TEST=1 BI 101 102
SUNWAY_1P5MM
PACK_OPTION=SUNWAY
BOMOPTION=RF_CONN

JL130
20431-001E-01
F-ST-SM
SIGNAL 1 RF_ANT_0 101 102
GND
IPEX 2MM
PACK_OPTION=3X_ANTENNA_IPEX PACK_IGNORE=TRUE
BOMOPTION=RF_CONN

2G_C1
5G_C1
BT_C1

JL121
IR050D15010C
F-ST-SM
1 RF_ANT_1 NO_TEST=1 BI 101 102
SUNWAY_1P5MM
PACK_OPTION=SUNWAY
BOMOPTION=RF_CONN

JL131
20431-001E-01
F-ST-SM
SIGNAL 1 RF_ANT_1 101 102
GND
IPEX 2MM
PACK_OPTION=3X_ANTENNA_IPEX PACK_IGNORE=TRUE
BOMOPTION=RF_CONN

BT_C1_DED

JL122
IR050D15010C
F-ST-SM
1 102 RF_BT_DED_ANT NO_TEST=1
SUNWAY_1P5MM
PACK_OPTION=3X_ANTENNA
BOMOPTION=RF_CONN

UL101
2GHZ
LFL182G44UA1F627
IN 1
OUT 3 RF_BT_DED NO_TEST=1 BI 101 102
GND 2
PACK_OPTION=3X_ANTENNA
BOMOPTION=RF_CONN
ALLOW_APPLE_PREFIX=U

JL132
20431-001E-01
F-ST-SM
SIGNAL 1 102 RF_BT_DED_ANT
GND
IPEX 2MM
PACK_OPTION=3X_ANTENNA_IPEX
BOMOPTION=RF_CONN

UL111
2GHZ
LFL182G44UA1F627
IN 1
OUT 3 RF_BT_DED 101 102
GND 2
PACK_IGNORE=TRUE
PACK_OPTION=3X_ANTENNA_IPEX
BOMOPTION=RF_CONN
ALLOW_APPLE_PREFIX=U

RF CONNECTOR ALTERNATE BOM:

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
518S0867	518S00033	RFCONN_ALT	ALL	IPEX

WLBT DEBUG CONNECTOR

JL103
505070-1222
M-ST-SM

101 6	WLAN_TIME_SYNC	TP_WLAN_JTAG_TCK	4388 SWD:
NC		TP_WLAN_JTAG_TMS	SWD_CLK 101
NC		NC	SWD_DIO 101
101 44	WLBT_WAKE	WLBT_CLKREQ_L	8 101
136 101 45 44	WLBT_PWR_EN	BT_TIME_SYNC	6 101 136
136 101 8	WLBT_RESET_L	PMU_CLK32K_WLBT	45 101 136

BOMOPTION=WLBT_DBG
PACK_IGNORE=TRUE
PACK_OPTION=WLBT_DBG_CONN

BOM_COST_GROUP=WIRELESS

PAGE TITLE
WIFI/BT: ANTENNA and GND

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NAND0 S5E0

PCIE AC caps - place as close as possible to NAND

PCB designers should add stiching vias for RFU/RFU_2 NC pins

Spec recommends to tie BCM, WP directly to 1.2V rail

Spec recommends to tie Boot2 directly to Gnd

The inductance from CN047, CN046, CN045, CN044 to their S5E pins shall be less than 1100pH

UN000 MK2-H1.3MM BGA SYM 2 OF 4 OMIT_TABLE

UN000 MK2-H1.3MM BGA SYM 1 OF 4 OMIT_TABLE

UN000 MK2-H1.3MM BGA SYM 4 OF 4 OMIT_TABLE

UN000 MK2-H1.3MM BGA SYM 3 OF 4 OMIT_TABLE

BOM_COST_GROUP=SSD

PAGE TITLE	STORAGE: SSD0 S5E MK2 <0>
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*** OK2INTEGRATE ***

NAND0 S5E1

PCIE AC caps - place as close as possible to NAND

PCB designers should add stiching vias for RFU/RFU_2 NC pins

The inductance from CN147, CN146, CN145, CN144 to their S5E pins shall be less than 1100pH

BOM_COST_GROUP=SSD

UN100 MK2-H1.3MM BGA SYM 2 OF 4 OMIT_TABLE

UN100 MK2-H1.3MM BGA SYM 1 OF 4 OMIT_TABLE

UN100 MK2-H1.3MM BGA SYM 3 OF 4 OMIT_TABLE

UN100 MK2-H1.3MM BGA SYM 4 OF 4 OMIT_TABLE

PAGE TITLE	STORAGE: SSD0 S5E MK2 <1>
DRAWING NUMBER	051-08156
SIZE	D
REVISION	3.0.0
BRANCH	evt-1
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Apple Inc.

*** OK2INTEGRTE ***

NAND0 S5E2

PCIE AC caps - place as close as possible to NAND

PCB designers should add stiching vias for RFU/RFU_2 NC pins

The inductance from CN247, CN246, CN245, CN244 to their S5E pins shall be less than 1100pH

BOM_COST_GROUP=SSD

UN200 MK2-H1.3MM BGA SYM 2 OF 4 OMIT_TABLE

13	NAND0_CLK24M_23	N11	CLK_IN
148	NAND0_RESET_L	J6	RESET*
134 106 104 103	NAND0_JTAG_TRST_L	F7	TRST* (INT PD)
113 11	PCIE_CLK100M_NAND0_2_3_P	T6	PCIE_REFCLK_P
113 11	PCIE_CLK100M_NAND0_2_3_N	U6	PCIE_REFCLK_N
13	NAND0_CLKREQ2_R_L	P6	PCIE_CLKREQ*
8	PCIE_NAND0_R2D_C_P<2>	U8	PCIE_RX0_P
8	PCIE_NAND0_R2D_C_N<2>	T8	PCIE_RX0_N
8	PCIE_NAND0_D2R_P<2>	U10	PCIE_TX0_P
8	PCIE_NAND0_D2R_N<2>	T10	PCIE_TX0_N
134 106 104 103 8	NAND0_PCIE_RESET_L	F10	EXT_NCE/PERST*
134	NAND0_S5E2_PCIE_RESREF	N10	PCIE_RESREF
134	NAND0_S5E2_ZQ_1	K5	ZQ_1
134	NAND0_S5E2_ZQ_0	M11	ZQ_0

(INT PU)	EXT_D0/BOOT0	G8	NAND0_LPB_L
(INT PD)	EXT_D1/BOOT1	H9	NAND_BFH
	EXT_D2/BOOT2/SPINAND_SCLK	F8	NAND0_BOOT2
	EXT_D3/SPINAND_MISO/SWD_UID0	E8	NAND0_S5E2_SWD_UID0
	EXT_D4/SPI_CS	G9	
	EXT_D5/SPINAND_MOSI/SWD_UID1	E9	NAND0_S5E2_SWD_UID1
	EXT_D6/BOOT3	F9	
	EXT_D7/SPF*	G10	NAND0_PFN_L
(INT PU)	EXT_DQS/BCM*	E10	NAND0_BCM_L
(INT PU)	EXT_NRE/JTAG_TMS	E6	SWD_NAND0_S5E2_S5E3_SWDIO
(INT PU)	EXT_NWE/JTAG_TCK	F6	SWD_NAND0_S5E2_S5E3_SWCLK
	EXT_RNB/JTAG_TDO	G6	NAND0_S5E2_JTAG_TDO
(INT PU)	EXT_CLE/JTAG_TDI	G7	NAND0_S5E1_JTAG_TDO
(INT PD)	EXT_ALE/JTAG_SEL	E7	NAND0_JTAG_SEL
	DROOP*	N4	TP_NAND0_S5E2_DROOP_L
	WP*	E5	NAND0_WP_L
	ANI0_VREF	K11	TP_NAND0_S5E2_ANI0_VREF
	ANI1_VREF	M5	TP_NAND0_S5E2_ANI1_VREF

UN200 MK2-H1.3MM BGA SYM 1 OF 4 OMIT_TABLE

E4 E12 F4 F12 T4 T12 U4 U12	VCC	(VCC)	
G5 G11 H5 H11 P5 P11 R5 R11	VDDIO_1	(VCCQ_IO)	
P9 P10	PCIE_AVDD_H		
N6	AVDD1X_PLL		
G12 G4 H4 H12 K4 M12 P4 P12 R4 R12	VDDIO_2_L_ANI	(VCCQ_ANI)	
K12 L4 L12 M4	VDDIO_2_DP		
J7 J9 K7 K9 M7 M9 N7 N9	VDD	(VDD)	
P7 R7 R9	PCIE_VDD		
M6	VDD_PLL		
E11	VPP		
H6	VQPS		
B5 B6 B7 B8 B9 B10 B11 C4 C12 D3 D13 E3 E13 F3 F5 F11 F13 G3 G13 H3 H7 H8 H13 J3 J4 J5 J8 J11 J12 J13 K3 K8 K13 L3 L7 L8 L9 L13 M3 M8 M13 N3 N5 N8 N12 N13 P3 P8 P13 R3 R6 R8 R10 R13 T3 T5 T7 T9 T11 T13 U3 U5 U7 U9 U11 U13 V4 V5 V6 V7 V8 V9 V10 V11 V12	VSS	(VSS)	

UN200 MK2-H1.3MM BGA SYM 4 OF 4 OMIT_TABLE

A1	VSS/DUMMY	N15	VSS/DUMMY
A2	VSS/DUMMY	P1	VSS/DUMMY
A3	VSS/DUMMY	P2	VSS/DUMMY
A4	VSS/DUMMY	P14	VSS/DUMMY
A5	VSS/DUMMY	P15	VSS/DUMMY
A6	VSS/DUMMY	R1	VSS/DUMMY
A7	VSS/DUMMY	R2	VSS/DUMMY
A8	VSS/DUMMY	R14	VSS/DUMMY
A9	VSS/DUMMY	R15	VSS/DUMMY
A10	VSS/DUMMY	T1	VSS/DUMMY
A11	VSS/DUMMY	T2	VSS/DUMMY
A12	VSS/DUMMY	T14	VSS/DUMMY
A13	VSS/DUMMY	T15	VSS/DUMMY
A14	VSS/DUMMY	U1	VSS/DUMMY
A15	VSS/DUMMY	U2	VSS/DUMMY
B1	VSS/DUMMY	U14	VSS/DUMMY
B2	VSS/DUMMY	U15	VSS/DUMMY
B3	VSS/DUMMY	V1	VSS/DUMMY
B4	VSS/DUMMY	V2	VSS/DUMMY
B12	VSS/DUMMY	V3	VSS/DUMMY
B13	VSS/DUMMY	V13	VSS/DUMMY
B14	VSS/DUMMY	V14	VSS/DUMMY
B15	VSS/DUMMY	V15	VSS/DUMMY
C1	VSS/DUMMY	W1	VSS/DUMMY
C2	VSS/DUMMY	W2	VSS/DUMMY
C3	VSS/DUMMY	W3	VSS/DUMMY
C13	VSS/DUMMY	W4	VSS/DUMMY
C14	VSS/DUMMY	W5	VSS/DUMMY
C15	VSS/DUMMY	W6	VSS/DUMMY
D1	VSS/DUMMY	W7	VSS/DUMMY
D2	VSS/DUMMY	W8	VSS/DUMMY
D14	VSS/DUMMY	W9	VSS/DUMMY
D15	VSS/DUMMY	W10	VSS/DUMMY
E1	VSS/DUMMY	W11	VSS/DUMMY
E2	VSS/DUMMY	W12	VSS/DUMMY
E14	VSS/DUMMY	W13	VSS/DUMMY
E15	VSS/DUMMY	W14	VSS/DUMMY
F1	VSS/DUMMY	W15	VSS/DUMMY
F2	VSS/DUMMY	Y1	VSS/DUMMY
F14	VSS/DUMMY	Y2	VSS/DUMMY
F15	VSS/DUMMY	Y3	VSS/DUMMY
G1	VSS/DUMMY	Y4	VSS/DUMMY
G2	VSS/DUMMY	Y5	VSS/DUMMY
G14	VSS/DUMMY	Y6	VSS/DUMMY
G15	VSS/DUMMY	Y7	VSS/DUMMY
H1	VSS/DUMMY	Y8	VSS/DUMMY
H2	VSS/DUMMY	Y9	VSS/DUMMY
H14	VSS/DUMMY	Y10	VSS/DUMMY
H15	VSS/DUMMY	Y12	VSS/DUMMY
J1	VSS/DUMMY	Y13	VSS/DUMMY
J2	VSS/DUMMY	Y14	VSS/DUMMY
J14	VSS/DUMMY	Y15	VSS/DUMMY
J15	VSS/DUMMY	AA1	VSS/DUMMY
K1	VSS/DUMMY	AA2	VSS/DUMMY
K2	VSS/DUMMY	AA3	VSS/DUMMY
K14	VSS/DUMMY	AA4	VSS/DUMMY
K15	VSS/DUMMY	AA5	VSS/DUMMY
L1	VSS/DUMMY	AA6	VSS/DUMMY
L2	VSS/DUMMY	AA7	VSS/DUMMY
L14	VSS/DUMMY	AA8	VSS/DUMMY
L15	VSS/DUMMY	AA9	VSS/DUMMY
M1	VSS/DUMMY	AA10	VSS/DUMMY
M2	VSS/DUMMY	AA11	VSS/DUMMY
M14	VSS/DUMMY	AA12	VSS/DUMMY
M15	VSS/DUMMY	AA13	VSS/DUMMY
N1	VSS/DUMMY	AA14	VSS/DUMMY
N2	VSS/DUMMY	AA15	VSS/DUMMY
N14	VSS/DUMMY		

UN200 MK2-H1.3MM BGA SYM 3 OF 4 OMIT_TABLE

NC_UN200_C5	C5	NC	Y11
NC_UN200_C6	C6	RFU_2	C10 NC_UN200_C10
NC_UN200_C7	C7	RFU_2	C11 NC_UN200_C11
NC_UN200_C8	C8	RFU	H10 NC_UN200_H10
NC_UN200_C9	C9	RFU	J10 NC_UN200_J10
NC_UN200_D4	D4	RFU	K6 NC_UN200_K6
NC_UN200_D5	D5	RFU	K10 NC_UN200_K10
NC_UN200_D6	D6	RFU	L5 NC_UN200_L5
NC_UN200_D7	D7	RFU	L6 NC_UN200_L6
NC_UN200_D8	D8	RFU	L10 NC_UN200_L10
NC_UN200_D9	D9	RFU	L11 NC_UN200_L11
NC_UN200_D10	D10	RFU	M10 NC_UN200_M10
NC_UN200_D11	D11		
NC_UN200_D12	D12		

PAGE TITLE	STORAGE: SSD0 S5E MK2 <2>		
Apple Inc.	DRAWING NUMBER	051-08156	SIZE D
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	BRANCH	evt-1	
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*** OK2INTEGRATE ***

NAND0 S5E3

UN300
MK2-H1.3MM
BGA
SYM 2 OF 4
OMIT_TABLE

13 IN NAND0_CLK24M_23 → N11 CLK_IN
148 IN NAND0_RESET_L → J6 RESET*
134 105 104 103 IN NAND0_JTAG_TRST_L → F7 TRST* (INT PD)
11 IN PCIE_CLK100M_NAND0_2_3_P → T6 PCIE_REFCLK_P
11 IN PCIE_CLK100M_NAND0_2_3_N → U6 PCIE_REFCLK_N
13 OUT NAND0_CLKREQ3_R_L ← P6 PCIE_CLKREQ*

PCIE AC caps - place as close as possible to NAND

8 IN PCIE_NAND0_R2D_C_P<3> — CN303 0.22UF 10% 6.3V X5R-CERM 0201 — PCIE_NAND0_R2D_P<3> (GND_VOID=TRUE) → U8 PCIE_RX0_P
8 IN PCIE_NAND0_R2D_C_N<3> — CN304 0.22UF 10% 6.3V X5R-CERM 0201 — PCIE_NAND0_R2D_N<3> (GND_VOID=TRUE) → T8 PCIE_RX0_N
8 OUT PCIE_NAND0_D2R_P<3> — CN301 0.22UF 10% 6.3V X5R-CERM 0201 — PCIE_NAND0_D2R_C_P<3> (GND_VOID=TRUE) → U10 PCIE_TX0_P
8 OUT PCIE_NAND0_D2R_N<3> — CN302 0.22UF 10% 6.3V X5R-CERM 0201 — PCIE_NAND0_D2R_C_N<3> (GND_VOID=TRUE) → T10 PCIE_TX0_N
134 105 104 103 8 IN NAND0_PCIE_RESET_L → F10 EXT_NCE/PERST*

134 NAND0_S5E3_PCIE_RESREF → N10 PCIE_RESREF

SSD_4L CN385 10PF 5% 25V C0G 0201
SSD_4L RN304 200 0.1% 1/20W TK 0201-2
134 NAND0_S5E3_ZQ_1 → K5 ZQ_1
134 NAND0_S5E3_ZQ_0 → M11 ZQ_0
PLACE_NEAR=UN300.K5:15MM — SSD_4L RN305 300 1% 1/20W TK 0201
PLACE_NEAR=UN300.M11:15MM — SSD_4L RN306 300 1% 1/20W TK 0201

(INT PU) EXT_D0/BOOT0 G8 NAND0_LPB_L → 103 104 105 107 134
(INT PD) EXT_D1/BOOT1 H9 NAND_BFH → 8 103 104 105 108 109 110 111 134
EXT_D2/BOOT2/SPINAND_SCLK F8 NAND0_BOOT2 → 103 104 105 134
EXT_D3/SPINAND_MISO/SWD_UID0 E8 NAND0_S5E3_SWD_UID0 → 106 134
EXT_D4/SPI_CS G9
EXT_D5/SPINAND_MOSI/SWD_UID1 E9 NAND0_S5E3_SWD_UID1 → 106 134
EXT_D6/BOOT3 F9
EXT_D7/SPF* G10 NAND0_PFN_L → 103 104 105 107 134
(INT PU) EXT_DQS/BCM* E10 NAND0_BCM_L → 103 104 105
(INT PU) EXT_NRE/JTAG_TMS E6 SWD_NAND0_S5E2_S5E3_SWDIO → 146
(INT PU) EXT_NWE/JTAG_TCK F6 SWD_NAND0_S5E2_S5E3_SWCLK → 146
EXT_RNB/JTAG_TDO G6 TP_NAND0_S5E3_JTAG_TDO → 134
(INT PU) EXT_CLE/JTAG_TDI G7 NAND0_S5E2_JTAG_TDO → 105 136
(INT PD) EXT_ALE/JTAG_SEL E7 NAND0_JTAG_SEL → 103 104 105 134
DROOP* N4 TP_NAND0_S5E3_DROOP_L → 135
WP* E5 NAND0_WP_L → 103 104 105 134
ANI0_VREF K11 TP_NAND0_S5E3_ANI0_VREF → 134 136
ANI1_VREF M5 TP_NAND0_S5E3_ANI1_VREF → 134 136

107 105 104 103 PP2V5_NAND0
SSD_4L CN320 20UF 20% 10V X5R 0402
SSD_4L CN322 2.2UF 20% 10V X5R 0201
SSD_4L CN323 2.2UF 20% 10V X5R 0201
SSD_4L CN324 2.2UF 20% 10V X5R 0201
SSD_4L CN325 2.2UF 20% 10V X5R 0201

SSD_4L FLN300 10OHM-50%-1A-0.05OHM 0201 PLACE_NEAR=UN300.P9:11.5MM
107 106 105 104 103 PP1V2_NAND0
SSD_4L CN345 4.7UF 20% 4V CER-X5R 0201
SSD_4L CN344 0.1UF 10% 6.3V CERM-X5R 0201
PP1V2_NAND0_S5E3_PCI_AVDD_H (MIN_LINE_WIDTH=0.1000 MIN_NECK_WIDTH=0.1000 VOLTAGE=1.2V)
SSD_4L RN310 2 1% 1/20W TK 0201 PLACE_NEAR=UN300.N6:11.5MM
SSD_4L CN347 2.2UF 20% 10V X5R 0201
SSD_4L CN346 0.1UF 10% 6.3V CERM-X5R 0201
PP1V2_NAND0_S5E3_AVDD1X_PLL (MIN_LINE_WIDTH=0.1000 MIN_NECK_WIDTH=0.1000 VOLTAGE=1.2V)

The inductance from CN347, CN346, CN345, CN344 to their S5E pins shall be less than 1100pH

PCB designers should add stiching vias for RFU/RFU_2 NC pins

UN300
MK2-H1.3MM
BGA
SYM 3 OF 4
OMIT_TABLE

NC_UN300_C5 C5 RFU_2
NC_UN300_C6 C6 RFU_2
NC_UN300_C7 C7 RFU_2
NC_UN300_C8 C8 RFU_2
NC_UN300_C9 C9 RFU_2
NC_UN300_D4 D4 RFU_2
NC_UN300_D5 D5 RFU_2
NC_UN300_D6 D6 RFU_2
NC_UN300_D7 D7 RFU_2
NC_UN300_D8 D8 RFU_2
NC_UN300_D9 D9 RFU_2
NC_UN300_D10 D10 RFU_2
NC_UN300_D11 D11 RFU_2
NC_UN300_D12 D12 RFU_2
NC Y11
RFU_2 C10 NC_UN300_C10
RFU_2 C11 NC_UN300_C11
RFU H10 NC_UN300_H10
RFU J10 NC_UN300_J10
RFU K6 NC_UN300_K6
RFU K10 NC_UN300_K10
RFU L5 NC_UN300_L5
RFU L6 NC_UN300_L6
RFU L10 NC_UN300_L10
RFU L11 NC_UN300_L11
RFU M10 NC_UN300_M10

PP1V2_NAND0 103 104 105 106 107
SSD_4L RN308 47K 1% 1/20W TK 0201
SSD_4L RN309 47K 1% 1/20W TK 0201
134 106 NAND0_S5E3_SWD_UID0
134 106 NAND0_S5E3_SWD_UID1

107 106 105 104 103 PP1V2_NAND0
SSD_4L CN330 4.3UF 20% 4V CERM 0402-THICKSTNCL
SSD_4L CN332 20UF 20% 10V X5R 0402
SSD_4L CN334 2.2UF 20% 10V X5R 0201
SSD_4L CN335 2.2UF 20% 10V X5R 0201
SSD_4L CN336 2.2UF 20% 10V X5R 0201
SSD_4L CN337 2.2UF 20% 10V X5R 0201
SSD_4L CN338 2.2UF 20% 10V X5R 0201
SSD_4L CN339 2.2UF 20% 10V X5R 0201
SSD_4L CN33A 2.2UF 20% 10V X5R 0201

107 106 PP0V9_NAND0
SSD_4L CN310 20UF 20% 10V X5R 0402
SSD_4L CN311 20UF 20% 10V X5R 0402
SSD_4L CN312 2.2UF 20% 10V X5R 0201
SSD_4L CN313 2.2UF 20% 10V X5R 0201
SSD_4L CN314 2.2UF 20% 10V X5R 0201
SSD_4L CN315 0.1UF 10% 6.3V CERM-X5R 0201
SSD_4L CN316 0.1UF 10% 6.3V CERM-X5R 0201
SSD_4L CN317 0.1UF 10% 6.3V CERM-X5R 0201

SSD_4L FLN301 10OHM-50%-1A-0.05OHM 0201 PLACE_NEAR=UN300.M6:11.5MM
107 106 PP0V9_NAND0 PLACE_NEAR=FLN301.2:5MM
SSD_4L CN383 4.7UF 20% 4V CER-X5R 0201
PP0V9_NAND0_S5E3_VDD_PLL (MIN_LINE_WIDTH=0.1000 MIN_NECK_WIDTH=0.1000 VOLTAGE=0.9V)

UN300
MK2-H1.3MM
BGA
SYM 1 OF 4
OMIT_TABLE

E4 VCC
E12 VCC
F4 VCC
F12 VCC
T4 VCC
T12 VCC
U4 VCC
U12 VCC
(VCC)

G5 VDDIO_1
G11 VDDIO_1
H5 VDDIO_1
H11 VDDIO_1
P5 VDDIO_1
P11 VDDIO_1
R5 VDDIO_1
R11 VDDIO_1
(VCCQ_IO)

P9 PCIE_AVDD_H
P10 PCIE_AVDD_H
N6 AVDD1X_PLL

G12 VDDIO_2_L_ANI
G4 VDDIO_2_L_ANI
H4 VDDIO_2_L_ANI
H12 VDDIO_2_L_ANI
K4 VDDIO_2_L_ANI
M12 VDDIO_2_L_ANI
P4 VDDIO_2_L_ANI
P12 VDDIO_2_L_ANI
R4 VDDIO_2_L_ANI
R12 VDDIO_2_L_ANI
(VCCQ_ANI)

K12 VDDIO_2_DP
L4 VDDIO_2_DP
L12 VDDIO_2_DP
M4 VDDIO_2_DP

J7 VDD
J9 VDD
K7 VDD
K9 VDD
M7 VDD
M9 VDD
N7 VDD
N9 VDD
(VDD)

P7 PCIE_VDD
R7 PCIE_VDD
R9 PCIE_VDD

M6 VDD_PLL
135 TP_NAND0_S5E3_VPP E11 VPP
H6 VQPS

VSS B5 B6 B7 B8 B9 B10 B11 C4 C12 D3 D13 E3 E13 F3 F5 F11 F13 G3 G13 H3 H7 H8 H13 J3 J4 J5 J8 J11 J12 J13 K3 K8 K13 L3 L7 L8 L9 L13 M3 M8 M13 N3 N5 N8 N12 N13 P3 P8 P13 R3 R6 R8 R10 R13 T3 T5 T7 T9 T11 T13 U3 U5 U7 U9 U11 U13 V4 V5 V6 V7 V8 V9 V10 V11 V12
(VSS)

UN300
MK2-H1.3MM
BGA
SYM 4 OF 4
OMIT_TABLE

A1 VSS/DUMMY — N15 VSS/DUMMY
A2 VSS/DUMMY — P1 VSS/DUMMY
A3 VSS/DUMMY — P2 VSS/DUMMY
A4 VSS/DUMMY — P14 VSS/DUMMY
A5 VSS/DUMMY — P15 VSS/DUMMY
A6 VSS/DUMMY — R1 VSS/DUMMY
A7 VSS/DUMMY — R2 VSS/DUMMY
A8 VSS/DUMMY — R14 VSS/DUMMY
A9 VSS/DUMMY — R15 VSS/DUMMY
A10 VSS/DUMMY — T1 VSS/DUMMY
A11 VSS/DUMMY — T2 VSS/DUMMY
A12 VSS/DUMMY — T14 VSS/DUMMY
A13 VSS/DUMMY — T15 VSS/DUMMY
A14 VSS/DUMMY — U1 VSS/DUMMY
A15 VSS/DUMMY — U2 VSS/DUMMY
B1 VSS/DUMMY — U14 VSS/DUMMY
B2 VSS/DUMMY — U15 VSS/DUMMY
B3 VSS/DUMMY — V1 VSS/DUMMY
B4 VSS/DUMMY — V2 VSS/DUMMY
B12 VSS/DUMMY — V3 VSS/DUMMY
B13 VSS/DUMMY — V13 VSS/DUMMY
B14 VSS/DUMMY — V14 VSS/DUMMY
B15 VSS/DUMMY — V15 VSS/DUMMY
C1 VSS/DUMMY — W1 VSS/DUMMY
C2 VSS/DUMMY — W2 VSS/DUMMY
C3 VSS/DUMMY — W3 VSS/DUMMY
C13 VSS/DUMMY — W4 VSS/DUMMY
C14 VSS/DUMMY — W5 VSS/DUMMY
C15 VSS/DUMMY — W6 VSS/DUMMY
D1 VSS/DUMMY — W7 VSS/DUMMY
D2 VSS/DUMMY — W8 VSS/DUMMY
D14 VSS/DUMMY — W9 VSS/DUMMY
D15 VSS/DUMMY — W10 VSS/DUMMY
E1 VSS/DUMMY — W11 VSS/DUMMY
E2 VSS/DUMMY — W12 VSS/DUMMY
E14 VSS/DUMMY — W13 VSS/DUMMY
E15 VSS/DUMMY — W14 VSS/DUMMY
F1 VSS/DUMMY — W15 VSS/DUMMY
F2 VSS/DUMMY — Y1 VSS/DUMMY
F14 VSS/DUMMY — Y2 VSS/DUMMY
F15 VSS/DUMMY — Y3 VSS/DUMMY
G1 VSS/DUMMY — Y4 VSS/DUMMY
G2 VSS/DUMMY — Y5 VSS/DUMMY
G14 VSS/DUMMY — Y6 VSS/DUMMY
G15 VSS/DUMMY — Y7 VSS/DUMMY
H1 VSS/DUMMY — Y8 VSS/DUMMY
H2 VSS/DUMMY — Y9 VSS/DUMMY
H14 VSS/DUMMY — Y10 VSS/DUMMY
H15 VSS/DUMMY — Y12 VSS/DUMMY
J1 VSS/DUMMY — Y13 VSS/DUMMY
J2 VSS/DUMMY — Y14 VSS/DUMMY
J14 VSS/DUMMY — Y15 VSS/DUMMY
J15 VSS/DUMMY — AA1 VSS/DUMMY
K1 VSS/DUMMY — AA2 VSS/DUMMY
K2 VSS/DUMMY — AA3 VSS/DUMMY
K14 VSS/DUMMY — AA4 VSS/DUMMY
K15 VSS/DUMMY — AA5 VSS/DUMMY
L1 VSS/DUMMY — AA6 VSS/DUMMY
L2 VSS/DUMMY — AA7 VSS/DUMMY
L14 VSS/DUMMY — AA8 VSS/DUMMY
L15 VSS/DUMMY — AA9 VSS/DUMMY
M1 VSS/DUMMY — AA10 VSS/DUMMY
M2 VSS/DUMMY — AA11 VSS/DUMMY
M14 VSS/DUMMY — AA12 VSS/DUMMY
M15 VSS/DUMMY — AA13 VSS/DUMMY
N1 VSS/DUMMY — AA14 VSS/DUMMY
N2 VSS/DUMMY — AA15 VSS/DUMMY
N14 VSS/DUMMY

BOM_COST_GROUP=SSD

PAGE TITLE
STORAGE: SSD0 S5E MK2 <3>

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PAGE TITLE
STORAGE: SSD0 OCARINA & NAND VCC

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SHEET 107 OF 159

*** OK2INTEGRATE ***

NAND1 S5E0

PCIE AC caps - place as close as possible to NAND

PCB designers should add stiching vias for RFU/RFU_2 NC pins

Spec recommends to tie BCM, WP directly to 1.2V rail

Spec recommends to tie Boot2 directly to Gnd

The inductance from CN547, CN546, CN545, CN544 to their S5E pins shall be less than 1100pH

BOM_COST_GROUP=SSD

PAGE TITLE: STORAGE: SSD1 S5E MK2 <0>

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*** OK2INTEGRATE ***

NAND1 S5E1

PCIE AC caps - place as close as possible to NAND

PCB designers should add stiching vias for RFU/RFU_2 NC pins

The inductance from CN647, CN646, CN645, CN644 to their S5E pins shall be less than 1100pH

BOM_COST_GROUP=SSD

PAGE TITLE: STORAGE: SSD1 S5E MK2 <1>

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*** OK2INTEGRATE ***

NAND1 S5E2

PCIE AC caps - place as close as possible to NAND

PCB designers should add stiching vias for RFU/RFU_2 NC pins

The inductance from CN747, CN746, CN745, CN744 to their S5E pins shall be less than 1100pH

BOM_COST_GROUP=SSD

PAGE TITLE: STORAGE: SSD1 S5E MK2 <2>

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*** OK2INTEGRATE ***

NAND1 S5E3

PCIE AC caps - place as close as possible to NAND

PCB designers should add stiching vias for RFU/RFU_2 NC pins

BOM_COST_GROUP=SSD

PAGE TITLE: STORAGE: SSD1 S5E MK2 <3>

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BRANCH: evt-1

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*** OK2INTEGRATE***

PAGE TITLE
STORAGE: SSD1 OCARINA & NAND VCC

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NAND CLK TEST POINTS

PPP009
P4MM
SM
PP
103 11 PCIE_CLK100M_NAND0_0_1_N 1

PPP010
P4MM
SM
PP
103 11 PCIE_CLK100M_NAND0_0_1_P 1

PPP013
P4MM
SM
PP
105 11 PCIE_CLK100M_NAND0_2_3_N 1

PPP014
P4MM
SM
PP
105 11 PCIE_CLK100M_NAND0_2_3_P 1

PPP017
P4MM
SM
PP
108 11 PCIE_CLK100M_NAND1_0_1_N 1

PPP018
P4MM
SM
PP
108 11 PCIE_CLK100M_NAND1_0_1_P 1

PPP021
P4MM
SM
PP
110 11 PCIE_CLK100M_NAND1_2_3_N 1

PPP022
P4MM
SM
PP
110 11 PCIE_CLK100M_NAND1_2_3_P 1

BOM_COST_GROUP=SSD

PAGE TITLE
STORAGE: SSD SUPPORT

Apple Inc.

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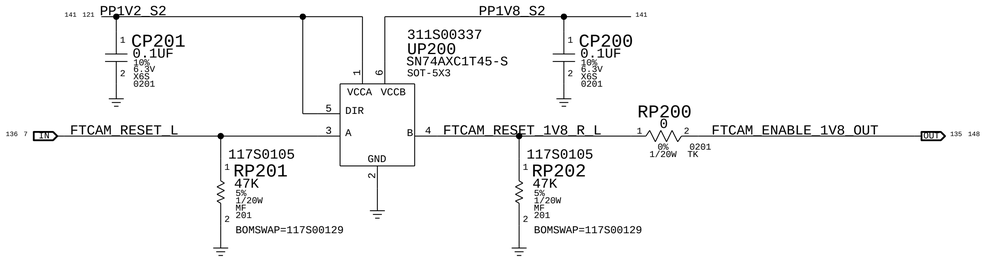
Level Shifter - FTCAM



PP CLOSE TO SOC FOR PROBING

PLACE_NEAR=U0600.B62:15MM
PPP200
P2MM
SM
135 115 7 LPDP_FTCAM_DATA_P<0>
PLACE_NEAR=U0600.C62:15MM
PPP201
P2MM
SM
135 115 7 LPDP_FTCAM_DATA_N<0>

BOM_COST_GROUP=CAMERA

SYNC_MASTER=J414_TKIM3_MLB_C_0.98.1 SYNC_DATE=09/20/2021

PAGE TITLE
CAMERA-SUPPORT

Apple Inc.

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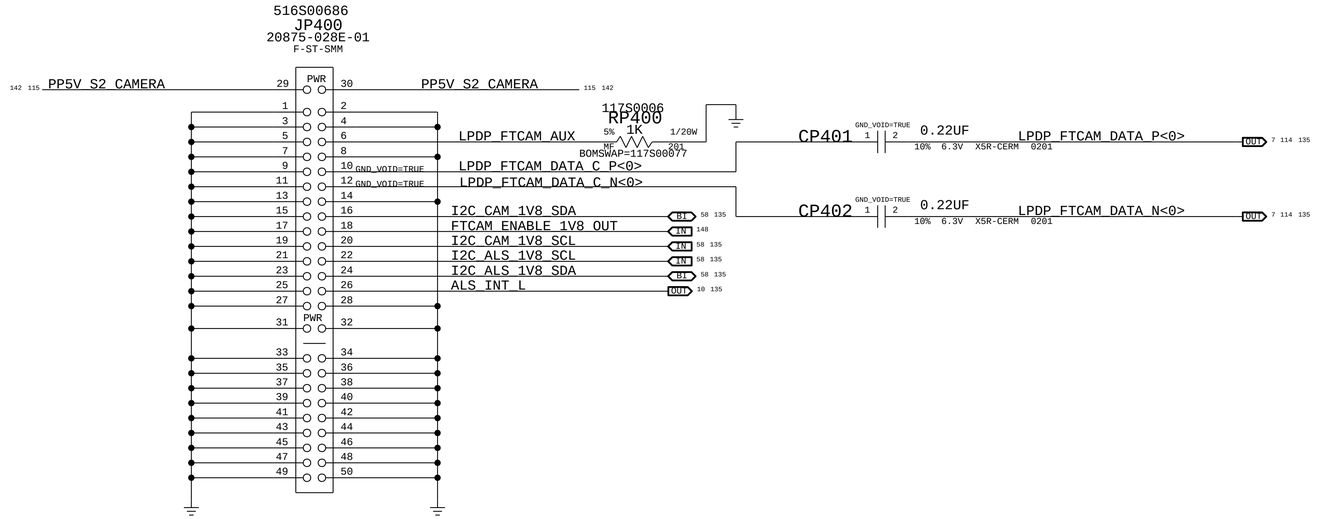

BOM_COST_GROUP=CAMERA

SYNC_MASTER= SYNC_DATE=

PAGE TITLE

CAMERA: FLEX CONNECTOR

Apple Inc.

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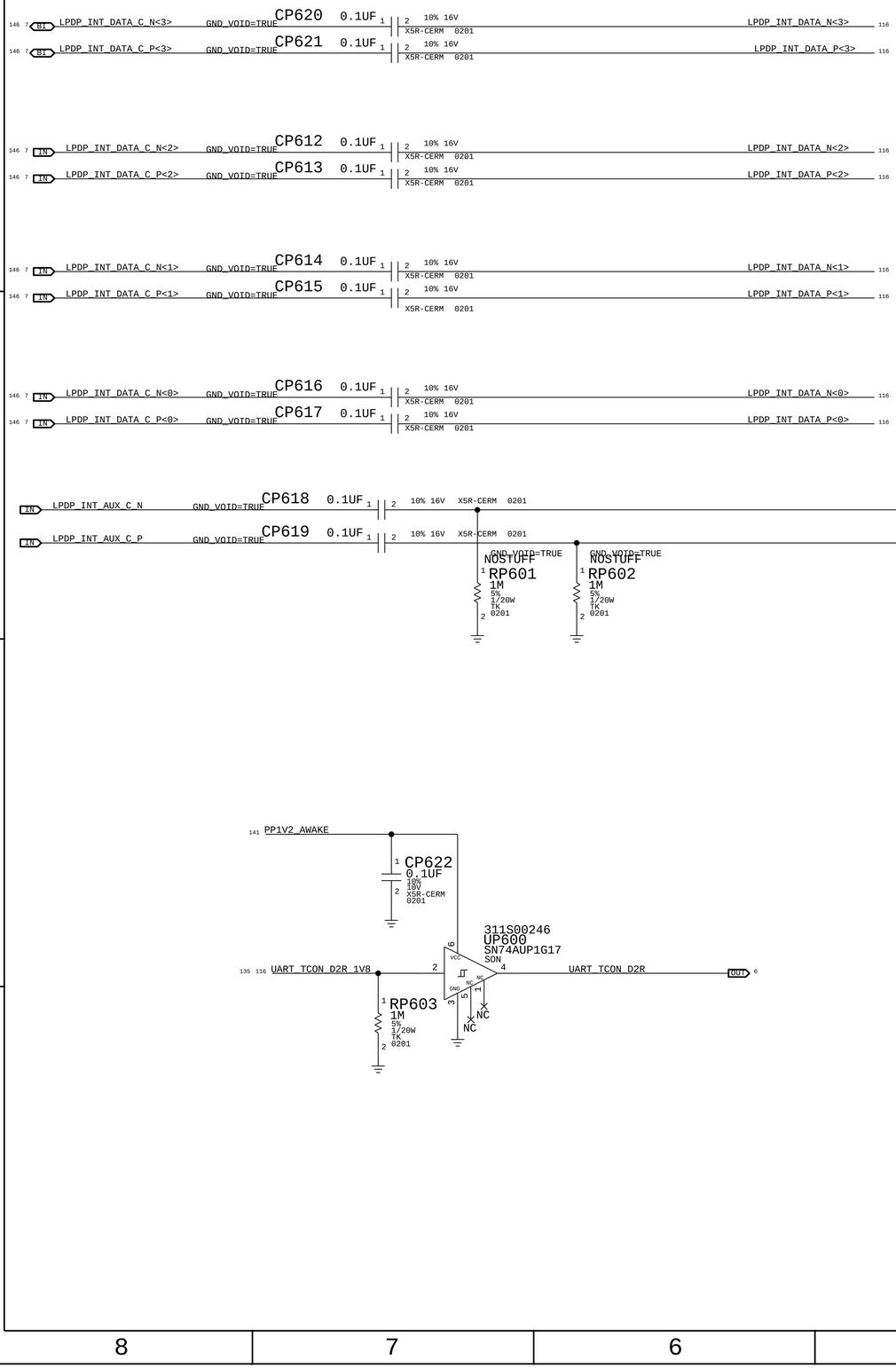

BOM_COST_GROUP=DISPLAY

PAGE TITLE: DISPLAY CONNECTOR

Apple Inc.

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*** OK2INTEGRATE ***

BOM_COST_GROUP=DISPLAY

PAGE TITLE
DISPLAY POWER SEQUENCER

Apple Inc.

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*** OK2INTEGRATE***

CP800 AND CP801 MUST BE MIRRORED

CP834 AND CP835 MUST BE MIRRORED

OD SIGNAL.
47K PU IS ON THE BCON CONNECTOR PAGE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S02811	1	IC,RAA209100,A1,BUCK-BOOST CTRLR,WLCSP36	UP800	

BOM_COST_GROUP=DISPLAY

PAGE TITLE: LUXE LCD Backlight Driver

Apple Inc.

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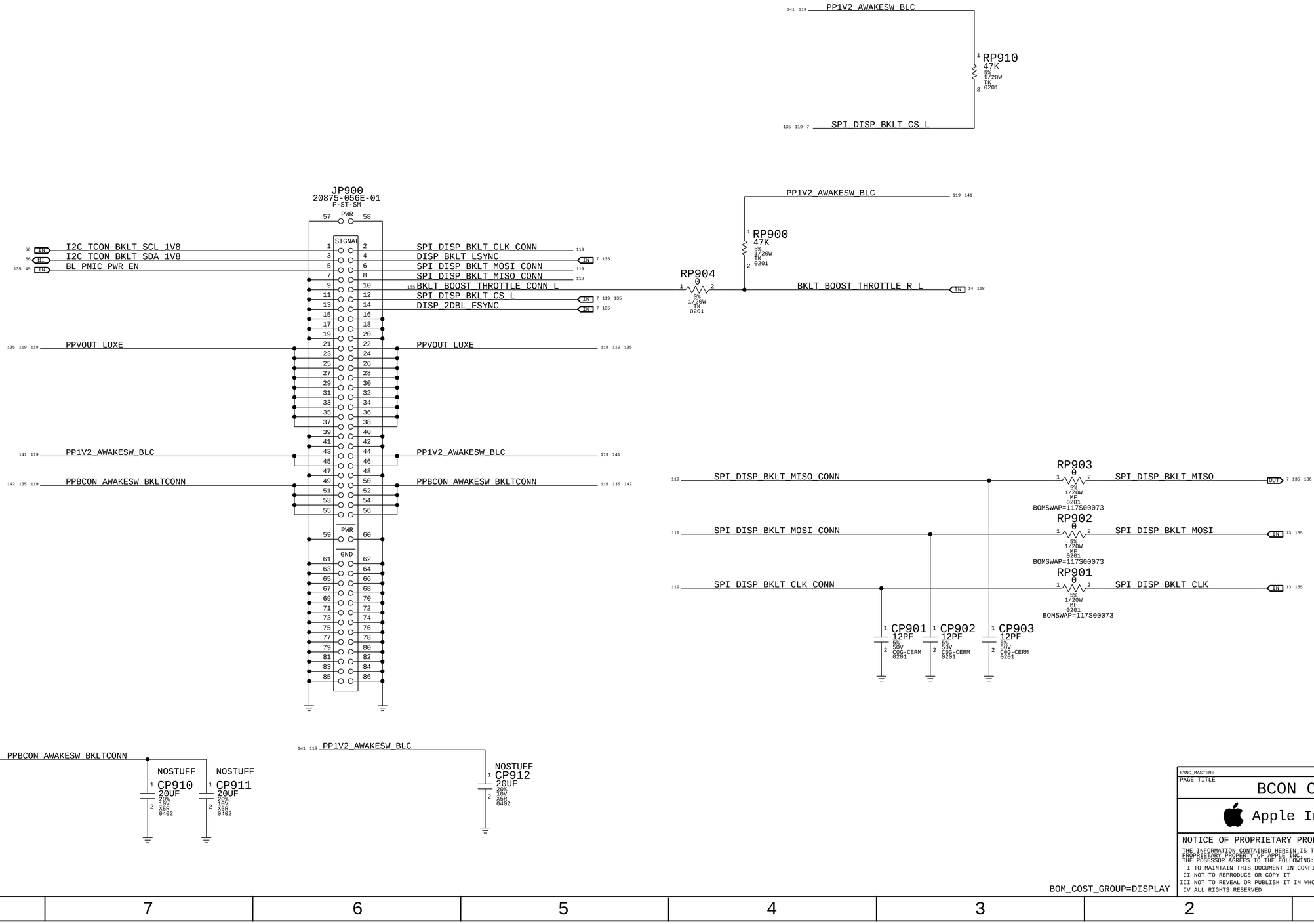

SYNC_MASTER=
SYNC_DATE=

PAGE TITLE

BCON CONNECTOR

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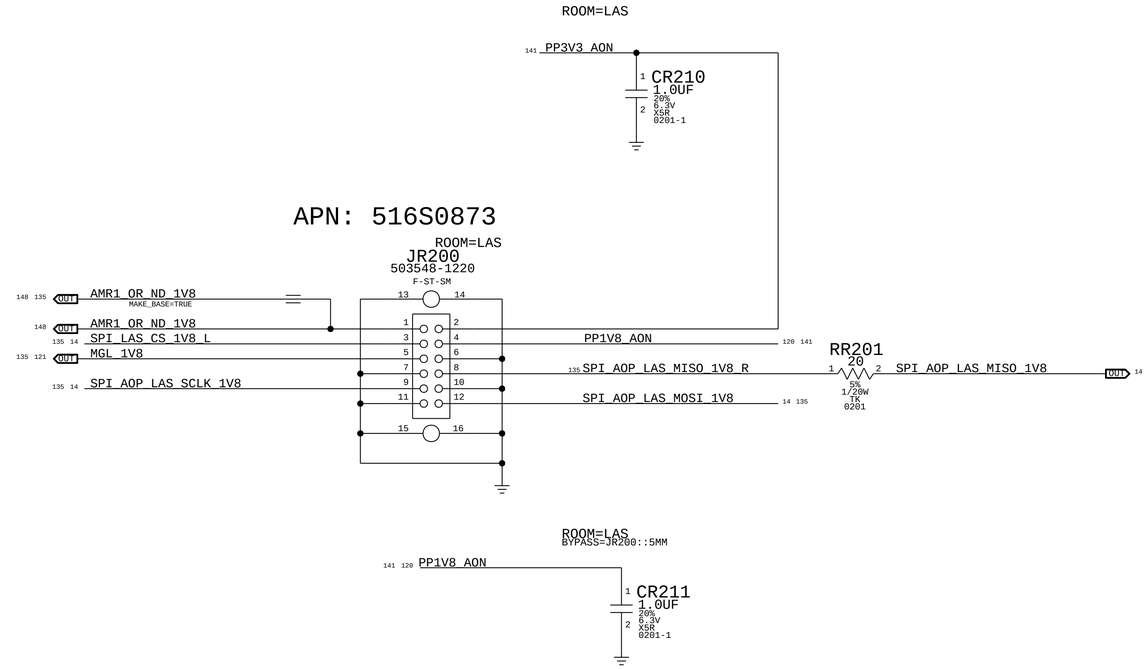
BOM_COST_GROUP=DISPLAY

*** OK2INTEGRATE ***



CURRENT PER RAIL

RAIL	TYPICAL	PEAK
1.2 S2	22UA	1.2MA
1.8 AON	30UA	8 MA
3.3 AON	1UA	10 MA

BOM_COST_GROUP=SOC

PAGE TITLE
SECDIS: LID ANGLE SENSOR

Apple Inc.

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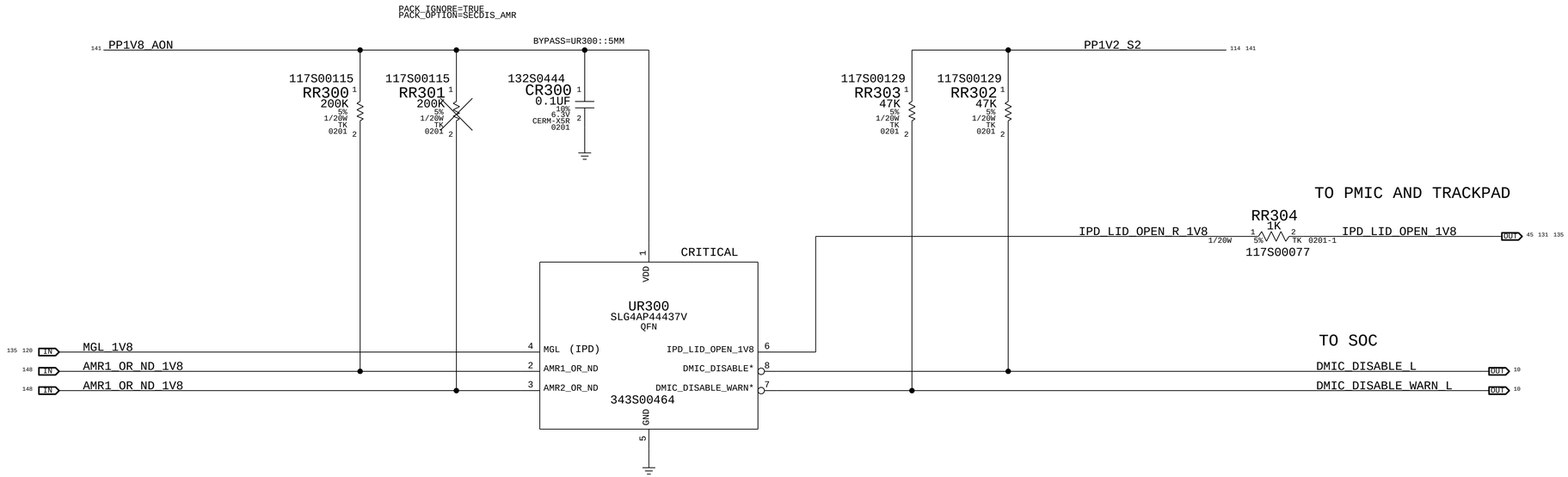
*** OK2INTEGRATE ***

LID SECDIS LOGIC



BOM_COST_GROUP=SOC

PAGE TITLE
SECDIS: SAK

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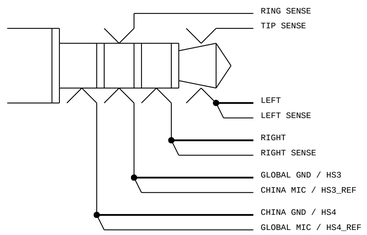
*** OK2INTEGRATE ***

CARLOW CODEC I2C ADDRESS	
ADDR PIN	ADDRESS
0R TO GND	0X48
100K TO GND	0X49
100K TO VDDIO	0X4A
0R TO VDDIO	0X4B <--

AUDIO JACK PINOUT



TO / FROM
AUDIO JACK
CONNECTOR

NOTES:

- SEE TEST POINT SIGNALS & LOCATIONS ON REF DESIGN PAGE 1

- THE FOLLOWING SIGNALS SHOULD HAVE A LOW DCR PATH:
  - VP SUPPLY
  - VCP SUPPLY
  - AUDIO_JACK_LEFT/RIGHT_OUT
  - AUDIO_JACK_GB/CH_GND

- GB_MIC SIGNAL CONNECTS TO CH_GND AT A/J CONNECTOR.
  CH_MIC SIGNAL CONNECTS TO GB_GND AT A/J CONNECTOR.

- VP SUPPLY RAIL ACCEPTS 3.0V TO 5.25V AND NEEDS TO
  COME UP FIRST AND TURN OFF LAST (NEED TO STAY UP
  WHEN THE OTHER RAILS GO DOWN)
  VP CURRENT CONSUMPTION WITH PART IN LOWEST POWER STATE:
  3.1UA (1V8 OFF, RST# LOW)
  TBD (1V8 ON, RST# LOW)
  37UA (1V8 OFF, RST# HIGH)

CARLOW B0 SILICON

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO JACK CODEC

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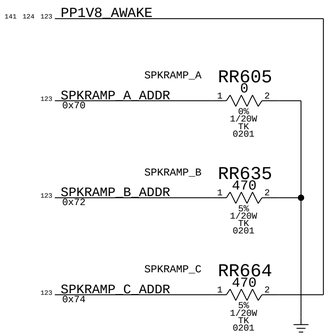
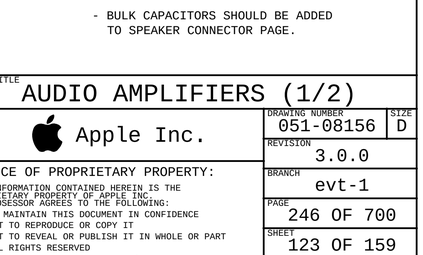
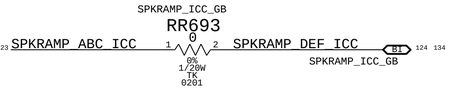




THIS RESISTOR TIES ICC SIGNAL
BETWEEN AMPS A,B,C AND AMPS D,E,F:
0R --> GLOBAL ICC (ABCDEF)
DNE --> LOCAL ICC (ABC, DEF)



NOTES:
- SEE TEST POINTS SIGNALS AND LOCATIONS ON REF DESIGN PAGE 1.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- PVDD_SNS XW SHOULD BE LOCATED BY MAIN PBUS SHAPE.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.
- BULK CAPACITORS SHOULD BE ADDED TO SPEAKER CONNECTOR PAGE.

PAGE TITLE: AUDIO AMPLIFIERS (1/2)

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*** OK2INTEGRATE ***

AMP D

PP1V8_AWAKE
PP1V2_AWAKE
PP3V8_AON
MAX CURRENT EDC = 1A (PER AMP)
PPBUS_AON_SPKRAMP_DEF
MAX CURRENT EDC = 4A (PER AMP)
SPKRAMP_D_DREG
CR700 1.0UF 20% 6.3V X5R 0201-1
CR701 1.0UF 20% 6.3V X5R 0201-1
CR702 1.0UF 20% 6.3V X5R 0201-1
CR703 0.1UF 10% 25V X5R 0201
CR704 10UF 20% 25V X5R-CERM 0603
CR705 10UF 20% 25V X5R-CERM 0603
CR706 0.1UF 10% 25V X5R 0201
CR707 10UF 20% 10V X5R-CERM 0402-7
XWR700 SHORT-10L-0.1MM-SM * SEE NOTE
SPKRAMP_D_PVDD_SNS
SPKRAMP_D_VSENSEP * SEE NOTE
SPKRAMP_D_VSENSEN
UR700 SN012776B0YBH DSBGA SPKRAMP_D
TAWANG B0
I2C_SPKRAMP_R_SCL
I2C_SPKRAMP_R_SDA
SPKRAMP_D_ADDR
TDM_SPKRAMP_R_BCLK
TDM_SPKRAMP_R_FSYNC
TDM_SPKRAMP_R_R2D
TDM_SPKRAMP_R_D2R
SPKRAMP_DEF_ICC_R
TP_SPKRAMP_D_LV_EN
SPKRAMP_INT_L
SPKRAMP_RESET_L
RR700 33 5% 1/20W TK 0201 TDM_SPKRAMP_D_D2R_R
RR701 33 5% 1/20W TK 0201 SPKRAMP_D_ICC_R
SPKRAMP_D_BOOTP CR708 0.1UF 10% 25V X5R 0201
SPKRAMP_D_OUTP_R
SPKRAMP_D_OUTN_R
SPKRAMP_D_BOOTN CR709 0.1UF 10% 25V X5R 0201
SPKRAMP_D BYPASS=UR700.B2:B3:10MM NO_XNET_CONNECTION=1
RR702 0 1% 1/16W TK 0603 1/5W
RR703 0 1% 1/16W TK 0603 1/5W
SPKRAMP_D_OUTP * SEE NOTE
SPKRAMP_D_OUTN * SEE NOTE
CR710 12PF 5% 25V CERM 0201 OMIT_TABLE
CR711 12PF 5% 25V CERM 0201 OMIT_TABLE
RR705 2.2K 5% 1/20W TK 0201 SPKRAMP_D_ADDR 0X76
RR734 2.2K 5% 1/20W TK 0201 SPKRAMP_E_ADDR 0X78
RR765 10K 5% 1/20W TK 0201 SPKRAMP_F_ADDR 0X7A
RR706 0 0% 1/20W TK 0201 SPKRAMP_DEF_ICC SPKRAMP_DEF_ICC_R
RR707 0 0% 1/20W TK 0201 NOSTUFF

RR706 TO REDUCE STUB LENGTH FOR LOCAL ICC OPERATION. RR707 PROVIDES THE OPTION TO GND FLOATING SPKRAMP_DEF_ICC TRACE

AMP E

PP1V8_AWAKE
PP1V2_AWAKE
PP3V8_AON
PPBUS_AON_SPKRAMP_DEF
SPKRAMP_E_DREG
CR730 1.0UF 20% 6.3V X5R 0201-1
CR731 1.0UF 20% 6.3V X5R 0201-1
CR732 1.0UF 20% 6.3V X5R 0201-1
CR733 0.1UF 10% 25V X5R 0201
CR734 10UF 20% 25V X5R-CERM 0603
CR735 10UF 20% 25V X5R-CERM 0603
CR736 0.1UF 10% 25V X5R 0201
CR737 10UF 20% 10V X5R-CERM 0402-7
XWR701 SHORT-10L-0.1MM-SM * SEE NOTE
SPKRAMP_E_PVDD_SNS
SPKRAMP_E_VSENSEP * SEE NOTE
SPKRAMP_E_VSENSEN
UR730 SN012776B0YBH DSBGA SPKRAMP_E
TAWANG B0
I2C_SPKRAMP_R_SCL
I2C_SPKRAMP_R_SDA
SPKRAMP_E_ADDR
TDM_SPKRAMP_R_BCLK
TDM_SPKRAMP_R_FSYNC
TDM_SPKRAMP_R_R2D
TDM_SPKRAMP_R_D2R
SPKRAMP_DEF_ICC_R
TP_SPKRAMP_E_LV_EN
SPKRAMP_INT_L
SPKRAMP_RESET_L
RR730 33 5% 1/20W TK 0201 TDM_SPKRAMP_E_D2R_R
RR731 33 5% 1/20W TK 0201 SPKRAMP_E_ICC_R
SPKRAMP_E_BOOTP CR738 0.1UF 10% 25V X5R 0201
SPKRAMP_E_OUTP_R
SPKRAMP_E_OUTN_R
SPKRAMP_E_BOOTN CR739 0.1UF 10% 25V X5R 0201
SPKRAMP_E BYPASS=UR730.B2:B3:10MM NO_XNET_CONNECTION=1
RR732 0 1% 1/16W TK 0603 1/5W
RR733 0 1% 1/16W TK 0603 1/5W
SPKRAMP_E_OUTP * SEE NOTE
SPKRAMP_E_OUTN * SEE NOTE
CR740 12PF 5% 25V CERM 0201 OMIT_TABLE
CR741 12PF 5% 25V CERM 0201 OMIT_TABLE

AMP F

PP1V8_AWAKE
PP1V2_AWAKE
PP3V8_AON
PPBUS_AON_SPKRAMP_DEF
SPKRAMP_F_DREG
CR760 1.0UF 20% 6.3V X5R 0201-1
CR761 1.0UF 20% 6.3V X5R 0201-1
CR762 1.0UF 20% 6.3V X5R 0201-1
CR763 0.1UF 10% 25V X5R 0201
CR764 10UF 20% 25V X5R-CERM 0603
CR765 10UF 20% 25V X5R-CERM 0603
CR766 0.1UF 10% 25V X5R 0201
CR767 10UF 20% 10V X5R-CERM 0402-7
XWR702 SHORT-10L-0.1MM-SM * SEE NOTE
SPKRAMP_F_PVDD_SNS
SPKRAMP_F_VSENSEP * SEE NOTE
SPKRAMP_F_VSENSEN
UR760 SN012776B0YBH DSBGA SPKRAMP_F
TAWANG B0
I2C_SPKRAMP_R_SCL
I2C_SPKRAMP_R_SDA
SPKRAMP_F_ADDR
TDM_SPKRAMP_R_BCLK
TDM_SPKRAMP_R_FSYNC
TDM_SPKRAMP_R_R2D
TDM_SPKRAMP_R_D2R
SPKRAMP_DEF_ICC_R
TP_SPKRAMP_F_LV_EN
SPKRAMP_INT_L
SPKRAMP_RESET_L
RR760 33 5% 1/20W TK 0201 TDM_SPKRAMP_F_D2R_R
RR761 33 5% 1/20W TK 0201 SPKRAMP_F_ICC_R
SPKRAMP_F_BOOTP CR768 0.1UF 10% 25V X5R 0201
SPKRAMP_F_OUTP_R
SPKRAMP_F_OUTN_R
SPKRAMP_F_BOOTN CR769 0.1UF 10% 25V X5R 0201
SPKRAMP_F BYPASS=UR760.B2:B3:10MM NO_XNET_CONNECTION=1
RR762 0 1% 1/16W TK 0603 1/5W
RR763 0 1% 1/16W TK 0603 1/5W
SPKRAMP_F_OUTP * SEE NOTE
SPKRAMP_F_OUTN * SEE NOTE
CR770 12PF 5% 25V CERM 0201 OMIT_TABLE
CR771 12PF 5% 25V CERM 0201 OMIT_TABLE

NOTES:
- SEE TEST POINTS SIGNALS AND LOCATIONS ON REF DESIGN PAGE 1.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- PVDD_SNS XW SHOULD BE LOCATED BY MAIN PBUS SHAPE.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.
- BULK CAPACITORS SHOULD BE ADDED TO SPEAKER CONNECTOR PAGE.

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO AMPLIFIERS (2/2)

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LEFT AUDIO SPEAKER CONNECTOR

NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1

123 OUT SPKRAMP_A_VSENSEP — SHORT-16L-0.1MM-SM 1 2 XWR800 — PLACE_NEAR=JR800.5:10MM
123 OUT SPKRAMP_A_VSENSEN — SHORT-16L-0.1MM-SM 1 2 XWR801 — PLACE_NEAR=JR800.6:10MM
123 OUT SPKRAMP_B_VSENSEP — SHORT-16L-0.1MM-SM 1 2 XWR802 — PLACE_NEAR=JR800.7:10MM
123 OUT SPKRAMP_B_VSENSEN — SHORT-16L-0.1MM-SM 1 2 XWR803 — PLACE_NEAR=JR800.8:10MM
123 OUT SPKRAMP_C_VSENSEP — SHORT-16L-0.1MM-SM 1 2 XWR804 — PLACE_NEAR=JR800.1:10MM
123 OUT SPKRAMP_C_VSENSEN — SHORT-16L-0.1MM-SM 1 2 XWR805 — PLACE_NEAR=JR800.2:10MM

L Woofer 1
L Woofer 2
L Tweeter

135 125 123 IN SPKRAMP_A_OUTP
135 125 123 IN SPKRAMP_A_OUTN
135 125 123 IN SPKRAMP_B_OUTP
135 125 123 IN SPKRAMP_B_OUTN
135 125 123 IN SPKRAMP_C_OUTP
135 125 123 IN SPKRAMP_C_OUTN
135 125 6 OUT SPKR_ID0

516S00787
JR800
247129004101829
F-ST-SM

13, 9, 10
135 125 123 SPKRAMP_A_OUTP — 5 PWR 6 — SPKRAMP_A_OUTN 123 125 135
135 125 123 SPKRAMP_C_OUTP — 1 PWR 2 — SPKRAMP_C_OUTN 123 125 135
135 125 6 SPKR_ID0 — 3 PWR 4
135 125 123 SPKRAMP_B_OUTP — 7 PWR 8 — SPKRAMP_B_OUTN 123 125 135
11, 12, 14

LEFT AMPLIFIERS BULK CAPACITANCE

PPBUS_AON_SPKRAMP_ABC 123 125 142
CR800 33UF 20% 16V TANT CASE-T
CR801 33UF 20% 16V TANT CASE-T
CR802 33UF 20% 16V TANT CASE-T
CR803 33UF 20% 16V TANT CASE-T

PPBUS_AON_SPKRAMP_ABC 123 125 142
CR804 33UF 20% 16V TANT CASE-T
CR805 33UF 20% 16V TANT CASE-T
CR806 33UF 20% 16V TANT CASE-T
CR807 33UF 20% 16V TANT CASE-T

RIGHT AMPLIFIERS BULK CAPACITANCE

PPBUS_AON_SPKRAMP_DEF 124 125 142
CR850 33UF 20% 16V TANT CASE-T
CR851 33UF 20% 16V TANT CASE-T
CR852 33UF 20% 16V TANT CASE-T
CR853 33UF 20% 16V TANT CASE-T

PPBUS_AON_SPKRAMP_DEF 124 125 142
CR854 33UF 20% 16V TANT CASE-T
CR855 33UF 20% 16V TANT CASE-T
CR856 33UF 20% 16V TANT CASE-T
CR857 33UF 20% 16V TANT CASE-T

RIGHT AUDIO SPEAKER CONNECTOR

NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1

124 OUT SPKRAMP_D_VSENSEP — SHORT-16L-0.1MM-SM 1 2 XWR850 — PLACE_NEAR=JR850.5:10MM
124 OUT SPKRAMP_D_VSENSEN — SHORT-16L-0.1MM-SM 1 2 XWR851 — PLACE_NEAR=JR850.6:10MM
124 OUT SPKRAMP_E_VSENSEP — SHORT-16L-0.1MM-SM 1 2 XWR852 — PLACE_NEAR=JR850.7:10MM
124 OUT SPKRAMP_E_VSENSEN — SHORT-16L-0.1MM-SM 1 2 XWR853 — PLACE_NEAR=JR850.8:10MM
124 OUT SPKRAMP_F_VSENSEP — SHORT-16L-0.1MM-SM 1 2 XWR854 — PLACE_NEAR=JR850.3:10MM
124 OUT SPKRAMP_F_VSENSEN — SHORT-16L-0.1MM-SM 1 2 XWR855 — PLACE_NEAR=JR850.4:10MM

R Woofer 1
R Woofer 2
R Tweeter

135 125 124 IN SPKRAMP_D_OUTP
135 125 124 IN SPKRAMP_D_OUTN
135 125 124 IN SPKRAMP_E_OUTP
135 125 124 IN SPKRAMP_E_OUTN
135 125 124 IN SPKRAMP_F_OUTP
135 125 124 IN SPKRAMP_F_OUTN
135 125 6 OUT SPKR_ID1

516S00787
JR850
247129004101829
F-ST-SM

13, 9, 10
135 125 124 SPKRAMP_D_OUTP — 5 PWR 6 — SPKRAMP_D_OUTN 124 125 135
135 125 6 SPKR_ID1 — 1 PWR 2
135 125 124 SPKRAMP_F_OUTP — 3 PWR 4 — SPKRAMP_F_OUTN 124 125 135
135 125 124 SPKRAMP_E_OUTP — 7 PWR 8 — SPKRAMP_E_OUTN 124 125 135
11, 12, 14

DUMMY 0201 CAPS

PLACE_NEAR=UR600:5mm — CR860 10UF 20% 10V X5R-CERM 0402-7 — CKPLUS_WAIVE=TERMSHORTED
PLACE_NEAR=UR600:5mm — CR861 10UF 20% 10V X5R-CERM 0402-7 — CKPLUS_WAIVE=TERMSHORTED
PLACE_NEAR=UR600:5mm — CR862 10UF 20% 10V X5R-CERM 0402-7 — CKPLUS_WAIVE=TERMSHORTED

BOM_COST_GROUP=AUDIO

PAGE TITLE
AUDIO CONNECTORS: AMPS

Apple Inc.

DRAWING NUMBER 051-08156 SIZE D
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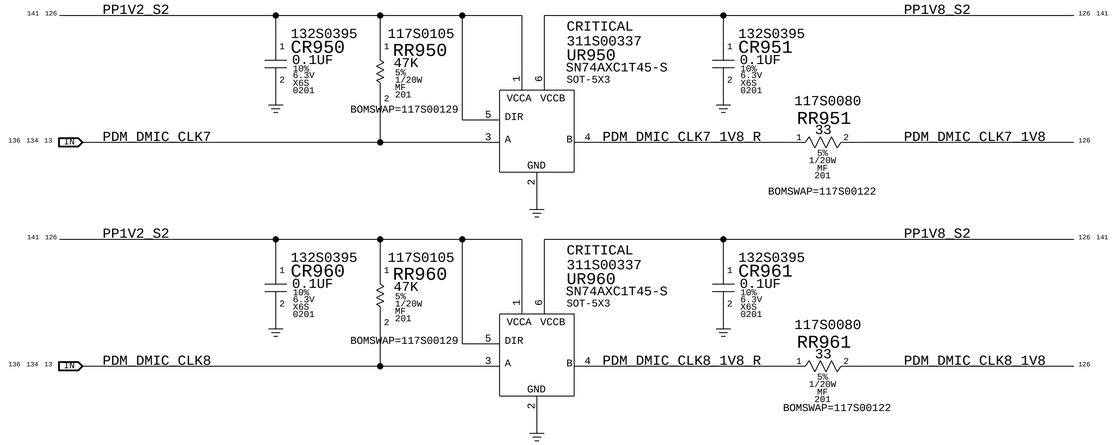
LEVEL SHIFTERS: DMIC CLOCK

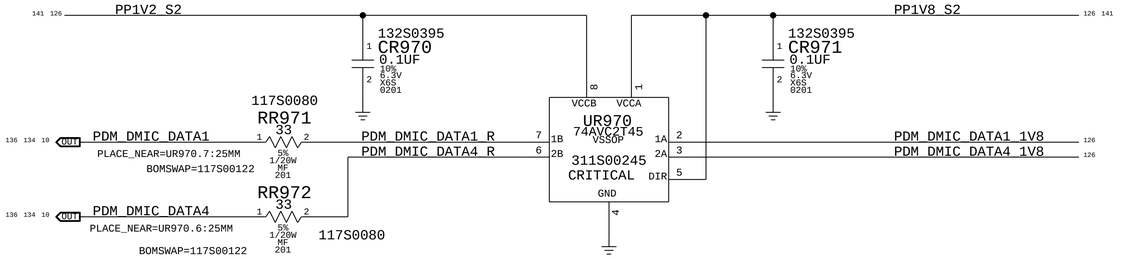
TWO SEPARATE SINGLE BIT LS FOR XTALK CONCERNS <RDAR://70058941> -- MAY CHANGE TO DUAL SHIFTER



LEVEL SHIFTER: DMIC DATA

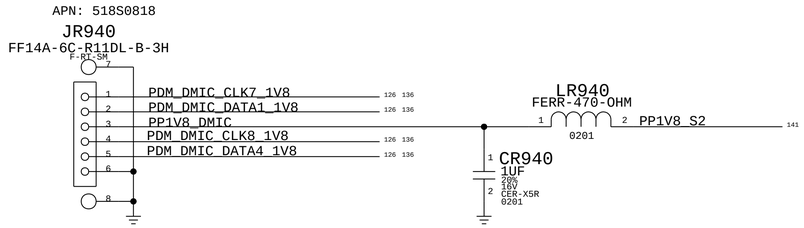
HIGH ON DIR IS A -> B

BOTH A AND B SIDE CAN BE ANY VOLTAGE FROM 0.8 TO 3.6

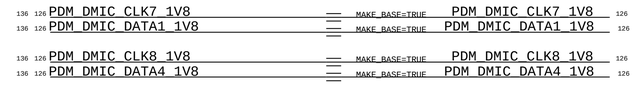


Digital Mic Flex Connector

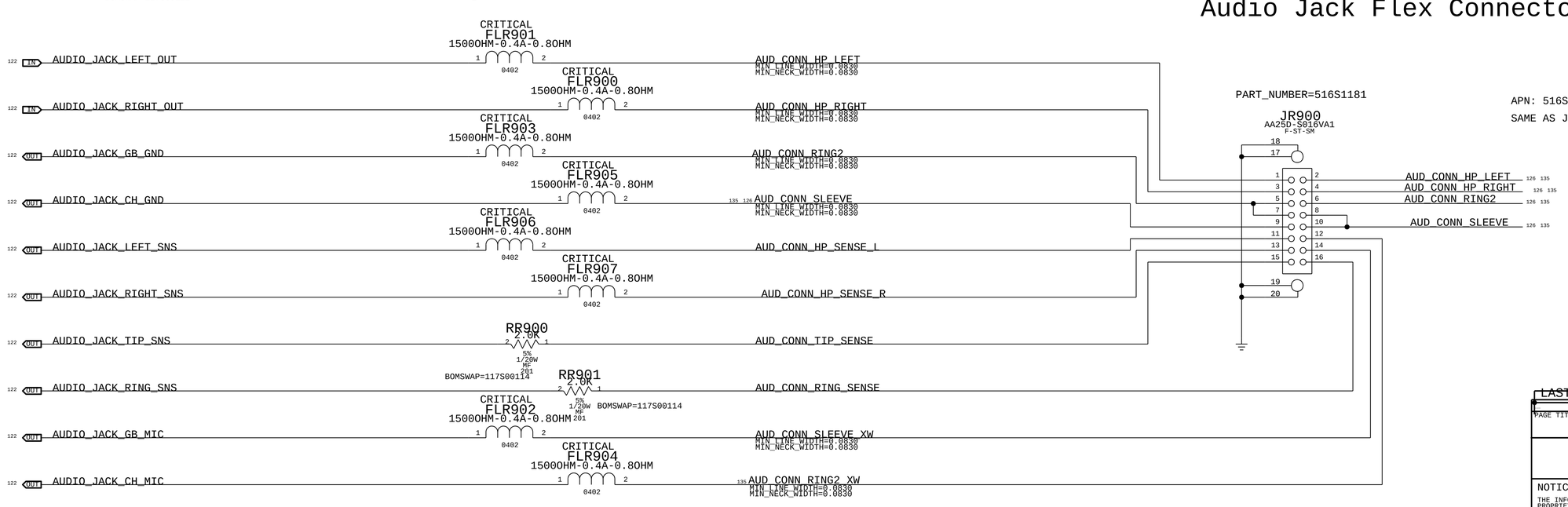
APN: 518S0818



TODO: Check if zero ohms between connector an SECDIS are required



Audio Jack Flex Connector



LAST CHANGE: Wed Feb 18 17:12:24 2015

PAGE TITLE

Audio Flex Connectors

Apple Inc.

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REVISION 3.0.0

BRANCH evt-1

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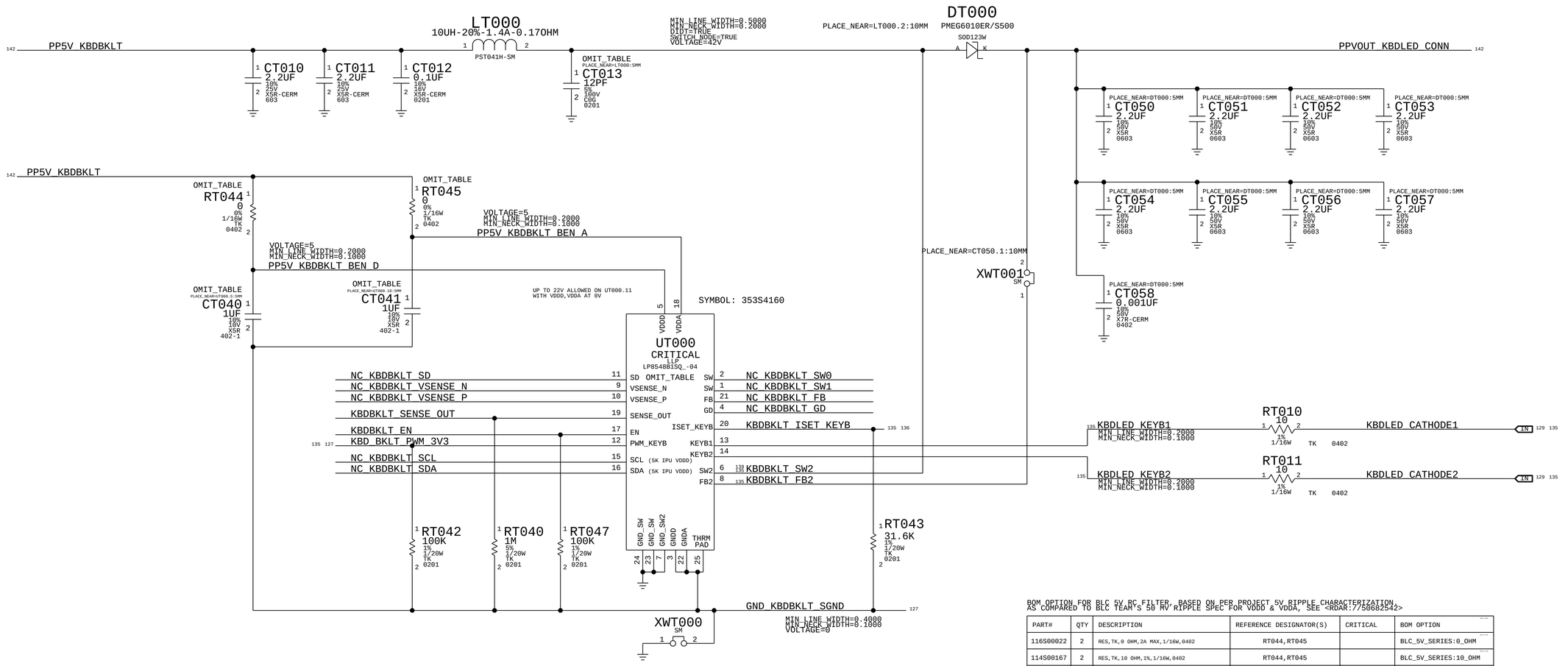
*** OK2INTEGRATE ***

BEN IC: KEYBOARD LED DRIVER

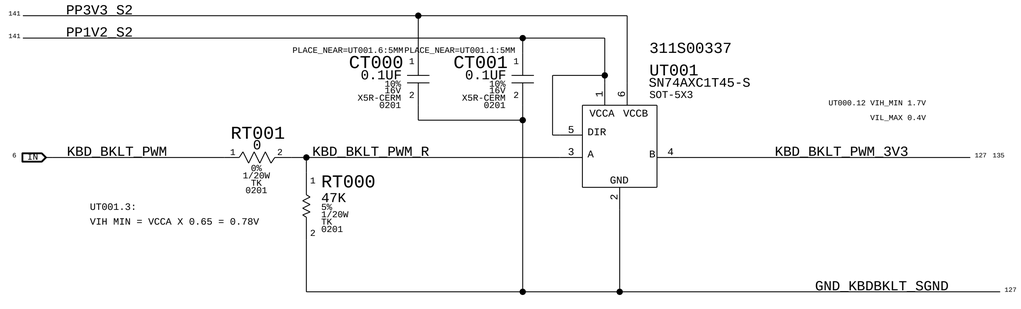


BOM OPTION FOR BLC 5V RC FILTER, BASED ON PER PROJECT 5V RIPPLE CHARACTERIZATION, AS COMPARED TO BLC TEAM'S 50 MV RIPPLE SPEC FOR VDDD & VDDA, SEE <RDAR:/750682542>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S00022	2	RES,TK,0 OHM,2A MAX,1/16W,0402	RT044,RT045		BLC_5V_SERIES:0_OHM
114S00167	2	RES,TK,10 OHM,1%,1/16W,0402	RT044,RT045		BLC_5V_SERIES:10_OHM
138S0614	2	CAP,CER,X5R,1UF,10%,10V,0402	CT040,CT041		BLC_5V_CAP:1_UF
138S00070	2	CAP,CER,X5R,4.7UF,20%,25V,0402	CT040,CT041		BLC_5V_CAP:4P7_UF

KEYBOARD BKLT PWM LEVEL-SHIFTER

UT001.4: VOH_MIN = 2.3V
VOL_MAX = 0.1V @ PWM_KEYB I_MAX OF 1UA



BEN IC VERSION 4 VS 6 DEPENDS ON WHICH VERSION OF JERRY IC IS ON THE PANEL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S01615	1	IC,LP8548B1-04,DC/DC CVTR,BST,AIZU,QFN-24	UT000		BLC_BEN_IC:V4
353S01685	1	IC,LP8548B1-06,DC/DC CVTR,BST,QFN24	UT000		BLC_BEN_IC:V6

ALTERNATE PART FOR BEN IC VERSION 4

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S4160	353S01615	BLC_BEN_IC:V4	ANY	RECOMMENDED BY LOUISA

KEYBOARD SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00141	1	CAP,C0G,12PF,5%,100V,0201	CT013		BLC_KBD_SW_NODE_DESENSE

BOM_COST_GROUP=DISPLAY

PAGE TITLE: BEN: KEYBD BKLT

Apple Inc.

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*** OK2PLACE ***

TO/FROM TRACKPAD

I2C_KBD_SCL — RT110 33 5% 1/20W TK 0201 — CKPLUS_WAIVE=I2C_PULLUP — IOXP_I2C_SCL
PLACE_NEAR=JT400.8:10MM
DZT110 5.5V-0.28PF 0201-THICKSTNCL

I2C_KBD_SDA — RT111 33 5% 1/20W TK 0201 — CKPLUS_WAIVE=I2C_PULLUP — IOXP_I2C_SCL
PLACE_NEAR=JT400.9:10MM
DZT111 5.5V-0.28PF 0201-THICKSTNCL

KBD_INT_L — RT112 33 5% 1/20W TK 0201 — IOXP2_INT_L
PLACE_NEAR=JT400.9:10MM
DZT112 5.5V-0.28PF 0201-THICKSTNCL

KEYBAORD IOX1

TIE TO SAME VOLTAGE AS TPAD CONTROLLER, EITHER 1V8 OR 3V3
Powered by 3.3V IPD LDO

PP3V3_S2_IPD
CT110 1.0UF 20% 6.3V X5R 0201-1 138S0692
CT112 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

ALL PLATFORMS CONNECT TO 1V8
PP1V85_S2_KBD
CT113 0.1UF 10% 6.3V CERM-X5R 0201 132S0444
CT114 10UF 20% 10V X5R-CERM 0402-7

IOX1 DOESN'T SEND THE INTERRUPT INSTEAD, IOX2 SENDS INT WHEN A KEY IS PRESSED

IOXP1_INT_L
CT111 0.1UF 10% 6.3V CERM-X5R 0201 132S0444
IOXP1_RESET_L

UT101 PCAL6416A HWQFN
311S0665
WRITE: 0X40
READ: 0X41

P0_0	KBD_DRIVE_Y0	
P0_1	KBD_DRIVE_Y1	
P0_2	KBD_DRIVE_Y2	
P0_3	KBD_DRIVE_Y3	
P0_4	KBD_DRIVE_Y4	
P0_5	KBD_DRIVE_Y5	
P0_6	KBD_DRIVE_Y6	
P0_7	KBD_DRIVE_Y7	
P1_0	KBD_DRIVE_Y8	
P1_1	KBD_DRIVE_Y9	
P1_2	KBD_DRIVE_Y10	
P1_3	KBD_DRIVE_Y11	
P1_4	NC	
P1_5	KBD_ID_DETECT2	
P1_6	KBD_LAYOUT_DETECT	
P1_7	CAPSLOCK_LED_EN	

ADD 4X NEW IO_Y8,Y9,Y10,Y11 FOR 3314/316 AND 34-PIN KBD
CONNECT THE NEW IO FROM KBD ZIF CONN TO NEARBY ESD DIODES

KEYBAORD IOX2

TIE TO SAME VOLTAGE AS TPAD CONTROLLER, EITHER 1V8 OR 3V3
Powered by 3.3V IPD LDO

PP3V3_S2_IPD
RT121 100K 5% 1/20W TK 0201
CT120 1.0UF 20% 6.3V X5R 0201-1 138S0692
CT121 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

ALL PLATFORMS CONNECT TO 1V8
PP1V85_S2_KBD
CT122 0.1UF 10% 10V X5R-CERM 0201

IOXP2_ADDR
IOXP2_RESET_L
CT123 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

UT102 PCAL6416A HWQFN
311S0665
WRITE: 0X42
READ: 0X43

P0_0	KBD_SENSE_X0	
P0_1	KBD_SENSE_X1	
P0_2	KBD_SENSE_X2	
P0_3	KBD_SENSE_X3	
P0_4	KBD_SENSE_X4	
P0_5	KBD_SENSE_X5	
P0_6	KBD_SENSE_X6	
P0_7	KBD_SENSE_X7	
P1_0	KBD_SENSE_X8	
P1_1	KBD_SENSE_X9	
P1_2	KBD_SENSE_X10	
P1_3	KBD_SENSE_X11	
P1_4	KBD_SENSE_X12	
P1_5	KBD_CONTROL_L	
P1_6	KBD_LEFT_OPTION_L	
P1_7	KBD_RIGHT_SHIFT_L	

3.3V RSLOC ISOLATION KEYS/ASIC RESET

PP3V3_AON
CT150 1.0UF 20% 6.3V X5R 0201-1 138S0692 — PLACE_NEAR=UT103.10:5MM
CT151 0.1UF 10% 6.3V CERM-X5R 0201 132S0444 — PLACE_NEAR=UT103.10:2MM

PP1V85_S2_KBD
RT190 0 0% 1/20W TK 0201

UT103 SLG4AP45306 QFN-THICKSTNCL
IN_X: VIH_MIN 2.0V VIL_MAX 0.8V 100K IPD
OUT_X: VOH_MIN 2.4V VOL_MAX 0.4V 12.5K IPU OE
VDD (2.97 < VDD < 3.63)

OUT123_EN

KBD_RIGHT_SHIFT_KEY	IN_1	OUT_1 KBD_RIGHT_SHIFT_L
KBD_LEFT_OPTION_KEY	IN_2	OUT_2 KBD_LEFT_OPTION_L
KBD_CONTROL_KEY	IN_3	OUT_3 KBD_CONTROL_L
		OUT_ALL*

RT152 33 1% 1/20W TK 0201
RSLOC_RST_L — PMU_RSLOC_RST_L

3V3 KBD CONN SERIES R

KBD DRI REQUEST, TO MEASURE CAPSLOCK LED CURRENT

PP3V3_AON — RT103 0 0% 1/20W TK 0201 — PP3V3_AON_KBD_CONN
TO KBD CONN AND ESD
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=3.3V

ID_DETECT SERIES R

KBD_LAYOUT_DETECT — RT117 1K 5% 1/20W TK 0201-1 — KBD_ID1
KBD_ID_1 PIN ON KBD CONNECTOR
ANSI: NO CONNECT
ISO: TIED HIGH TO PP1V8
JIS: TIED LOW TO GND

KBD_ID_DETECT2 — RT119 1K 5% 1/20W TK 0201-1 — KBD_ID2
KBD_ID_2 PIN ON KBD CONNECTOR
TIED LOW TO GND FOR 34-PIN NEW KBD

1.85V LDO (LOCAL TO IPD)

PP3V8_IPDLDO_VIN
CT1A1 1.0UF 20% 6.3V X5R 0201-1
IPD_PWR_EN

UT1A0 LP5907SNX-1.825 X2SON-COMBO-THICKSTNCL
VIN, EN, VOUT, GND EPAD

PP1V85_S2_KBD
CT1A0 1.0UF 20% 6.3V X5R 0201-1
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.85V

CAPSLOCK LED DRIVER

NOTE: THIS CAN BE THE SAME RAIL AS THE CAPSLOCK LED, OR IT CAN BE A RAIL THAT COMES UP AFTER

CURRENT CONTROLLED LED DRIVING FROM J214/J223/J230
DIFFERENT FROM RESISTANCE CONTROL LED DRIVING FROM J152

PP3V3_S2_IPD
CT105 1.0UF 20% 6.3V X5R 0201-1 138S0692

UT105 FAN5622 SSOT23
VIN_MIN 1.2V VIL_MAX 0.4V
R_SET 19.1K 15 MA SINK

CAPSLOCK_LED_EN — RT161 1K 5% 1/20W TK 0201-1 — LED_CTRL
LED_ISET — RT160 19.1K 1% 1/20W TK 0201 <R_SET>
RT162 200K 5% 1/20W TK 0201
LED1 — KBD_LED1 — RT118 1 5% 1/20W TK 0201 — KBD_CAP_CATHODE

PP1V85_S2_KBD

RT130	10K	5% 1/20W TK 0201	KBD_SENSE_X0
RT131	10K	5% 1/20W TK 0201	KBD_SENSE_X1
RT132	10K	5% 1/20W TK 0201	KBD_SENSE_X2
RT133	10K	5% 1/20W TK 0201	KBD_SENSE_X3
RT134	10K	5% 1/20W TK 0201	KBD_SENSE_X4
RT135	10K	5% 1/20W TK 0201	KBD_SENSE_X5
RT136	10K	5% 1/20W TK 0201	KBD_SENSE_X6
RT137	10K	5% 1/20W TK 0201	KBD_SENSE_X7
RT138	10K	5% 1/20W TK 0201	KBD_SENSE_X8
RT139	10K	5% 1/20W TK 0201	KBD_SENSE_X9
RT140	10K	5% 1/20W TK 0201	KBD_SENSE_X10
RT141	10K	5% 1/20W TK 0201	KBD_SENSE_X11
RT142	10K	5% 1/20W TK 0201	KBD_SENSE_X12
RT143	1K	1% 1/20W TK 0201	IOXP2_ADDR

PP3V3_S2_IPD

RT120	10K	5% 1/20W TK 0201	IOXP2_RESET_L
RT122	10K	5% 1/20W TK 0201	IOXP1_RESET_L
RT123	1.3K	1% 1/20W TK 0201	I2C_KBD_SCL
RT124	1.3K	1% 1/20W TK 0201	I2C_KBD_SDA
RT125	100K	5% 1/20W TK 0201	IOXP1_INT_L

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S00879	353S00754	ANY	ALL	rdar://32477358

BOM_COST_GROUP=KEYBOARD

PAGE TITLE: KEYBOARD IOX, SUPPORT

Apple Inc.

DRAWING NUMBER: 051-08156 SIZE: D
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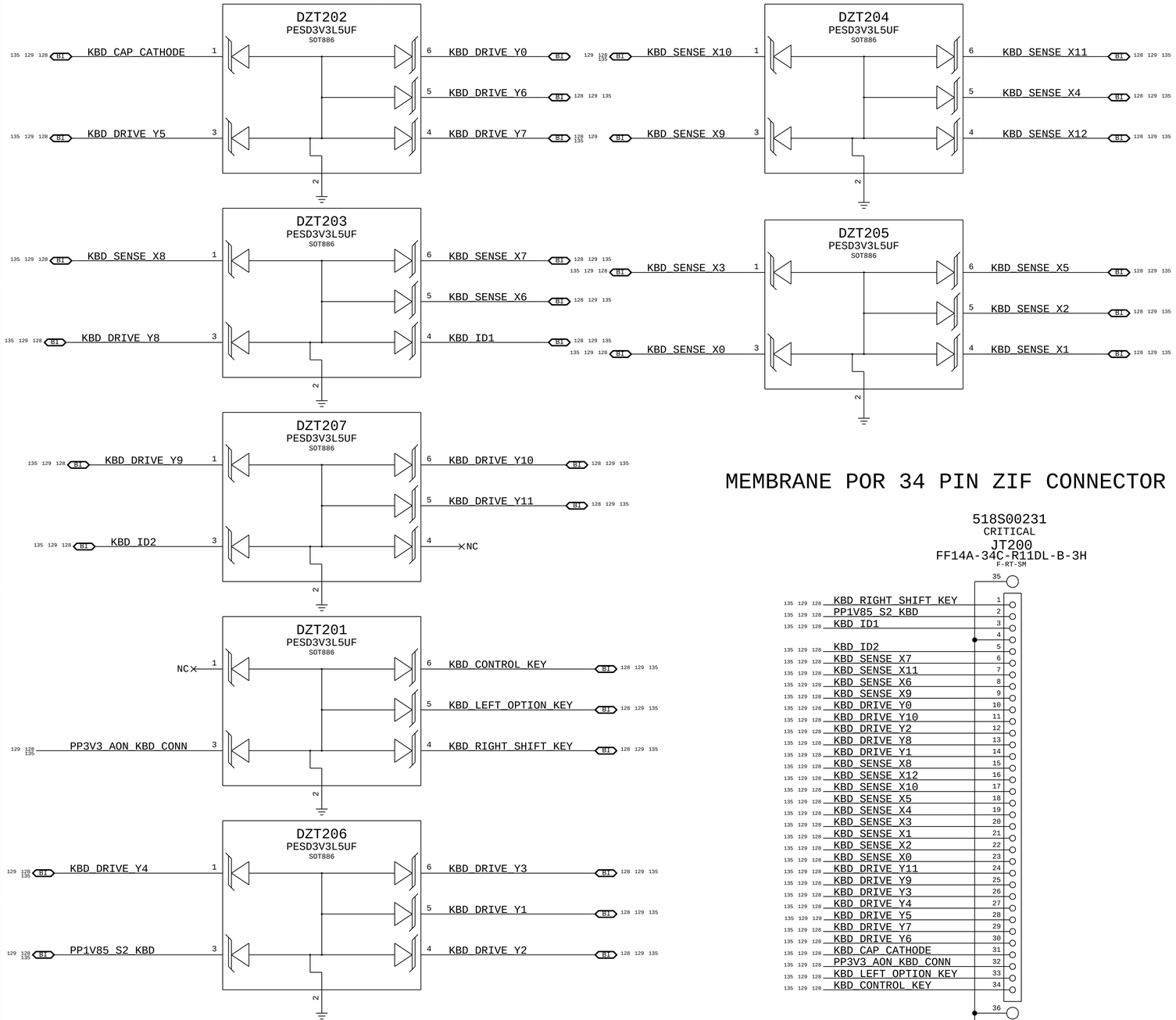
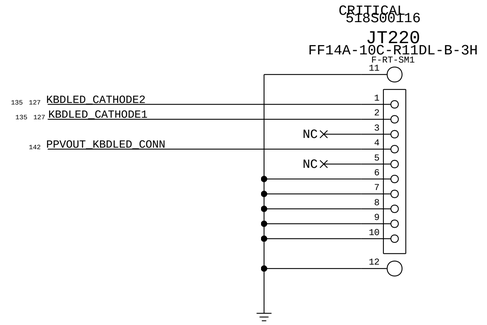
KEYBOARD ESD



MEMBRANE POR 34 PIN ZIF CONNECTOR

Touch ID Connector



BOM_COST_GROUP=KEYBOARD

PAGE TITLE
KEYBOARD SIGNAL CONNECTOR, ESD

Apple Inc.

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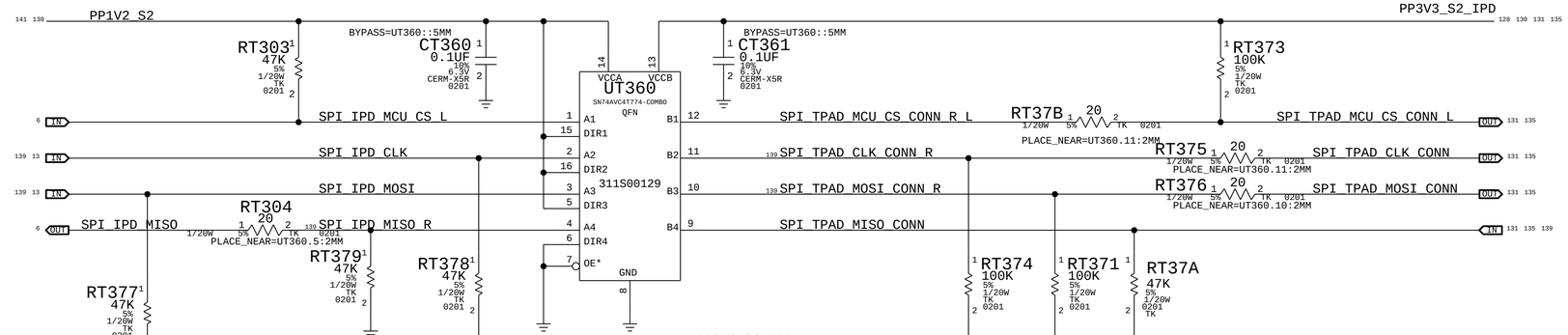
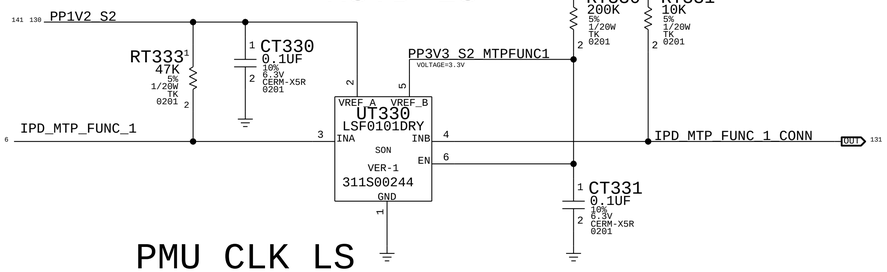
TRACKPAD SPI BUS LEVEL SHIFTER



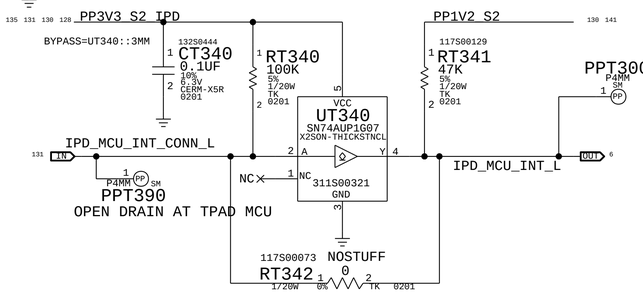
SN74AVC4T774 Truth Table

CTRL INPUTS		OUTPUT CIRCUITS		OPERATION
/OE	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

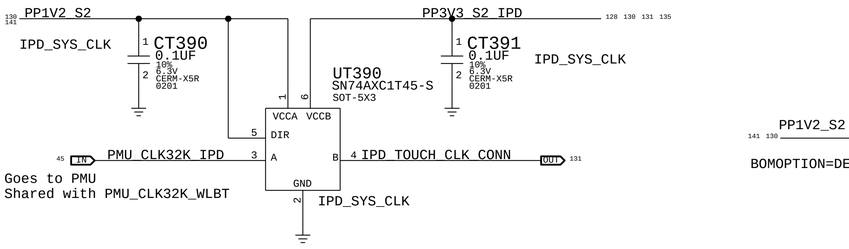
RSVD LS



MCU INTERUPT LS

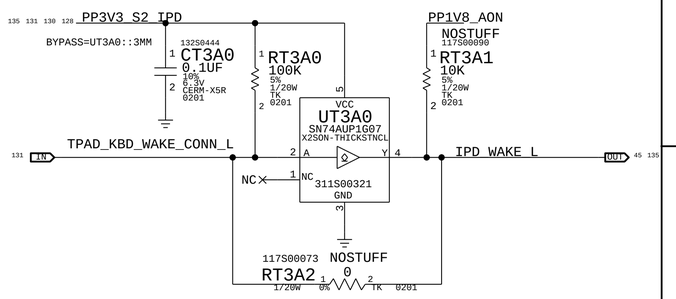


PMU CLK LS

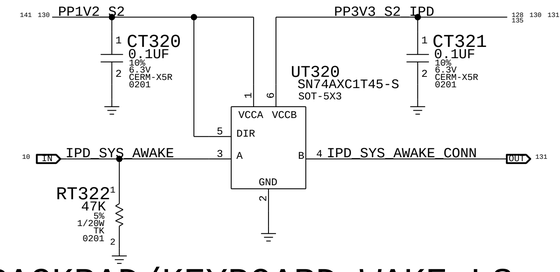


SWD LEVEL SHIFTERS

PP1V8_AON

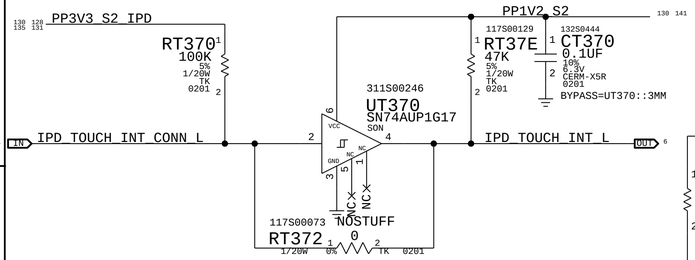


SYS AWAKE LS

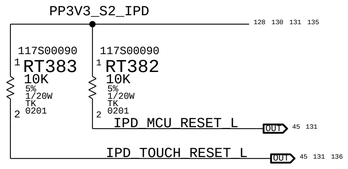


TRACKPAD/KEYBOARD WAKE LS

TOUCH INTERUPT LS



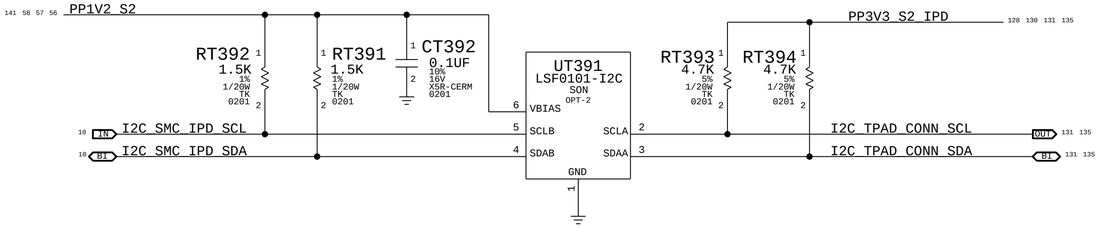
RESET PULL-UPs



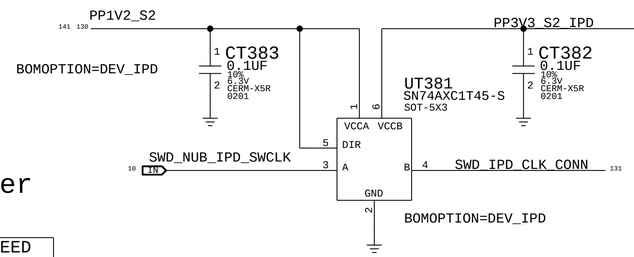
Temp Sensor I2C Level Shifter

SMC_I2C3

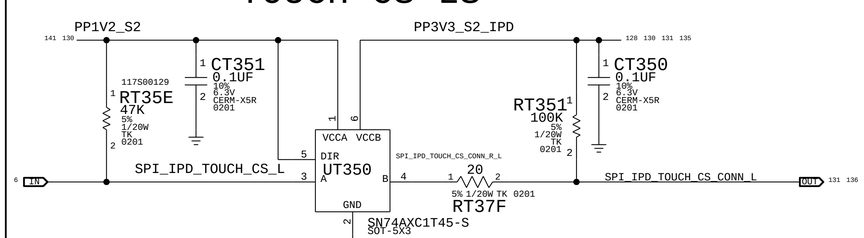
DEVICE	CARD/REFDES	7-BIT	8-BIT	SPEED
Palm Rest Temp	IPD	0X4C	0X98	100KHZ



SWD_NUB_IPD_SWCLK



TOUCH CS LS



BOM_COST_GROUP=TRACKPAD

PAGE TITLE: TRACKPAD SUPPORT 1

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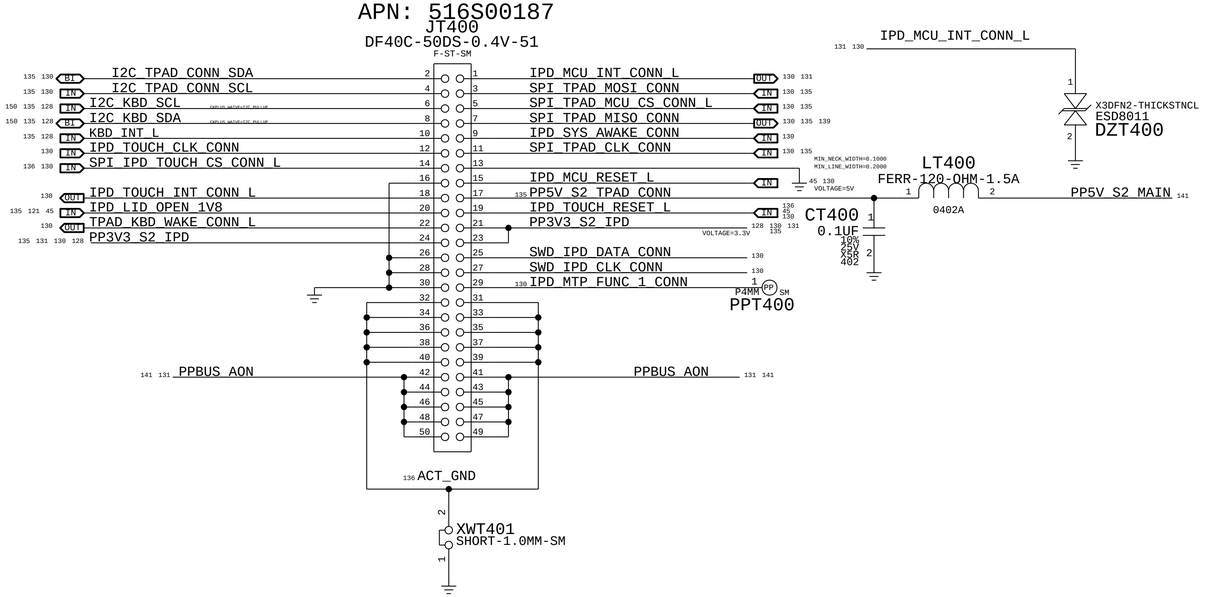
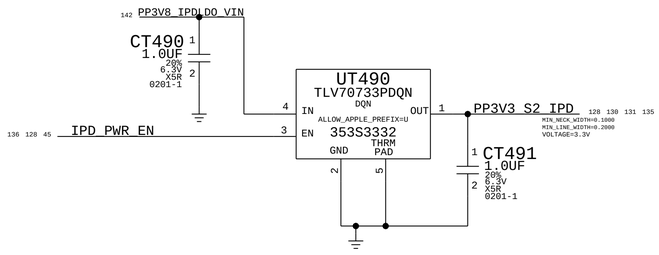
MATES WITH 518S00080
APN: 516S00187



3.3V LDO (LOCAL TO IPD)

Current Limit = 200mA



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PAGE TITLE: TRACKPAD SUPPORT 2

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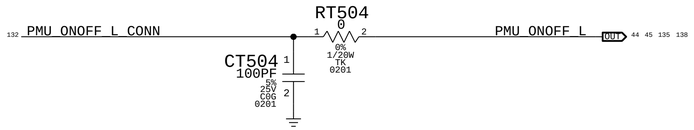
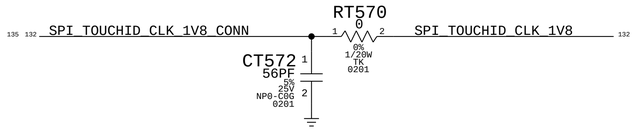
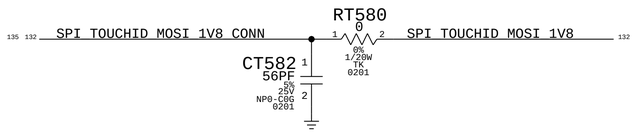
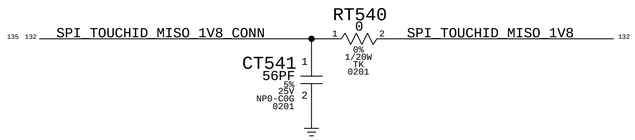
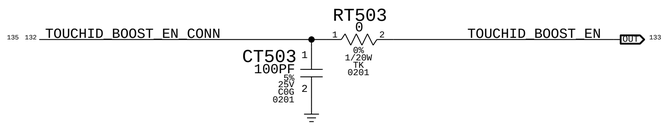
ISOLATE FROM OTHER COMPONENTS / NETS AS MUCH AS POSSIBLE

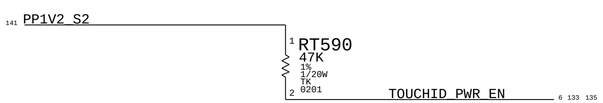


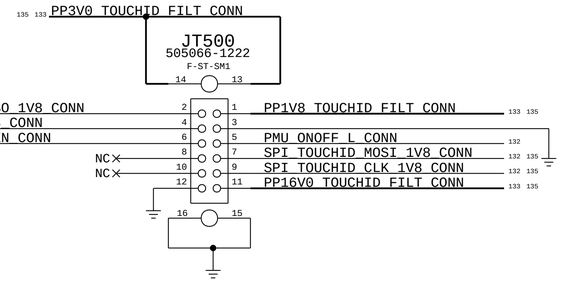


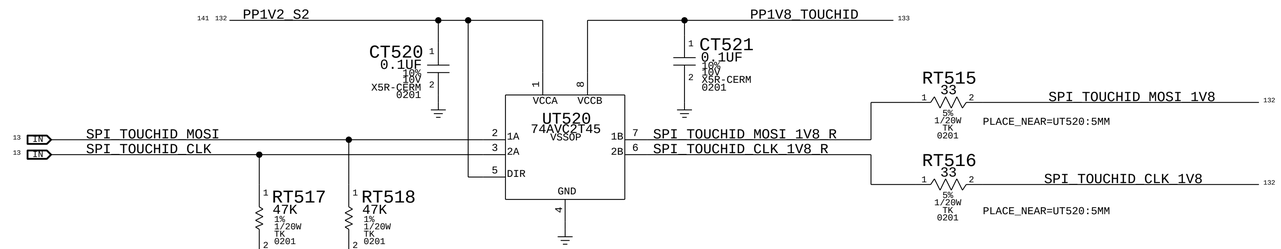


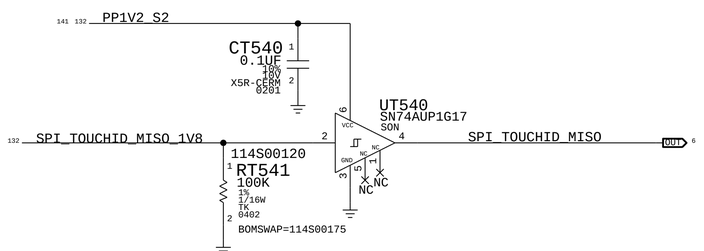












BOM_COST_GROUP=TOUCHID

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PAGE TITLE

TOUCHID CONN

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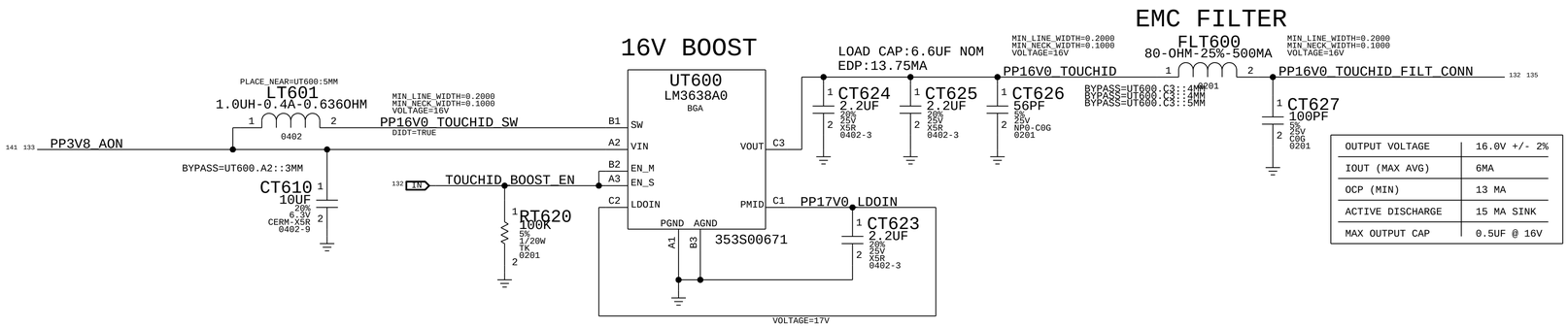
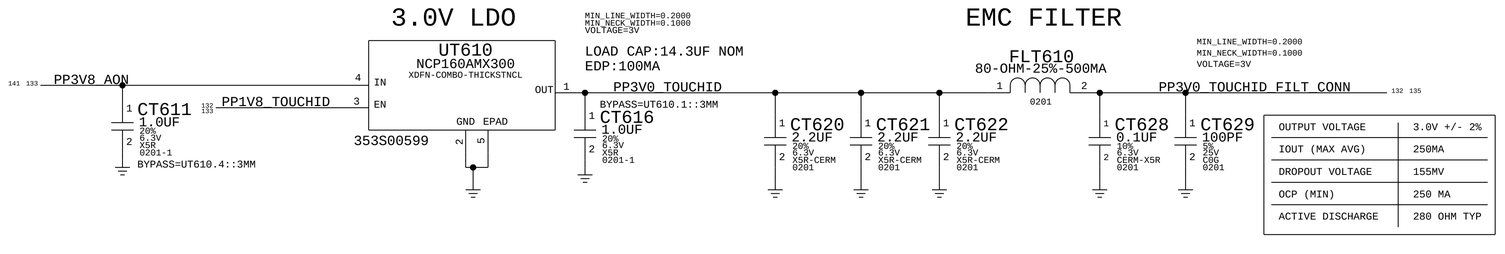
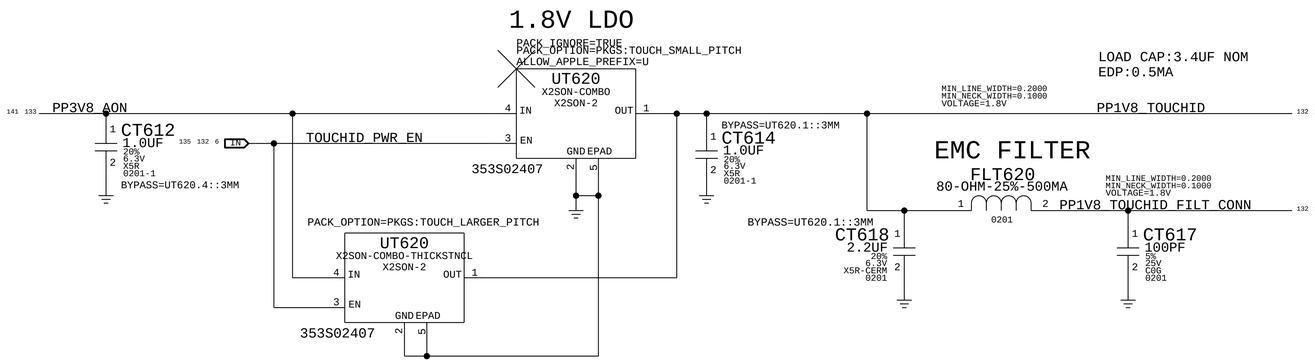
TOUCHID POWER SEQUENCING REQUIREMENTS
POWER ON: 1V8 -> 3V3 -> 16V0



OUTPUT VOLTAGE	16.0V +/- 2%
IOUT (MAX AVG)	6MA
OCP (MIN)	13 MA
ACTIVE DISCHARGE	15 MA SINK
MAX OUTPUT CAP	0.5UF @ 16V

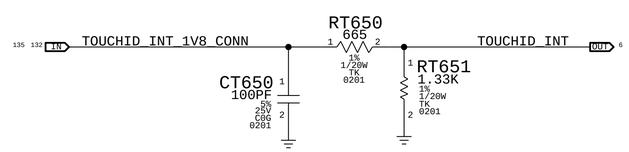


OUTPUT VOLTAGE	3.0V +/- 2%
IOUT (MAX AVG)	250MA
DROPOUT VOLTAGE	155MV
OCP (MIN)	250 MA
ACTIVE DISCHARGE	280 OHM TYP



OUTPUT VOLTAGE	1.825 V +/- 2%
IOUT (MAX AVG)	250 MA
DROPOUT VOLTAGE	75MV TYP @ 100MA
OCP (MIN)	250 MA
ACTIVE DISCHARGE	280 OHM TYP
MIN OUTPUT CAP	1.0 UF

UT620 CHANGED FROM 353S00754 TO 353S02407 FOR 1.2V EN SIGNAL SUPPORT.
N.B.: TOUCHID_PWR_EN REQUIRES 47K PULL-UP TO PP1V25_S2 AT THE SOC



BOM_COST_GROUP=TOUCHID

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Test Point Types Guide

PP are for EE debug (0.3mm)
TPs for general fixtures (0.4mm)
FCT test points use FUNC_TEST=TRUE, all go on TOP (0.4mm)
ICT test points placed by PCB designer not published in netlist, or use FCT (0.4mm)

NAND0 TPs

107 106 105 104 103	IN	NAND0_LPB_L	TOP	TPU603 TP-P4
109 108 107 106 105 104 103 8 111 110 109 108	IN	NAND_BFH	TOP	TPU604 TP-P4
106 105 104 103	IN	NAND0_BOOT2	TOP	TPU605 TP-P4
103	IN	NAND0_S5E0_SWD_UID0	TOP	TPU606 TP-P4
104	IN	NAND0_S5E1_SWD_UID0	TOP	TPU607 TP-P4
105	IN	NAND0_S5E2_SWD_UID0	TOP	TPU608 TP-P4
106	IN	NAND0_S5E3_SWD_UID0	TOP	TPU609 TP-P4
103	IN	NAND0_S5E0_SWD_UID1	TOP	TPU610 TP-P4
104	IN	NAND0_S5E1_SWD_UID1	TOP	TPU611 TP-P4
105	IN	NAND0_S5E2_SWD_UID1	TOP	TPU612 TP-P4
106	IN	NAND0_S5E3_SWD_UID1	TOP	TPU613 TP-P4
107 106 105 104 103	IN	NAND0_PFN_L	TOP	TPU614 TP-P4
106 105 104 103 8	IN	NAND0_PCIE_RESET_L	TOP	TPU615 TP-P4
11	IN	SWD_NAND0_SWDIO	TOP	TPU616 TP-P4
11	IN	SWD_NAND0_SWCLK	TOP	TPU617 TP-P4
106 105 104 103	IN	NAND0_WP_L	TOP	TPU618 TP-P4
13 8	IN	NAND0_CLKREQ0_L	TOP	TPU619 TP-P4
13 8	IN	NAND0_CLKREQ1_L	TOP	TPU620 TP-P4
13 8	IN	NAND0_CLKREQ2_L	TOP	TPU621 TP-P4
13 8	IN	NAND0_CLKREQ3_L	TOP	TPU622 TP-P4
103	IN	NAND0_S5E0_PCIE_RESREF	TOP	TPU623 TP-P4
104	IN	NAND0_S5E1_PCIE_RESREF	TOP	TPU624 TP-P4
105	IN	NAND0_S5E2_PCIE_RESREF	TOP	TPU625 TP-P4
106	IN	NAND0_S5E3_PCIE_RESREF	TOP	TPU626 TP-P4
148 107	IN	NAND0_RESET_L	TOP	TPU627 TP-P4
103	IN	NAND0_S5E0_ZQ_0	TOP	TPU628 TP-P4
103	IN	NAND0_S5E0_ZQ_1	TOP	TPU629 TP-P4
104	IN	NAND0_S5E1_ZQ_1	TOP	TPU630 TP-P4
104	IN	NAND0_S5E1_ZQ_0	TOP	TPU631 TP-P4
105	IN	NAND0_S5E2_ZQ_0	TOP	TPU632 TP-P4
105	IN	NAND0_S5E2_ZQ_1	TOP	TPU633 TP-P4
106	IN	NAND0_S5E3_ZQ_1	TOP	TPU634 TP-P4
106	IN	NAND0_S5E3_ZQ_0	TOP	TPU635 TP-P4
103	IN	TP_NAND0_S5E0_JTAG_TDI	TOP	TPU668 TP-P4
106	IN	TP_NAND0_S5E3_JTAG_TDO	TOP	TPU669 TP-P4
106 105 104 103	IN	NAND0_JTAG_SEL	TOP	TPU670 TP-P4
106 105 104 103	IN	NAND0_JTAG_TRST_L	TOP	TPU671 TP-P4
136 103	IN	TP_NAND0_S5E0_ANI1_VREF	TOP	TPU672 TP-P4
136 103	IN	TP_NAND0_S5E0_ANI0_VREF	TOP	TPU673 TP-P4
136 104	IN	TP_NAND0_S5E1_ANI1_VREF	TOP	TPU674 TP-P4
136 104	IN	TP_NAND0_S5E1_ANI0_VREF	TOP	TPU675 TP-P4
136 105	IN	TP_NAND0_S5E2_ANI1_VREF	TOP	TPU676 TP-P4
136 105	IN	TP_NAND0_S5E2_ANI0_VREF	TOP	TPU677 TP-P4
136 106	IN	TP_NAND0_S5E3_ANI1_VREF	TOP	TPU678 TP-P4
136 106	IN	TP_NAND0_S5E3_ANI0_VREF	TOP	TPU679 TP-P4
107	IN	TP_NAND0_OCARINA_VEN2	TOP	TPU600 TP-P4

NAND1 TPs

112 111 110 109 108	IN	NAND1_LPB_L	TOP	TPU636 TP-P4
111 110 109 108	IN	NAND1_BOOT2	TOP	TPU637 TP-P4
108	IN	NAND1_S5E0_SWD_UID0	TOP	TPU638 TP-P4
109	IN	NAND1_S5E1_SWD_UID0	TOP	TPU639 TP-P4
110	IN	NAND1_S5E2_SWD_UID0	TOP	TPU640 TP-P4
111	IN	NAND1_S5E3_SWD_UID0	TOP	TPU641 TP-P4
108	IN	NAND1_S5E0_SWD_UID1	TOP	TPU642 TP-P4
109	IN	NAND1_S5E1_SWD_UID1	TOP	TPU643 TP-P4
110	IN	NAND1_S5E2_SWD_UID1	TOP	TPU644 TP-P4
111	IN	NAND1_S5E3_SWD_UID1	TOP	TPU645 TP-P4
112 111 110 109 108	IN	NAND1_PFN_L	TOP	TPU646 TP-P4
111 110 109 108 8	IN	NAND1_PCIE_RESET_L	TOP	TPU647 TP-P4
11	IN	SWD_NAND1_SWDIO	TOP	TPU648 TP-P4
11	IN	SWD_NAND1_SWCLK	TOP	TPU649 TP-P4
111 110 109 108	IN	NAND1_WP_L	TOP	TPU650 TP-P4
13 8	IN	NAND1_CLKREQ0_L	TOP	TPU651 TP-P4
13 8	IN	NAND1_CLKREQ1_L	TOP	TPU652 TP-P4
13 8	IN	NAND1_CLKREQ2_L	TOP	TPU653 TP-P4
13 8	IN	NAND1_CLKREQ3_L	TOP	TPU654 TP-P4
108	IN	NAND1_S5E0_PCIE_RESREF	TOP	TPU655 TP-P4
109	IN	NAND1_S5E1_PCIE_RESREF	TOP	TPU656 TP-P4
110	IN	NAND1_S5E2_PCIE_RESREF	TOP	TPU657 TP-P4
111	IN	NAND1_S5E3_PCIE_RESREF	TOP	TPU658 TP-P4
148 112	IN	NAND1_RESET_L	TOP	TPU659 TP-P4
108	IN	NAND1_S5E0_ZQ_0	TOP	TPU660 TP-P4
108	IN	NAND1_S5E0_ZQ_1	TOP	TPU661 TP-P4
109	IN	NAND1_S5E1_ZQ_1	TOP	TPU662 TP-P4
109	IN	NAND1_S5E1_ZQ_0	TOP	TPU663 TP-P4
110	IN	NAND1_S5E2_ZQ_0	TOP	TPU664 TP-P4
110	IN	NAND1_S5E2_ZQ_1	TOP	TPU665 TP-P4
111	IN	NAND1_S5E3_ZQ_1	TOP	TPU666 TP-P4
111	IN	NAND1_S5E3_ZQ_0	TOP	TPU667 TP-P4
110 109	IN	NAND1_S5E1_JTAG_TDO	TOP	TPU680 TP-P4
111 110	IN	NAND1_S5E2_JTAG_TDO	TOP	TPU681 TP-P4
108	IN	TP_NAND1_S5E0_JTAG_TDI	TOP	TPU682 TP-P4
111	IN	TP_NAND1_S5E3_JTAG_TDO	TOP	TPU683 TP-P4
111 110 109 108	IN	NAND1_JTAG_SEL	TOP	TPU684 TP-P4
111 110 109 108	IN	NAND1_JTAG_TRST_L	TOP	TPU685 TP-P4
136 108	IN	TP_NAND1_S5E0_ANI1_VREF	TOP	TPU686 TP-P4
136 108	IN	TP_NAND1_S5E0_ANI0_VREF	TOP	TPU687 TP-P4
136 109	IN	TP_NAND1_S5E1_ANI1_VREF	TOP	TPU688 TP-P4
136 109	IN	TP_NAND1_S5E1_ANI0_VREF	TOP	TPU689 TP-P4
136 110	IN	TP_NAND1_S5E2_ANI1_VREF	TOP	TPU690 TP-P4
136 110	IN	TP_NAND1_S5E2_ANI0_VREF	TOP	TPU691 TP-P4
136 111	IN	TP_NAND1_S5E3_ANI1_VREF	TOP	TPU692 TP-P4
136 111	IN	TP_NAND1_S5E3_ANI0_VREF	TOP	TPU693 TP-P4
112	IN	TP_NAND1_OCARINA_VEN2	TOP	TPU601 TP-P4

SoC Misc Debug TPs

135 74 6	IN	UART_DEBUGPRT_D2R	BOTTOM	TPU6614 TP-P4
135 74 6	IN	UART_DEBUGPRT_R2D	BOTTOM	TPU6615 TP-P4
135 44 12 10	IN	PMU_RESET_L	BOTTOM	TPU6616 TP-P4
138 135 74 44 5	IN	SOC_FORCE_DFU	BOTTOM	TPU6617 TP-P4
5	IN	SOC_REQUEST_DFU1_L	BOTTOM	TPU6618 TP-P4
5	IN	SOC_REQUEST_DFU2_L	BOTTOM	TPU6619 TP-P4
137 135 73 44 10 5	IN	PMU_ACTIVE_READY	BOTTOM	TPU6621 TP-P4
135 5	IN	SOC_HOLD_RESET	BOTTOM	TPU6622 TP-P4
5	IN	SOC_KIS_DFU_SELECT	TOP	TPU6623 TP-P4
5	IN	SOC_DBG_PROBE_VALID	BOTTOM	TPU6624 TP-P4
5	IN	SOC_STOP_CLK_L	BOTTOM	TPU6625 TP-P4
45 10	IN	PMU_CLK32K_SOC	BOTTOM	TPU6600 TP-P4
135 14 10	IN	SMC_FIXTURE_MODE_L	TOP	TPU6603 TP-P4
TPT_SOC_DOCK_ATTENTION MAKE_BASE=TRUE		TPT_SOC_DOCK_ATTENTION	TOP	TPU6601 TP-P4
TPT_TST_CLKOUT MAKE_BASE=TRUE		TPT_TST_CLKOUT	TRUE	PPU1 P3MM

SoC JTAG TPs

10	IN	SOC_JTAG_SEL		TPU6604 TP-P4
135 74 11	IN	SWD_SOC_SWCLK PLACE_NEAR=UF400:20mm		TPU6605 TP-P4
135 74 11	IN	SWD_SOC_SWDIO PLACE_NEAR=UF400:20mm		TPU6608 TP-P4
150 10		SOC_JTAG_TDI		TPU6606 TP-P4
150 10		SOC_JTAG_TDO		TPU6607 TP-P4
TPT_JTAG_SOC_TRST_L MAKE_BASE=TRUE	10	TPT_JTAG_SOC_TRST_L		TPU6609 TP-P4

Fan TPs

67	IN	TP_I2C_FAN0_SCL	BOTTOM	TPU6200 TP-P4
67	IN	TP_I2C_FAN0_SDA	BOTTOM	TPU6201 TP-P4
67	IN	TP_I2C_FAN1_SCL	BOTTOM	TPU6202 TP-P4
67	IN	TP_I2C_FAN1_SDA	BOTTOM	TPU203 TP-P4

H116	VSNS_PVDDSRAM_SENSE	TRUE	11 16
H116	VSNS_PVDDAMPH0_SENSE	TRUE	11 19
H116	VSNS_PVDDDCS_SENSE	TRUE	11 16
H118	ATCRTMR_ACTIVE_READY_3V3	TRUE	73 78 89

33	IN	GND		TPV001 TP-P4
33	IN	GND		TPV002 TP-P4
45 29	IN	CHGR_AUX_OK	TOP	TPU6664 TP-P4
143 136 135	IN	PP1V8_S1_CLVR_VDDH	TOP	TPU6665 TP-P4
128	IN	KBD_RIGHT_SHIFT_L PLACE_NEAR=UY103.9:20MM	TOP	TPU6666 TP-P4
128	IN	KBD_LEFT_OPTION_L PLACE_NEAR=UY103.8:20MM	TOP	TPU6667 TP-P4
128	IN	KBD_CONTROL_L PLACE_NEAR=UY103.7:20MM	TOP	TPU6668 TP-P4

Audio Team TPs

122	IN	PP3V8_CODEC_VP		TPU6626 TP-P4
122	IN	PP1V8_CODEC_VCP		TPU6627 TP-P4
122 10	IN	CODEC_RESET_L		TPU6628 TP-P4
122 6	IN	CODEC_INT_L		TPU6629 TP-P4
I2C0		CODEC_WAKE_L TRUE		44 122
122 13	IN	TDM_CODEC_FSYNC PLACE_NEAR=UR500.B2:20MM		TPU6630 TP-P4
122 13	IN	TDM_CODEC_R2D PLACE_NEAR=UR500.B3:20MM		TPU6631 TP-P4
122 6	IN	TDM_CODEC_D2R PLACE_NEAR=U0600.BG52:20MM		TPU6632 TP-P4
122 13	IN	TDM_CODEC_BCLK PLACE_NEAR=UR500.A3:20MM		TPU6633 TP-P4
122 56	IN	I2C_CODEC_SDA		TPU6634 TP-P4
122 56	IN	I2C_CODEC_SCL		TPU6635 TP-P4
124 123 6	IN	SPKRAMP_RESET_L		TPU6636 TP-P4
124 123 6	IN	SPKRAMP_INT_L		TPU6637 TP-P4
123 13	IN	TDM_SPKRAMP_L_BCLK PLACE_NEAR=UR600.E1:20MM		TPU6638 TP-P4
123 13	IN	TDM_SPKRAMP_L_FSYNC PLACE_NEAR=UR600.D2:20MM		TPU6639 TP-P4
123 13	IN	TDM_SPKRAMP_L_R2D PLACE_NEAR=UR600.E2:20MM		TPU6640 TP-P4
123 13	IN	TDM_SPKRAMP_L_D2R PLACE_NEAR=U0600.BG55:20MM		TPU6641 TP-P4
123	IN	SPKRAMP_ABC_ICC		TPU6642 TP-P4
123	IN	SPKRAMP_DEF_ICC		TPU6672 TP-P4
5 TP_ANALOGMUX_OUT0	IN	I2C_SPKRAMP_SCL		TPU6643 TP-P4
5 TP_ANALOGMUX_OUT1	IN	I2C_SPKRAMP_SDA		TPU6644 TP-P4
123	IN	TP_SPKRAMP_A_LV_EN		TPU6645 TP-P4
123	IN	TP_SPKRAMP_B_LV_EN		TPU6646 TP-P4
123	IN	TP_SPKRAMP_C_LV_EN		TPU6647 TP-P4
124 13	IN	TDM_SPKRAMP_R_BCLK PLACE_NEAR=UR700.E1:20MM		TPU6648 TP-P4
124 13	IN	TDM_SPKRAMP_R_FSYNC PLACE_NEAR=UR700.D2:20MM		TPU6649 TP-P4
124 13	IN	TDM_SPKRAMP_R_R2D PLACE_NEAR=UR700.E2:20MM		TPU6650 TP-P4
124 13	IN	TDM_SPKRAMP_R_D2R PLACE_NEAR=U0600.BG50:20MM		TPU6651 TP-P4
124 56	IN	I2C_SPKRAMP_R_SCL		TPU6652 TP-P4
124 56	IN	I2C_SPKRAMP_R_SDA		TPU6653 TP-P4
124	IN	TP_SPKRAMP_D_LV_EN		TPU6654 TP-P4
124	IN	TP_SPKRAMP_E_LV_EN		TPU6655 TP-P4
124	IN	TP_SPKRAMP_F_LV_EN		TPU6656 TP-P4
136 126 10	IN	PDM_DMIC_DATA1 PLACE_NEAR=U0600.BB12:20MM	TOP	TPU6657 TP-P4
136 126 10	IN	PDM_DMIC_DATA4 PLACE_NEAR=U0600.AG13:20MM	TOP	TPU6658 TP-P4
136 126 13	IN	PDM_DMIC_CLK7 PLACE_NEAR=UR960.3:20MM	TOP	TPU6659 TP-P4
136 126 13	IN	PDM_DMIC_CLK8 PLACE_NEAR=UR950.3:20MM	TOP	TPU6660 TP-P4
T818		FUNC_TEST		
136 31 30	IN	USBC5_CC1	TOP	TPU6663 TP-P4
30	IN	USBC5_CC1_PIN	TOP	TPU6669 TP-P4

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PLACE_NEAR=RH000.2:5MM
PLACE_NEAR=RH001.2:5MM

DFU, Debug

		FUNC_TEST	
J3	USB2_ATC0_LS_P	TPU7A2 TP-P4	
J4	USB2_ATC0_LS_N	TPU7A3 TP-P4	
J1	USBC0_USB_TOP_P	TRUE	68 69 75
J2	USBC0_USB_TOP_N	TRUE	68 69 75
J5	USB_DBG_LS_N	TRUE	74 150
J6	USB_DBG_LS_P	TRUE	74 150
J1N	SOC_DOCK_CONNECT	TPU6671 TP-P4	
J7	SOC_FORCE_DFU	TRUE	5 44 74 134 138
J8	SOC_DFU_STATUS	TRUE	5 74 137
J9	SOC_FORCE_DFU_DBG	TRUE	138
J10	UART_DEBUGPRT_R2D	TRUE	6 74 134
J11	UART_DEBUGPRT_D2R	TRUE	6 74 134
J12	SWD_SOC_SWCLK	TRUE	11 74 134
J13	SWD_SOC_SWDIO	TRUE	11 74 134
J14	UART_SMC_DEBUGPRT_R2D	TRUE	10 74
J15	UART_SMC_DEBUGPRT_D2R	TRUE	10 74
J16	SMC_FIXTURE_MODE_L	TRUE	10 14 134
J17	I2C_SMC_UPC_SDA	TRUE	10 32 57 136
J18	I2C_SMC_UPC_SCL	TRUE	10 32 57 136
J19	PMU_SYS_ALIVE	TRUE	44 87 89 93 107 112 117
J638	P5VS2_PWR_EN	TRUE	29 44 45
J20	PMU_ACTIVE_READY	TRUE	5 10 44 73 134
J21	PMU_ONOFF_L	TRUE	44 45 132 138
J22	PMU_RSLOC_RST_L	TRUE	44 45 128 138
J23	SOC_SOCHOT_L	TRUE	5 44
J24	PMU_RESET_L	TRUE	10 12 44 134
J25	PMU_SHDN	TRUE	44 45 138
J643	RTMRMUX_OE_L	TRUE	140
J640	PMU_SCRASH_L	TRUE	40 44
J4N	PMU_WAKE2MS	TPU6670 TP-P4	
J644	USB0_3V3_LDO_EN_VITC	TRUE	150

Battery

		FUNC_TEST
J26	PPVBAT_AON	TPU700 TP-P4
		TPU701 TP-P4
		TPU702 TP-P4
		TPU703 TP-P4
		TPU704 TP-P4
		TPU705 TP-P4
		TPU706 TP-P4
		TPU707 TP-P4
		TPU708 TP-P4
		TPU709 TP-P4
		TPU710 TP-P4
		TPU711 TP-P4
		TPU712 TP-P4
		TPU713 TP-P4
		TPU714 TP-P4
		TPU715 TP-P4
		TPU716 TP-P4
J27	SMBUS_BATT_SDA	TRUE 27 57 136
J28	SMBUS_BATT_SCL	TRUE 27 57 136
J29	SYS_DETECT_L	TRUE 27
J30	SYS_DETECT	TRUE 27 138
J605	I2C_SMC_PWR_SCL	TRUE 10 57
J606	I2C_SMC_PWR_SDA	TRUE 10 57
	GND	TPU717 TP-P4

Charger

		FUNC_TEST
J32	PPDCIN_AON	TPU718 TP-P4
		TPU719 TP-P4
		TPU720 TP-P4
		TPU721 TP-P4
		TPU722 TP-P4
		TPU723 TP-P4
		TPU724 TP-P4
		TPU725 TP-P4
		TPU726 TP-P4
		TPU727 TP-P4
		TPU728 TP-P4
J33	PPDCIN_AON_CHGR	TRUE 32 59
J34	PPHV_INT5_AONSW	TRUE 32 136
J35	PPVBUS_USBC5	TPU729 TP-P4
		TPU730 TP-P4
		TPU731 TP-P4
		TPU732 TP-P4
		TPU733 TP-P4
		TPU734 TP-P4
		TPU735 TP-P4
		TPU736 TP-P4
		TPU737 TP-P4
		TPU738 TP-P4
		TPU739 TP-P4
J570	PP5V_CHGR	TRUE 29
J616	CHGR_INT_L	TRUE 10 29 148
J617	CHGR_RST_IN	TRUE 27 28 45
J618	CHGR_THMSNS	TRUE 45 65
J592	PP5V_CHGR_SW	TPU7A0 TP-P4
	GND	TPU740 TP-P4
		TPU741 TP-P4
		TPU742 TP-P4
		TPU743 TP-P4
		TPU744 TP-P4
		TPU745 TP-P4
		TPU746 TP-P4
		TPU747 TP-P4
		TPU748 TP-P4
		TPU749 TP-P4
		TPU750 TP-P4

Power rails

		FUNC_TEST
J52	PPBUS_AON	TPU751 TP-P4
		TPU752 TP-P4
		TPU753 TP-P4
		TPU754 TP-P4
		TPU755 TP-P4
		TPU756 TP-P4
		TPU757 TP-P4
		TPU758 TP-P4
		TPU759 TP-P4
		TPU760 TP-P4
		TPU761 TP-P4
J53	PP3V8_AON	TRUE 141
J64	PPVDD_DISP_AWAKESW	TRUE 144
J55	PPVDD_SRAM_S1	TRUE 139 144
J57	PP1V8_S2SW	TRUE 137 144
J58	PPVDDQ0_S1	TRUE 145
J59	PPVDDQ1_S1	TRUE 144
J60	PPVDD_CIO_S2SW	TRUE 139 145
J61	PPVDD_GPU_BMPR_S1	TRUE 144
J62	PPVDD_AMPH1_S2SW	TRUE 144
J63	PPVDD_AMPH0_S2SW	TRUE 145
J64	PPVDD_ECPU_AWAKESW	TRUE 145
J65	PP1V8_AWAKE	TRUE 145
J66	PPVDD_AVEMSR_AWAKESW	TRUE 144
J67	PPVDD_FIXED_S1	TRUE 144
J68	PPVDD_SOC_S1	TRUE 145
J69	PPVDD_DCS_S1	TRUE 145
J70	PP1V8_S2	TRUE 135 145
J71	PP1V8_S2	TRUE 135 145
J72	PP1V2_S2	TRUE 56 139 144
J654	PP3V3_HVLDO_OUT	TRUE 29 136
J74	PP1V8_AON	TRUE 144
J75	PP1V2_AWAKE	TRUE 144
J76	PPVDD2H0_S2SW	TRUE 145
J77	PPVDD2H1_S2SW	TRUE 144
J78	PP1V8_S2SW_CLVR_VDDIO	TRUE 144
J79	PP1V8_S2SW_CLVR_VDDC1	TRUE 144
J80	PP0V8_S2_CLVR_VDDDIG	TRUE 136 144
J81	PP1V2_AON	TRUE 144
J82	PP1V5_AON_VCORE_MPMU	TRUE 42
J83	PP0V9_NAND0	TRUE 107
J84	PP1V2_NAND0	TRUE 107
J85	PP2V5_NAND0	TRUE 107
J86	PP0V9_NAND1	TRUE 112
J87	PP1V2_NAND1	TRUE 112
J88	PP2V5_NAND1	TRUE 112
J652	PP1V2_ATCRTMR01_VDDIO	TRUE 141
J653	PP1V2_ATCRTMR2_VDDIO	TRUE 141
J92	PP5V_S2SW_USBC01	TRUE 136 142
J93	PP5V_S2SW_USBC23	TRUE 136 142
J94	PPMDB_AWAKESW_TCON	TRUE 141
J95	PP3V3_AON	TRUE 137 141
J96	PP3V3_S2	TRUE 137 144
J97	PP5V_S2_MAIN	TPU762 TP-P4
		TPU763 TP-P4
J98	PP3V3_UPC0_LDO	TRUE 73 74 75
J100	PPVBAT_AON_CHGR_R	TRUE 28
J101	PPVBAT_AON_CHGR_REG	TPU764 TP-P4
		TPU765 TP-P4
		TPU766 TP-P4
J655	USBC5_UV_SENSE	TRUE 35
J656	PP1V8_S1_CLVR_VDDH	TRUE 134 136 143
J660	PP0V95_AWAKESW_DP2HDMI	TRUE 92 94
J670	PP1V85_S2_KBD	TRUE 128 129

Fan

		FUNC_TEST
J102	PPBUS_AON_FAN0_FILT	TPU767 TP-P4
		TPU768 TP-P4
		TPU769 TP-P4
J675	PP3V3_S2_FAN_LS	TRUE 67
J103	SMC_FAN_0_PWM_3V3	TRUE 67
J104	FAN_0_TACH	TRUE 67
J105	PPBUS_AON_FAN1_FILT	TPU770 TP-P4
		TPU771 TP-P4
		TPU772 TP-P4
J106	SMC_FAN_1_PWM_3V3	TRUE 67
J107	FAN_1_TACH	TRUE 67
J580	FAN_PWR_EN	TRUE 40 67
	GND	TPU773 TP-P4
	GND	TPU774 TP-P4
	GND	TPU775 TP-P4
	GND	TPU776 TP-P4

USB-C

		FUNC_TEST
J112	PPVBUS_USBC0	TPU778 TP-P4
		TPU779 TP-P4
		TPU780 TP-P4
		TPU781 TP-P4
		TPU782 TP-P4
		TPU783 TP-P4
J113	USBC0_SBU1	TRUE 68 69 75
J114	USBC0_SBU2	TRUE 68 69 75
J115	USBC0_CC1	TRUE 74 75
J116	USBC0_CC2	TRUE 74 75
J117	TP_USBC0_PP20V	TRUE 68 69
	GND	TPU784 TP-P4
J119	PPVBUS_USBC1	TPU785 TP-P4
		TPU786 TP-P4
		TPU787 TP-P4
		TPU788 TP-P4
		TPU789 TP-P4
		TPU790 TP-P4
J120	USBC1_CC1	TRUE 74 76
J121	USBC1_CC2	TRUE 74 76
J122	USBC1_SBU1	TRUE 68 69 76
J123	USBC1_SBU2	TRUE 68 69 76
J124	TP_USBC1_PP20V	TRUE 68 69
	GND	TPU791 TP-P4
J126	PPVBUS_USBC2	TPU792 TP-P4
		TPU793 TP-P4
		TPU794 TP-P4
		TPU795 TP-P4
		TPU796 TP-P4
		TPU797 TP-P4
J127	USBC2_CC1	TRUE 83 84
J128	USBC2_CC2	TRUE 83 84
J131	TP_USBC2_PP20V	TRUE 69 70
	GND	TPU798 TP-P4

Camera

		FUNC_TEST
J141	PP5V_S2_CAMERA	TRUE 142
J142	I2C_CAM_1V8_SDA	TRUE 58 115
J143	I2C_ALS_1V8_SDA	TRUE 58 115
J144	I2C_CAM_1V8_SCL	TRUE 58 115
J145	I2C_ALS_1V8_SCL	TRUE 58 115
J147	ALS_INT_L	TRUE 10 115
J577	FTCAM_ENABLE_1V8_OUT	TRUE 114 148
J600	LPDP_FTCAM_DATA_P<0>	TRUE 7 114 115
J601	LPDP_FTCAM_DATA_N<0>	TRUE 7 114 115
	GND	TPU799 TP-P4

Display

		FUNC_TEST
J149	PP3V8_AWAKESW_TCON	TRUE 142
J150	I2C_SMC_SNS0_SCL_1V8	TRUE 58
J151	I2C_SMC_SNS0_SDA_1V8	TRUE 58
J152	UART_TCON_D2R_1V8	TRUE 116
J153	EDP_PANEL_1V8_EN	TRUE 116 117
J154	LPDP_INT_HPD	TRUE 7 116 146 148
J155	SPI_TCON_CS_L	TRUE 13 116
J156	SPI_TCON_MISO	TRUE 6 116
J157	SPI_TCON_MOSI	TRUE 13 116
J158	SPI_TCON_CLK	TRUE 13 116
	GND	TPU800 TP-P4

Backlight

		FUNC_TEST
J160	I2C_TCON_BKLT_SCL_1V8	TRUE 56
J161	I2C_TCON_BKLT_SDA_1V8	TRUE 56
J162	BL_PMIC_PWR_EN	TRUE 45 119
J163	PPVOUT_LUXE	TRUE 118 119 135
		TPU801 TP-P4
		TPU802 TP-P4
		TPU803 TP-P4
		TPU804 TP-P4
		TPU805 TP-P4
		TPU806 TP-P4
J164	PP1V2_AWAKESW_BLC	TRUE 141
J165	PPBCON_AWAKESW_BKLTCONN	TRUE 119 142
J166	DISP_BKLT_LSYNC	TRUE 7 119
J167	BKLT_BOOST_THROTTLE_CONN_L	TRUE 119
J168	DISP_2DBL_FSYNC	TRUE 7 119

SPI

		FUNC_TEST
J169	SPI_DISP_BKLT_CS_L	TRUE 7 119
J170	SPI_DISP_BKLT_MISO	TRUE 7 119 136
J171	SPI_DISP_BKLT_MOSI	TRUE 13 119
J172	SPI_DISP_BKLT_CLK	TRUE 13 119
	GND	TP807 TP-P4

AMR

		FUNC_TEST
J174	MGL_1V8	TRUE 120 121
J175	AMR1_OR_ND_1V8	TRUE 120 148
J176	SPI_LAS_CS_1V8_L	TRUE 14 120
J177	SPI_AOP_LAS_SCLK_1V8	TRUE 14 120
J178	SPI_AOP_LAS_MISO_1V8_R	TRUE 120
J179	SPI_AOP_LAS_MOSI_1V8	TRUE 14 120
	GND	TPU808 TP-P4

Audio Jack

		FUNC_TEST
J181	AUD_CONN_HP_LEFT	TRUE 126
J182	AUD_CONN_SLEEVE	TRUE 126
J183	AUD_CONN_HP_RIGHT	TRUE 126
J184	AUD_CONN_RING2	TRUE 126
J185	AUD_CONN_TIP_SENSE	TRUE 126
J186	AUD_CONN_HP_SENSE_L	TRUE 126
J187	AUD_CONN_RING2_XW	TRUE 126
J188	AUD_CONN_RING_SENSE	TRUE 126
J189	AUD_CONN_HP_SENSE_R	TRUE 126
J190	AUD_CONN_SLEEVE_XW	TRUE 126
	GND	TPU809 TP-P4

Touch ID

		FUNC_TEST
J191	PP1V8_TOUCHID_FILT_CONN	TRUE 132 133
J192	SPI_TOUCHID_MISO_1V8_CONN	TRUE 132
J193	SPI_TOUCHID_MOSI_1V8_CONN	TRUE 132
J194	TOUCHID_INT_1V8_CONN	TRUE 132 133
J195	SPI_TOUCHID_CLK_1V8_CONN	TRUE 132
J196	TOUCHID_BOOST_EN_CONN	TRUE 132
J197	PP16V0_TOUCHID_FILT_CONN	TRUE 132 133
J607	TOUCHID_PWR_EN	TRUE 6 132 133
J198	PP3V0_TOUCHID_FILT_CONN	TRUE 132 133
		TPU810 TP-P4
		TPU811 TP-P4
		TPU812 TP-P4
	GND	TPU813 TP-P4

Audio speaker amp

		FUNC_TEST
J200	SPKRAMP_A_OUTP	TPU815 TP-P4
		TPU816 TP-P4
		TPU817 TP-P4
J207	SPKRAMP_A_OUTN	TPU818 TP-P4
		TPU819 TP-P4
		TPU820 TP-P4
J208	SPKRAMP_B_OUTP	TPU821 TP-P4
		TPU822 TP-P4
		TPU823 TP-P4
J209	SPKRAMP_B_OUTN	TPU824 TP-P4
		TPU825 TP-P4
		TPU826 TP-P4
J210	SPKRAMP_C_OUTP	TPU827 TP-P4
		TPU828 TP-P4
		TPU864 TP-P4
J211	SPKRAMP_C_OUTN	TPU829 TP-P4
		TPU830 TP-P4
		TPU831 TP-P4
J212	SPKR_ID0	TRUE 6 125
	GND	TPU832 TP-P4
	GND	TPU833 TP-P4
	GND	TPU834 TP-P4
	GND	TPU835 TP-P4
J217	SPKRAMP_D_OUTP	TPU836 TP-P4
		TPU837 TP-P4
		TPU838 TP-P4
J218	SPKRAMP_D_OUTN	TPU839 TP-P4
		TPU840 TP-P4
		TPU841 TP-P4
J219	SPKRAMP_E_OUTP	TPU842 TP-P4
		TPU843 TP-P4
		TPU844 TP-P4
J220	SPKRAMP_E_OUTN	TPU845 TP-P4
		TPU846 TP-P4
		TPU847 TP-P4

J221	SPKRAMP_F_OUTP	TPU848 TP-P4	124 125
		TPU849 TP-P4	
		TPU850 TP-P4	
J222	SPKRAMP_F_OUTN	TPU851 TP-P4	124 125
		TPU852 TP-P4	
		TPU853 TP-P4	
J223	SPKR_ID1	TRUE	6 125
	GND	TPU854 TP-P4	
	GND	TPU855 TP-P4	
	GND	TPU856 TP-P4	

Keyboard

		FUNC_TEST
J229	KBD_ID1	TRUE 128 129
J665	KBD_ID2	TRUE 128 129
J230	KBD_DRIVE_Y8	TRUE 128 129
J666	KBD_DRIVE_Y9	TRUE 128 129
J667	KBD_DRIVE_Y10	TRUE 128 129
J668	KBD_DRIVE_Y11	TRUE 128 129
J231	KBD_DRIVE_Y2	TRUE 128 129
J232	KBD_DRIVE_Y1	TRUE 128 129
J233	KBD_DRIVE_Y3	TRUE 128 129
J234	KBD_DRIVE_Y4	TRUE 128 129
J235	KBD_SENSE_X0	TRUE 128 129
J236	KBD_SENSE_X1	TRUE 128 129
J237	KBD_SENSE_X2	TRUE 128 129
J238	KBD_SENSE_X5	TRUE 128 129
J239	KBD_SENSE_X3	TRUE 128 129
J240	KBD_SENSE_X9	TRUE 128 129
J241	KBD_SENSE_X12	TRUE 128 129
J242	KBD_SENSE_X4	TRUE 128 129
J243	KBD_SENSE_X11	TRUE 128 129
J244	KBD_SENSE_X10	TRUE 128 129
J245	KBD_SENSE_X6	TRUE 128 129
J246	KBD_SENSE_X7	TRUE 128 129
J247	KBD_SENSE_X8	TRUE 128 129
J248	KBD_DRIVE_Y5	TRUE 128 129
J249	KBD_DRIVE_Y7	TRUE 128 129
J250	KBD_DRIVE_Y6	TRUE 128 129
J251	KBD_DRIVE_Y0	TRUE 128 129
J252	KBD_CAP_CATHODE	TRUE 128 129
J253	PP3V3_AON_KBD_CONN	TRUE 128 129
J254	KBD_RIGHT_SHIFT_KEY	TRUE 128 129
J255	KBD_LEFT_OPTION_KEY	TRUE 128 129
J256	KBD_CONTROL_KEY	TRUE 128 129
	GND	TPU857 TP-P4
J258	PPVOUT_KBDLED_CONN	TRUE 142
J259	KBDLED_CATHODE1	TRUE 127 129
J260	KBDLED_CATHODE2	TRUE 127 129
	GND	TPU858 TP-P4
	GND	TPU859 TP-P4

Trackpad

		FUNC_TEST
J262	IPD_LID_OPEN_1V8	TRUE 45 121 131
J263	I2C_TPAD_CONN_SCL	TRUE 130 131
J264	I2C_TPAD_CONN_SDA	TRUE 130 131
J265	IPD_WAKE_L	TRUE 45 130
J266	KBD_INT_L	TRUE 128 131
J268	I2C_KBD_SDA	TRUE 128 131 150
J269	I2C_KBD_SCL	TRUE 128 131 150
J270	SPI_TPAD_MOSI_CONN	TRUE 130 131
J271	SPI_TPAD_MCU_CS_CONN_L	TRUE 130 131
J272	SPI_TPAD_MISO_CONN	TRUE 130 131 139
J274	SPI_TPAD_CLK_CONN	TRUE 130 131
J275	PP5V_S2_TPAD_CONN	TRUE 131
J276	PP3V3_S2_IPD	TRUE 128 130 131
	GND	TPU860 TP-P4

Card Reader

		FUNC_TEST
J278	SDCONN_CMD_R_FL	TRUE 98
J280	PP3V3_GL_SDCONN	TRUE 97 98
J281	SDCONN_CLK_CONN_FL	TRUE 98
J282	SDCONN_D0_R_FL	TRUE 98
J283	SDCONN_D1_R_FL	TRUE 98
J284	SDCONN_D2_R_FL	TRUE 98
J285	SDCONN_D3_R_FL	TRUE 98
J286	SDCONN_SD0_UHS2_P	TRUE 97 98
J287	SDCONN_SD0_UHS2_N	TRUE 97 98
J288	SDCONN_SD1_UHS2_P	TRUE 97 98
J289	SDCONN_SD1_UHS2_N	TRUE 97 98
J290	PP1V8_GL_SDCONN	TRUE 97 98
J664	SDCONN_WP	TRUE 97 98
J663	SDCONN_DETECT	TRUE 98 99
J4N	PP1V2_GL_LOOP	TRUE 97
	GND	TPU861 TP-P4

Misc

		FUNC_TEST
J648	SOC_TESTMODE	TRUE 5
J647	SOC_HOLD_RESET	TPU7A1 TP-P4
J652	SE_PWR_EN	TRUE 26 40 45

LUXE

		FUNC_TEST
J294	I2C_LUXE_DEBUG_SCL	TRUE 56 118
J295	I2C_LUXE_DEBUG_SDA	TRUE 56 118
J296	LUXE_VPROG_TEST	TRUE 118
J297	PPBUS_AON_LUXE	TRUE 142
J298	PPLUXE_INPUT_R_V	TRUE 118 135 139
J299	PPVOUT_LUXE	TRUE 118 119 135
J300	PPLUXE_LX1	TRUE 118 139
J301	PPLUXE_LX2	TRUE 118 139
J302	LUXE_UG1	TRUE 118
J303	LUXE_LG1	TRUE 118
J304	LUXE_UG2	TRUE 118
J305	LUXE_LG2	TRUE 118
J306	BL_PWR_EN	TRUE 45 118
J307	SPMI_DISP_BKLT_CLK_R	TRUE 7 13
J308	SPMI_DISP_BKLT_DATA_R	TRUE 7 13
J309	BKLT_BOOST_THROTTLE_LUXE_L	TRUE 118
J310	PVOUT_LUXE_R	TRUE 118
J311	PPLUXE_INPUT_R_V	TRUE 118 135 139
J312	LUXE_AGND	TRUE 118
	GND	TPU862 TP-P4

KBD Backlight

		FUNC_TEST
J313	PP5V_KBDBKLT	TRUE 142
J314	KBDBKLT_SW2	TRUE 127 139
J315	KBDBKLT_FB2	TRUE 127
J316	KBDLED_KEYB1	TRUE 127
J317	KBDLED_KEYB2	TRUE 127
J318	KBD_BKLT_PWM_3V3	TRUE 127
J319	KBDBKLT_ISET_KEYB	TRUE 127 136
	GND	TPU863 TP-P4

CLVR

		FUNC_TEST
J563	CLVR_VDDH_UVWARN_L	TRUE 5 52 136
J562	TP_P1V8VDDH_DRMOS1_GL1	TRUE 49
J558	TP_P1V8VDDH_DRMOS2_GL1	TRUE 49
J559	TP_P1V8VDDH_DRMOS3_GL1	TRUE 50
J560	UPC5_SER_DBG	TRUE 31 32

NAND

		FUNC_TEST
J557	TP_NAND0_OCARINA_VCC_DET	TRUE 107
J554	TP_NAND0_S5E0_DROOP_L	TRUE 103
J555	TP_NAND0_S5E0_VPP	TRUE 103
J556	TP_NAND0_S5E1_DROOP_L	TRUE 104
J553	TP_NAND0_S5E1_VPP	TRUE 104
J552	TP_NAND0_S5E2_DROOP_L	TRUE 105
J551	TP_NAND0_S5E2_VPP	TRUE 105
J550	TP_NAND0_S5E3_DROOP_L	TRUE 106
J549	TP_NAND0_S5E3_VPP	TRUE 106
J548	TP_NAND1_OCARINA_VCC_DET	TRUE 112
J547	TP_NAND1_S5E0_DROOP_L	TRUE 108
J546	TP_NAND1_S5E0_VPP	TRUE 108
J545	TP_NAND1_S5E1_DROOP_L	TRUE 109
J544	TP_NAND1_S5E1_VPP	TRUE 109
J543	TP_NAND1_S5E2_DROOP_L	TRUE 110
J542	TP_NAND1_S5E2_VPP	TRUE 110
J541	TP_NAND1_S5E3_DROOP_L	TRUE 111
J540	TP_NAND1_S5E3_VPP	TRUE 111

HDMI

		FUNC_TEST
J530	HDMI_CEC_CONN	TRUE 90
J538	HDMI_DDC_5V_CONN_SCL	TRUE 90
J537	HDMI_DDC_5V_CONN_SDA	TRUE 90
J536	HDMI_HPD_IN_CONN	TRUE 90
J535	HDMI_RSVD	TRUE 90
J526	GND	TPU866 TP-P4
J678	DP2HDMI_PWR_EN_PMU	TRUE 45 93

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75 73 69 68 135	I151	PPVBUS_USBC0	BOTTOM 1 PP	PPU8C0	P3MM
73	I150	PPHV_INT0_AONSW	BOTTOM 1 PP	PPU8C1	P3MM
142 135	I149	PP5V_S2SW_USBC01	BOTTOM 1 PP	PPU8C2	P3MM
76 73 69 68 135	I148	PPVBUS_USBC1	BOTTOM 1 PP	PPU8C3	P3MM
73	I147	PPHV_INT1_AONSW	BOTTOM 1 PP	PPU8C4	P3MM
84 82 78 69 136	I146	PPVBUS_USBC2	BOTTOM 1 PP	PPU8C5	P3MM
82	I145	PPHV_INT2_AONSW	BOTTOM 1 PP	PPU8C6	P3MM
142 135	I144	PP5V_S2SW_USBC23	BOTTOM 1 PP	PPU8C7	P3MM
135 35 30 29	I143	PPVBUS_USBC5	BOTTOM 1 PP	PPU8C8	P3MM
135 32	I141	PPHV_INT5_AONSW	BOTTOM 1 PP	PPU8C9	P3MM
32 31 30	I142	PPHV_DIV	BOTTOM 1 PP	PPU8D0	P3MM
32	I180	PD_ACE5_VCONN	BOTTOM 1 PP	PPU8D1	P3MM

DCDC Debug 3mm PP

135 57 27	I229	SMBUS_BATT_SCL	BOTTOM 1 PP	PPU8D2	P3MM
135 57 27	I231	SMBUS_BATT_SDA	BOTTOM 1 PP	PPU8D3	P3MM
28	I230	CHGR_COMP	TOP 1 PP	PPU8D4	P3MM
28	I232	CHGR_BGATE	TOP 1 PP	PPU8D5	P3MM
49 48	I234	P1V8VDDH_DRMOS_PWM1	TOP 1 PP	PPU8D6	P3MM
49 48	I233	P1V8VDDH_DRMOS_PWM2	TOP 1 PP	PPU8D7	P3MM
50 48	I235	P1V8VDDH_DRMOS_PWM3	TOP 1 PP	PPU8D8	P3MM
	I237	SPI_DISP_BKLT_MISO	BOTTOM 1 PP	PPU8D9	P3MM

PLACE_NEAR=U0600.BG34:17MM

I245	I2C_UPC0_ATCRTMR0_SCL	TRUE	73 75 78 136
I246	I2C_UPC0_ATCRTMR0_SDA	TRUE	73 75 78 136

50 49 48	I239	P1V8VDDH_DRMOS_EN	TOP 1 PP	PPU8E2	P3MM
48	I238	P1V8VDDH_FAULT_L	TOP 1 PP	PPU8E3	P3MM
50 49 48	I240	P1V8VDDH_DRMOS_FAULT_L	TOP 1 PP	PPU8E4	P3MM
49	I241	P1V8VDDH_DRMOS_ISENSE1_P	TOP 1 PP	PPU8E5	P3MM
65 50 49 48	I242	P1V8VDDH_DRMOS_TSENSE	TOP 1 PP	PPU8E6	P3MM
49	I243	P1V8VDDH_DRMOS_ISENSE2_P	TOP 1 PP	PPU8E7	P3MM
50	I244	P1V8VDDH_DRMOS_ISENSE3_P	TOP 1 PP	PPU8E8	P3MM

MISC Power Rails

I270	P5VS2TPS_PGOOD	TRUE 29 36 55
I269	HDMI_HPD_AOP	TRUE 10 93
I273	PMU_VDDHI_UVWARN_L	TRUE 11 44
I272	PMU_VDDMAIN_UVWARN_L	TRUE 11 44
I275	DBL_CLICK_DET	TRUE 6 44
I202	TP_AON_SLEEP1_RESET_L	TRUE 10 136
I276	UPC_SMC_I2C_INT_L	TRUE 10 57
I271	P1V8VDDH_TLIMIT_THROTTLE_L	TRUE 5 48

I208	USBC0_CC1_CONN	TRUE 68 69 74
I209	USBC0_CC2_CONN	TRUE 68 69 74
I207	USBC1_CC1_CONN	TRUE 68 69 74
I206	USBC1_CC2_CONN	TRUE 68 69 74
I205	USBC2_CC1_CONN	TRUE 69 70 83
I204	USBC2_CC2_CONN	TRUE 69 70 83

USB-C (cont.)

I214	I2C_UPC_SCL	TRUE 6 32 56
I213	I2C_UPC_SDA	TRUE 6 32 56
I212	I2C_UPC5_SCL	TRUE 31 35
I211	I2C_UPC5_SDA	TRUE 31 35
I210	P5VUSBC01_EN	TRUE 79
I215	P5VUSBC23_EN	TRUE 87

I209	PMU_CRASH_L	TRUE 44 45
I266	CLVR_RESET_L	TRUE 44 51 52 53
I203	P3V8AON_PWR_EN	TRUE 27 28 33 35
I201	P5VS2TPS_PWR_EN	TRUE 45 55 94
I202	IPD_PWR_HOLD	TRUE 40 45

NAND (cont.)

I177	I2C_SMC_NAND_SCL	TRUE 10 57
I175	I2C_SMC_NAND_SDA	TRUE 10 57
I176	NAND0_OCARINA_VREF	TRUE 107
I174	NAND1_OCARINA_VREF	TRUE 112
I172	NAND1_S5E0_JTAG_TDO	TRUE 108 109
I173	P2V5_NAND0_PGOOD	TRUE 107
I170	P2V5_NAND1_PGOOD	TRUE 112
I171	PPVDD_LDO_NAND0_OCARINA	TRUE 107
I169	PPVDD_LDO_NAND1_OCARINA	TRUE 112

SoC

I167	I2C_SEEPROM_SCL	TRUE 6 12
I166	I2C_SEEPROM_SDA	TRUE 6 12

NAND (cont.)

I165	NAND0_OCARINA_TDEV1	TRUE 107
I164	NAND1_OCARINA_TDEV2	TRUE 112 136
I182	NAND0_S5E0_JTAG_TDO	TRUE 103 104
I181	NAND0_S5E1_JTAG_TDO	TRUE 104 105
I183	NAND0_S5E2_JTAG_TDO	TRUE 105 106
I163	NAND1_OCARINA_TDEV1	TRUE 112
I162	NAND1_OCARINA_TDEV2	TRUE 112 136
I187	P2V5_NAND0_EN_R	TRUE 107
I186	P2V5_NAND1_EN_R	TRUE 112

PMICs

I178	PMU_CLK32K_CLVR	TRUE 45 51 52 53
I179	PMU_VDDHI	TRUE 42
I177	SPMI_NUB_MPMU_CLK	TRUE 11 44
I178	SPMI_NUB_MPMU_DATA	TRUE 11 44
I176	SPMI_NUB_SPMU_CLK	TRUE 11 40
I175	SPMI_NUB_SPMU_DATA	TRUE 11 40
I174	SWD_NUB_PMU_SWCLK	TRUE 11
I173	SWD_NUB_PMU_SWDIO	TRUE 11
I170	DEBUG_SPMU_GPIO16	TRUE 45

WLBT

I116	PMU_CLK32K_WLBT	TRUE 45 101 102

I116	WLBT_RESET_L	TOP 1 TP	TPU867 TP-P4
I133	BT_TIME_SYNC	TRUE	6 101 102
I109	WLBT_PWR_EN	TRUE	44 45 101 102

8 101 102

IPD

I198	CAPSLOCK_LED_EN	TRUE 128
I197	IOXP1_RESET_L	TRUE 128
I191	IOXP2_RESET_L	TRUE 128
I190	KBDBKLT_ISET_KEYB	TRUE 127 135

Sensor

I201	AIRFLOW_C_THMSNS	TRUE 45 65
I200	AIRFLOW_L_THMSNS	TRUE 45 65
I199	AIRFLOW_R_THMSNS	TRUE 45 65
I194	DCIN_VSENSE	TRUE 45 59
I193	FINSTACK_L_THMSNS	TRUE 45 65
I192	FINSTACK_R_THMSNS	TRUE 45 65
I191	MPMU_THMSNS	TRUE 45 65
I190	P1V8VDDH_THMSNS_1	TRUE 45 65
I189	P1V8VDDH_THMSNS_2	TRUE 45 65
I197	P1V8VDDH_THMSNS_3	TRUE 45 65
I188	P3V8AON_THMSNS	TRUE 45 65
I196	PBUS_VSENSE	TRUE 45 59
I184	SOC_THMSNS_1	TRUE 45 65
I185	SPMU_THMSNS	TRUE 45 65
I182	WING_L_THMSNS	TRUE 45 65
I183	WING_R_THMSNS	TRUE 45 65
I181	WLBT_THMSNS	TRUE 45 65

I418	PP5V0_HDMI_DDC_CONN	TRUE	90
I419	PPVDD_LOW_S2	TRUE	145
I416	PP0V8_S2_CLVR_VDDDIG	TRUE	135 144
I417	PP1V8_S2SW_SNS	TRUE	141

I425	PP5V_S2_HDMI	VOLTAGE=5	TRUE 93 94
I423	PP1V2_AON_SPMU	VOLTAGE=1.2V	TRUE 38
I422	PP1V8_AON_SPMU	VOLTAGE=1.8V	TRUE 38 45
I426	PP1V2_AWAKESW_DP2HDMI	VOLTAGE=1.2V	TRUE 92 94
I424	PP3V3_SW_ACE5	VOLTAGE=3.3V	TRUE 29 31 35 136
I429	PP3V3_AWAKESW_DP2HDMI	VOLTAGE=3.3V	TRUE 90 92 93 94

USB2 DEBUG PPs

P3MM SM	PPU800 BOTTOM PP 1	TP_MACAW0_DEBUG_SWDCLK	77
P3MM SM	PPU801 BOTTOM PP 1	TP_MACAW0_DEBUG_SWDDAT	77
P3MM SM	PPU802 BOTTOM PP 1	TP_MACAW1_DEBUG_SWDCLK	77
P3MM SM	PPU803 BOTTOM PP 1	TP_MACAW1_DEBUG_SWDDAT	77
P3MM SM	PPU804 BOTTOM PP 1	TP_MACAW2_DEBUG_SWDCLK	85
P3MM SM	PPU805 BOTTOM PP 1	TP_MACAW2_DEBUG_SWDDAT	85

I460	ACT_GND	TRUE	131 136
I459	ACT_GND	TRUE	131 136

I438	I2C_UPC0_ATCRTMR0_SCL	TRUE	73 75 78 136
I437	I2C_UPC0_ATCRTMR0_SDA	TRUE	73 75 78 136
I439	ATCRTMR0_RESET_L	TRUE	73 75 78
I440	I2C_UPC1_ATCRTMR1_SCL	TRUE	73 76 78
I441	I2C_UPC1_ATCRTMR1_SDA	TRUE	73 76 78
I443	ATCRTMR1_RESET_L	TRUE	73 76 78
I442	UPC01_5V_EN	TRUE	79 89
I444	I2C_UPC2_ATCRTMR2_SCL	TRUE	82 84 86 147
I446	I2C_UPC2_ATCRTMR2_SDA	TRUE	82 84 86 147
I445	ATCRTMR2_RESET_L	TRUE	82 84 86
I447	UPC23_5V_EN	TRUE	83 84 87
I449	USBC2_SBU1	TRUE	69 70 84
I448	USBC2_SBU2	TRUE	69 70 84

Digital mic

I405	PDM_DMIC_DATA1	TRUE	10 126 134
I411	PDM_DMIC_DATA4	TRUE	10 126 134
I410	PDM_DMIC_CLK7	TRUE	13 126 134
I412	PDM_DMIC_CLK8	TRUE	13 126 134
126 I404	PDM_DMIC_CLK7_1V8	TOP 1 TP PLACE_NEAR=JR940.1:20MM	TPU865 TP-P4
I408	PDM_DMIC_DATA1_1V8	TRUE	126
I407	PP1V8_DMIC	TRUE	126
I406	PDM_DMIC_CLK8_1V8	TRUE	126
I405	PDM_DMIC_DATA4_1V8	TRUE	126
	GND	TOP 1 TP	TPU814 TP-P4

SSD

I686	TP_NAND0_S5E0_ANI0_VREF	TRUE 103 134
I688	TP_NAND0_S5E0_ANI1_VREF	TRUE 103 134
I687	TP_NAND0_S5E1_ANI0_VREF	TRUE 104 134
I689	TP_NAND0_S5E1_ANI1_VREF	TRUE 104 134
I693	TP_NAND0_S5E2_ANI0_VREF	TRUE 105 134
I695	TP_NAND0_S5E2_ANI1_VREF	TRUE 105 134
I696	TP_NAND0_S5E3_ANI0_VREF	TRUE 106 134
I694	TP_NAND0_S5E3_ANI1_VREF	TRUE 106 134
I690	TP_NAND1_S5E0_ANI0_VREF	TRUE 108 134
I698	TP_NAND1_S5E0_ANI1_VREF	TRUE 108 134
I692	TP_NAND1_S5E1_ANI0_VREF	TRUE 109 134
I691	TP_NAND1_S5E1_ANI1_VREF	TRUE 109 134
I697	TP_NAND1_S5E2_ANI0_VREF	TRUE 110 134
I699	TP_NAND1_S5E2_ANI1_VREF	TRUE 110 134
I700	TP_NAND1_S5E3_ANI0_VREF	TRUE 111 134
I698	TP_NAND1_S5E3_ANI1_VREF	TRUE 111 134

I418	FTCAM_RESET_L	TRUE	7 114

I465	ATCRTMR0_RESET_1V2_1V8_MCW_L	TRUE	89 150
I457	UPC0_SER_DBG	TRUE	73 75
I461	UPC1_SER_DBG	TRUE	73 76
I462	UPC2_SER_DBG	TRUE	82 84
I463	USBC5_UV_SNS	TRUE	35

I458	SPI_UPC0_R_CLK	TRUE	73 75
I139	UPC_PMU_RESET_1V2	TRUE	44 45
I464	UPC_PMU_RESET_1V2_R	TRUE	45 75 76 84 136 138 140
140 138 136 84 76 75 45	UPC_PMU_RESET_1V2_R	BOTTOM 1 TP	TPU6800 TP-P4
I138	EDP_BKLT_1V29_EN	TRUE	45 117
I137	IPD_PWR_EN	TRUE	45 128 131
I136	IPD_PWR_EN_PMU	TRUE	45

44	IN	GND_MPMU_QUIET	1 PP	PPU8A0	P3MM
39	IN	GND_SPMU_QUIET	1 PP	PPU8A3	P3MM
40	IN	GND_SPMU_QUIET	1 PP	PPU8A5	P3MM
135 52 5	IN	CLVR_VDDH_UVWARN_L	1 PP	PPU8A8	P3MM
48 5	IN	P1V8VDDH_ILIMIT_THROTTLE_L	1 PP	PPU8A9	P3MM
48 45 44	IN	P1V8VDDH_PWR_EN	1 PP	PPU8B0	P3MM
137 48 44	IN	P1V8VDDH_SLP_L	1 PP	PPU8B1	P3MM
45 33	IN	P3V8AON_LPM	1 PP	PPU8B2	P3MM
11 5	IN	PMU_UVWARN_ILIMIT_L	1 PP	PPU8B7	P3MM

Viper PPs

143 135 134 PP1V8_S1_CLVR_VDDH

NOSTUFF	PPU890	TP-5016 SM
NOSTUFF	PPU891	TP-5016 SM
NOSTUFF	PPU892	TP-5016 SM
NOSTUFF	PPU893	TP-5016 SM

SoC TP Nets

6	TP_AP_GPIO37	BOTTOM 1 TP	TPU880 TP-P4
6	TP_AP_GPIO38	BOTTOM 1 TP	TPU881 TP-P4
6	TP_AP_GPIO39	BOTTOM 1 TP	TPU882 TP-P4
6	I2C_ENET_SCL	BOTTOM 1 TP	TPU883 TP-P4
6	I2C_ENET_SDA	BOTTOM 1 TP	TPU884 TP-P4
6	TP_MTP_I2C0_SCL	BOTTOM 1 TP	TPU885 TP-P4
6	TP_MTP_I2C0_SDA	BOTTOM 1 TP	TPU886 TP-P4
148	IPD_MTP_FUNC_1	BOTTOM 1 TP	TPU887 TP-P4
6	TP_MTR_FUNC2	BOTTOM 1 TP	TPU888 TP-P4
6	TP_MTR_FUNC6	BOTTOM 1 TP	TPU889 TP-P4
6	TP_MTR_FUNC7	BOTTOM 1 TP	TPU890 TP-P4
10	TP_AOP_FUNC0	BOTTOM 1 TP	TPU891 TP-P4
10	TP_AOP_FUNC1	BOTTOM 1 TP	TPU892 TP-P4
10	TP_AOP_PDM_IN_CLK1	BOTTOM 1 TP	TPU893 TP-P4
136 10	TP_AON_SLEEP1_RESET_L	BOTTOM 1 TP	TPU894 TP-P4
10	TP_AOP_LEAP_MADI_IN	BOTTOM 1 TP	TPU895 TP-P4
10	TP_AOP_LEAP_MADI_OUT	BOTTOM 1 TP	TPU896 TP-P4
10	LOM_PMU_RESET_EN	BOTTOM 1 TP	TPU897 TP-P4
10	TP_NUB_GPIO8	BOTTOM 1 TP	TPU898 TP-P4

I439	SPI_GYRO_CS_L	TRUE 10 66

DCDC Debug 3mm PP

135 29	I227	PP3V3_HVLDO_OUT	BOTTOM 1 PP	PPU2	
136 35 31 29	I228	PP3V3_SW_ACE5	BOTTOM 1 PP	PPU3	
29	I226	HVSW_G2	BOTTOM 1 PP	PPU4	
134 31 30	I225	USBC5_CC1	BOTTOM 1 PP	PPU5	
135 57 32 10	I224	I2C_SMC_UPC_SCL	BOTTOM 1 PP	PPU6	
135 57 32 10	I223	I2C_SMC_UPC_SDA	BOTTOM 1 PP	PPU7	

I488	DP2HDMI_PWR_EN	TRUE	93 94
I487	HDMI_PWR_EN	TRUE	44 90
I490	DP2HDMI_RESET_L	TRUE	44 93
I489	SPI_DP2HDMI_CS_L	TRUE	92
I483	HDMI_CEC_AOP_RX	TRUE	10 93
I482	HDMI_CEC_AOP_TX	TRUE	10 93
I480	HDMI_CECFET_EN	TRUE	44 90
I485	CEC_FLT	TRUE	90 93
I484	IPD_TOUCH_RESET_L	TRUE	45 130 131
I435	SPI_IPD_TOUCH_CS_CONN_L	TRUE	130 131

I405	MPMU_3V8_ISENSE	TRUE	45 60
I407	SPMU_3V8_ISENSE	TRUE	45 60
I406	P1V8VDDH_HS_ISENSE	TRUE	45 59
I408	BMON_ISENSE	TRUE	45 59

SYNC_MASTER=J416_CSZSOXY_MLB_C_2.0.1 PMU_AUTO=2/19/2021

PAGE TITLE

FCT 3 and PMU TPs

Apple Inc.

DRAWING NUMBER 051-08156 SIZE D

REVISION 3.0.0

BRANCH evt-1

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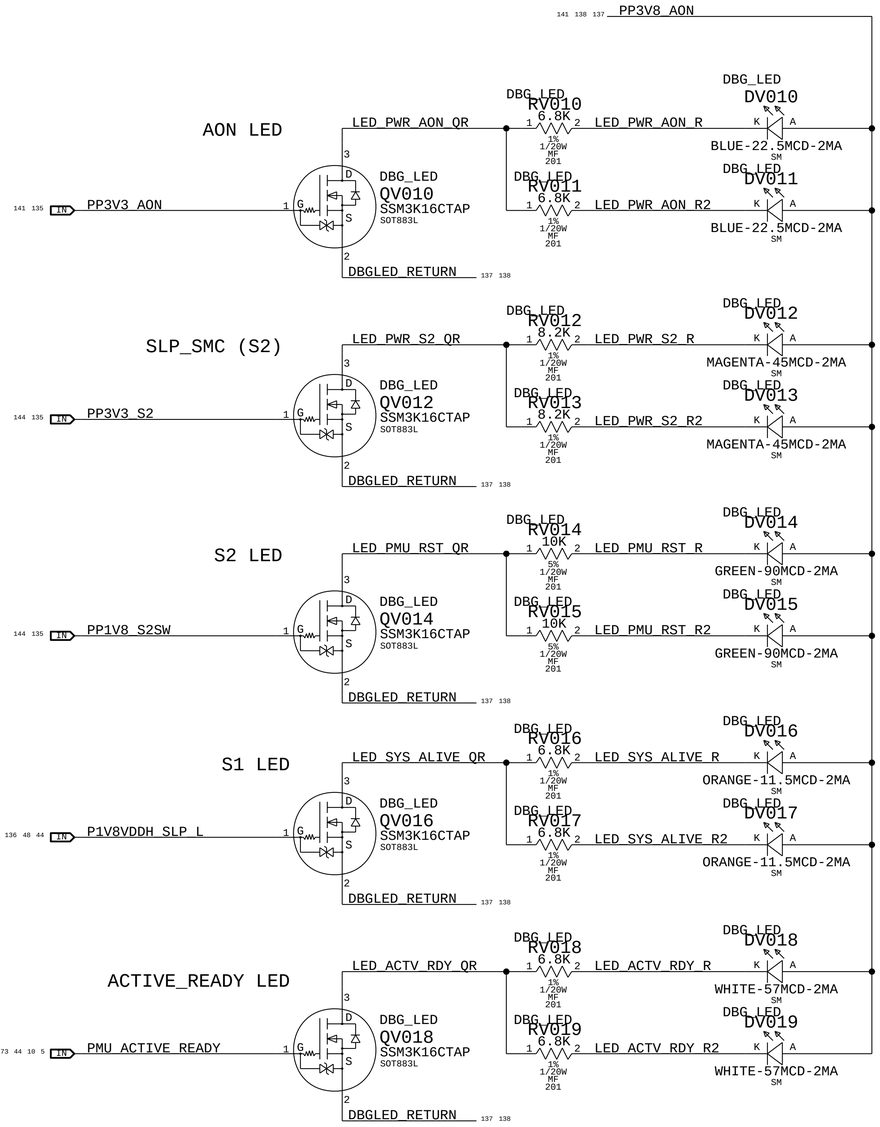
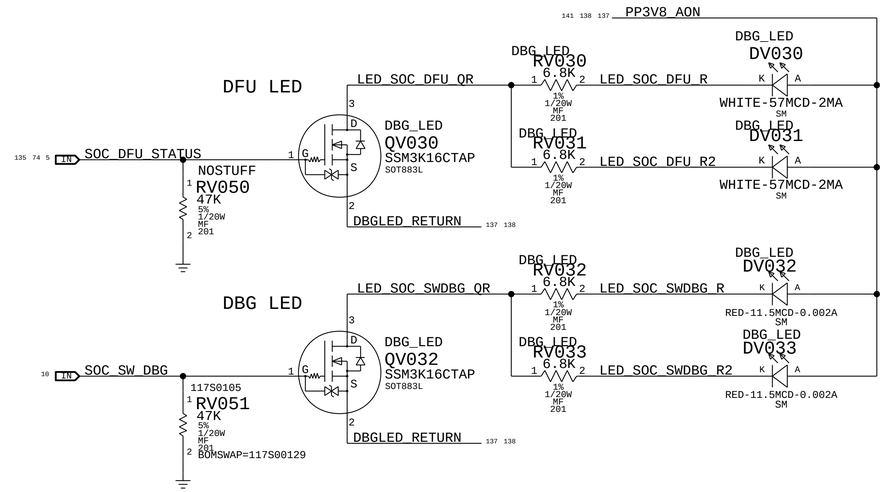
SHEET 136 OF 159

Debug LEDs





BOM_COST_GROUP=DEBUG

SYNC_MASTER= SYNC_DATE=

PAGE TITLE: Debug: LEDs, Koba

Apple Inc.

DRAWING NUMBER 051-08156 SIZE D

REVISION 3.0.0

BRANCH evt-1

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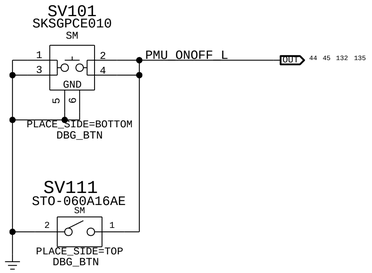
POWER BUTTON

Imitate a user-facing Power Button press, many functions:
- Press to Wake from any state
- Combine with RSLOC (see RSLOC)
- Hold for 8sec to trigger "one-finger reset"
- - Similar to PMU RESET, except SW gets a warning to initiate panic-flow



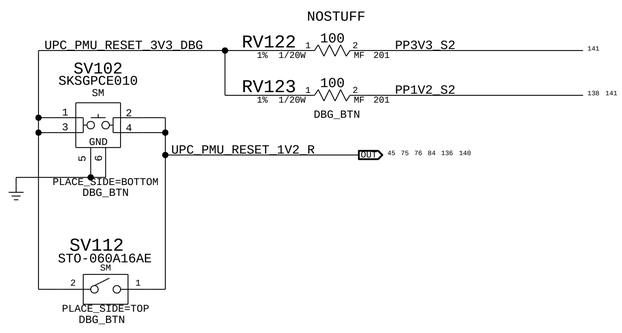
RSLOC BUTTON

Imitate a user-facing key combo Right-Shift + Left-Option + Control:
- Hold RSLOC 4sec, then press Power Button to initiate PMU RESET
- Hold RSLOC 4sec, then hold Power Button 4sec to power-cycle P3V8AON VR
- Hold Power Button 1sec, then hold RSLOC 10sec to trigger PMU RESET into DFU

(continue holding first button when second button is added)

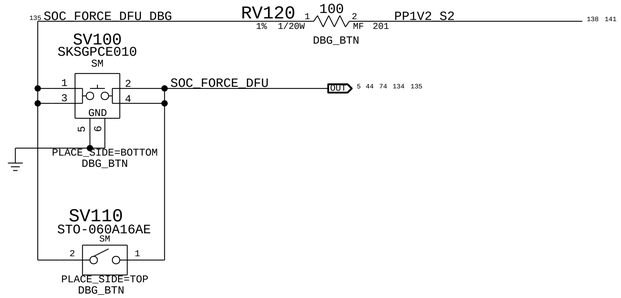
PMU RESET

PMU transitions to OFF and automatically proceeds up to AWAKE



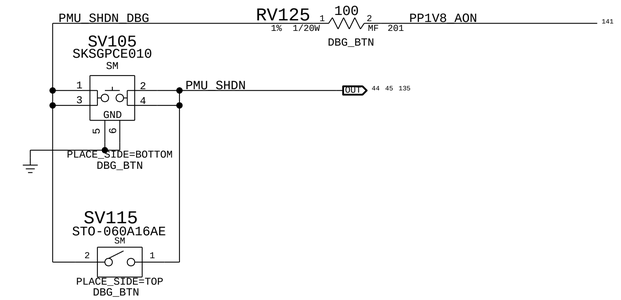
FORCE DFU

Hold during OFF->AWAKE transition to enter SOC's "Debug Firmware Update" mode



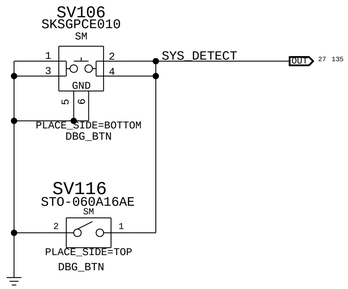
PMU SHUTDOWN

PMU transitions to OFF state and waits for a WAKE source*



SYS_DETECT (Battery Disconnect)

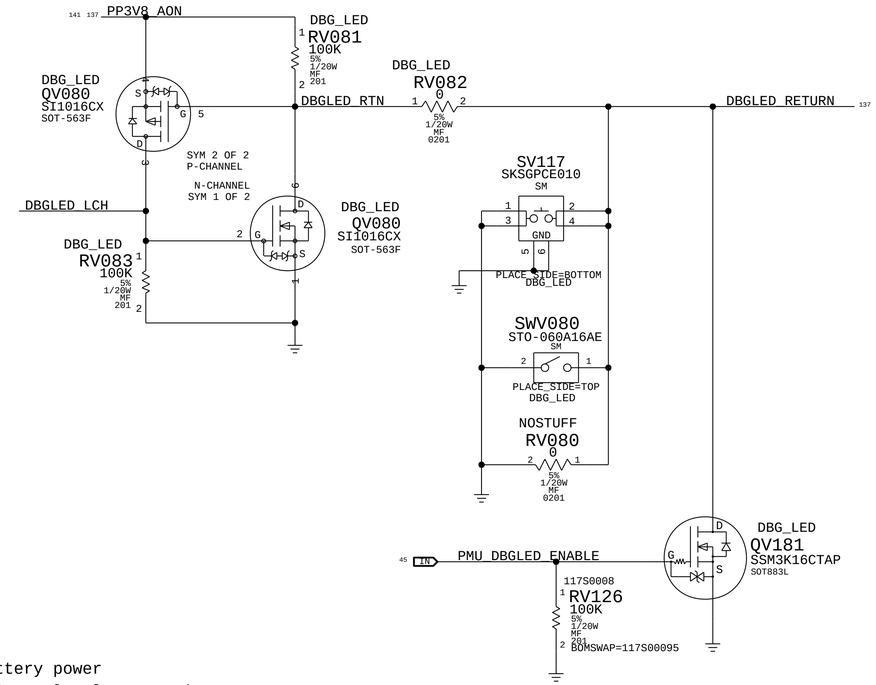
Imitate unplugging the battery signal flex, to disconnect MLB from Battery power
- Disconnect all DCIN sources, then hold SYS_DETECT for 2sec. MLB will completely power down



Debug LED Latch

Press button once to engage.
Remove power to disengage.

Debug LED Enable



*WAKE sources in OFF:
CHGR_AUX_OK (DCIN present)
IPD_LID_OPEN_1V8 (Lid is open)
PMU_ONOFF_L (User Power Button)

BOM_COST_GROUP=DEBUG

PAGE TITLE
Debug: Buttons

Apple Inc.

DRAWING NUMBER 051-08156
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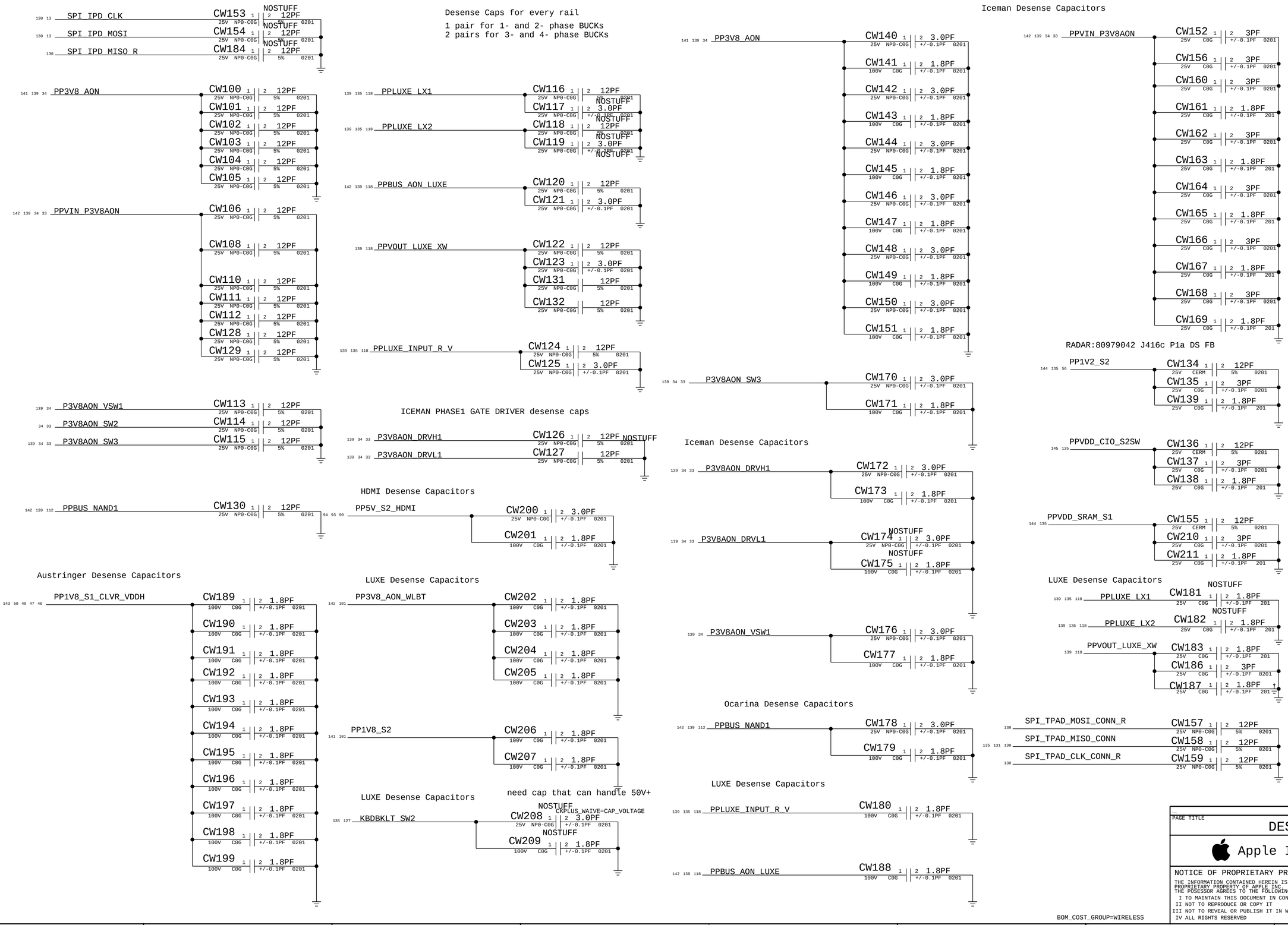
SPI IPD CLK
SPI IPD MOSI
SPI IPD MISO R
CW153 CW154 CW184 12PF NOSTUFF
PP3V8_AON
CW100 CW101 CW102 CW103 CW104 CW105 12PF
PPVIN_P3V8AON
CW106 CW108 CW110 CW111 CW112 CW128 CW129 12PF
P3V8AON_VSW1
P3V8AON_SW2
P3V8AON_SW3
CW113 CW114 CW115 12PF
PPBUS_NAND1
CW130 12PF
Austringer Desense Capacitors
PP1V8_S1_CLVR_VDDH
CW189 CW190 CW191 CW192 CW193 CW194 CW195 CW196 CW197 CW198 CW199 1.8PF
Desense Caps for every rail
1 pair for 1- and 2- phase BUCKs
2 pairs for 3- and 4- phase BUCKs
PPLUXE_LX1
PPLUXE_LX2
CW116 CW117 CW118 CW119 12PF 3.0PF NOSTUFF
PPBUS_AON_LUXE
CW120 CW121 12PF 3.0PF
PPVOUT_LUXE_XW
CW122 CW123 CW131 CW132 12PF 3.0PF
PPLUXE_INPUT_R_V
CW124 CW125 12PF 3.0PF
ICEMAN PHASE1 GATE DRIVER desense caps
P3V8AON_DRVH1
P3V8AON_DRVL1
CW126 CW127 12PF NOSTUFF
HDMI Desense Capacitors
PP5V_S2_HDMI
CW200 CW201 3.0PF 1.8PF
LUXE Desense Capacitors
PP3V8_AON_WLBT
CW202 CW203 CW204 CW205 1.8PF
PP1V8_S2
CW206 CW207 1.8PF
LUXE Desense Capacitors
KBDBKLT_SW2
CW208 CW209 3.0PF 1.8PF NOSTUFF
CKPLUS_WAIVE=CAP_VOLTAGE
need cap that can handle 50V+
PP3V8_AON
CW140 CW141 CW142 CW143 CW144 CW145 CW146 CW147 CW148 CW149 CW150 CW151 3.0PF 1.8PF
P3V8AON_SW3
CW170 CW171 3.0PF 1.8PF
Iceman Desense Capacitors
P3V8AON_DRVH1
P3V8AON_DRVL1
CW172 CW173 CW174 CW175 3.0PF 1.8PF NOSTUFF
P3V8AON_VSW1
CW176 CW177 3.0PF 1.8PF
Ocarina Desense Capacitors
PPBUS_NAND1
CW178 CW179 3.0PF 1.8PF
LUXE Desense Capacitors
PPLUXE_INPUT_R_V
CW180 1.8PF
PPBUS_AON_LUXE
CW188 1.8PF
Iceman Desense Capacitors
PPVIN_P3V8AON
CW152 CW156 CW160 CW161 CW162 CW163 CW164 CW165 CW166 CW167 CW168 CW169 3PF 1.8PF
RADAR:80979042 J416c P1a DS FB
PP1V2_S2
CW134 CW135 CW139 12PF 3PF 1.8PF
PPVDD_CIO_S2SW
CW136 CW137 CW138 12PF 3PF 1.8PF
PPVDD_SRAM_S1
CW155 CW210 CW211 12PF 3PF 1.8PF
LUXE Desense Capacitors
PPLUXE_LX1
PPLUXE_LX2
PPVOUT_LUXE_XW
CW181 CW182 CW183 CW186 CW187 1.8PF 3PF NOSTUFF
SPI_TPAD_MOSI_CONN_R
SPI_TPAD_MISO_CONN
SPI_TPAD_CLK_CONN_R
CW157 CW158 CW159 12PF
BOM_COST_GROUP=WIRELESS
PAGE TITLE
DESENSE_1
Apple Inc.
DRAWING NUMBER 051-08156
SIZE D
REVISION 3.0.0
BRANCH evt-1
PAGE 281 OF 700
SHEET 139 OF 159
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SOC USB DFU MUX

141 PP3V3_AON
PACK_OPTION=VITAMINC
20K LIMITS USB MINI-B
FROM BACK POWERING MLB
VITAMIN-C:YES
RX412
20K
5% 1/20W TK 0201
PACK_OPTION=VITAMINC
VITAMIN-C:YES
BYPASS=UX410::5MM
CX410
0.1UF
10% 10V X5R-CERM 0201
PP3V3_AON_DFUMUX
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
9 2UA MAX IDD
VCC
VIT-C CONN
LVL SHFTR
PACK_OPTION=VITAMINC
UX410
PI3USB102EZLE
TQFN-THICKSTNCL
CRITICAL
VITAMIN-C:YES
GND
SEL
OE*
140 USB2_ATC0_VITC_CONN_P
140 USB2_ATC0_VITC_CONN_N
M+ M-
Y+ Y-
1 USB2_ATC0_LS_MUX_P
2 USB2_ATC0_LS_MUX_N
140 150 B1
150 140 B1 USB2_ATC0_LS_P
150 140 B1 USB2_ATC0_LS_N
D+ D-
DEBUG SPI ACE
10 DFUMUX_SEL 140
PACK_OPTION=VITAMINC
VITAMIN-C:YES
RX410
100K
5% 1/20W TK 0201

SEL	OUTPUT
L	VIT-C (M)
H	TYPE-C (D)

PACK_OPTION=VITAMINC
VITAMIN-C:NO
RX414
0
0% 1/20W TK 0201
NO_XNET_CONNECTION=1
150 140 USB2_ATC0_LS_P — USB2_ATC0_LS_MUX_P 140 150
VITAMIN-C:NO
RX416
0
0% 1/20W TK 0201
NO_XNET_CONNECTION=1
150 140 USB2_ATC0_LS_N — USB2_ATC0_LS_MUX_N 140 150

SOC DBG MUX

141 140 PP3V3_AON
PACK_OPTION=VITAMINC
20K LIMITS USB MINI-B
FROM BACK POWERING MLB
VITAMIN-C:YES
RX413
20K
5% 1/20W TK 0201
PACK_OPTION=VITAMINC
VITAMIN-C:YES
BYPASS=UX411::5MM
CX411
0.1UF
10% 10V X5R-CERM 0201
PP3V3_AON_DBGMUX_VC
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
9 2UA MAX IDD
VCC
VIT-C CONN
LVL SHFTR
PACK_OPTION=VITAMINC
UX411
PI3USB102EZLE
TQFN-THICKSTNCL
CRITICAL
VITAMIN-C:YES
GND
SEL
OE*
140 USB_DBG_VITC_CONN_P
140 USB_DBG_VITC_CONN_N
M+ M-
Y+ Y-
1 USB_DBG_LS_MUX_P
2 USB_DBG_LS_MUX_N
140 150 B1
150 140 B1 USB_DBG_LS_P
150 140 B1 USB_DBG_LS_N
D+ D-
DEBUG SPI ACE
10 KISMUX_SEL 140
PACK_OPTION=VITAMINC
VITAMIN-C:YES
RX411
100K
5% 1/20W TK 0201

SEL	OUTPUT
L	VIT-C (M)
H	TYPE-C (D)

PACK_OPTION=VITAMINC
VITAMIN-C:NO
RX415
0
0% 1/20W TK 0201
NO_XNET_CONNECTION=1
150 140 USB_DBG_LS_P — USB_DBG_LS_MUX_P 140 150
VITAMIN-C:NO
RX417
0
0% 1/20W TK 0201
NO_XNET_CONNECTION=1
150 140 USB_DBG_LS_N — USB_DBG_LS_MUX_N 140 150

MACAW DBG MUX

USING PI3USB102 FOR SINGLE ENDED CONTROL SIGNAL: <RDAR://72709253>

141 140 PP3V3_AON
PACK_OPTION=VITAMINC
20K LIMITS USB MINI-B
FROM BACK POWERING MLB
VITAMIN-C:YES
RX418
20K
5% 1/20W TK 0201
PACK_OPTION=VITAMINC
VITAMIN-C:YES
BYPASS=UX412::10MM
CX415
0.1UF
10% 10V X5R-CERM 0201
PP3V3_AON_DBGMUX
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1500
9 2UA MAX IDD
VCC
(1V2 IF DRIVEN BY MLB, 1V8 BY VITAMIN C)
<RDAR://75096896> J404: 1.8V ON PARROT RESET W/ VIOSEL=GND
VIT-C CONN
353S4037
UX412
PI3USB102EZLE
TQFN-THICKSTNCL
CRITICAL
VITAMIN-C:YES
GND
SEL
OE*
140 VITC_RTMR_RESET_1V8_L
140 VITC_RTMR_PWR_EN
M+ M-
Y+ Y-
1 ATCRTMR0_RESET_1V2_1V8_MCW_L OUT 140 150
2 USB0_3V3_LDO_EN_VITC 150
140 78 74 IN ATCRTMR0_RESET_1V2_L
150 USB0_3V3_LDO_EN_VITC
D+ D-
10 DFUMUX_SEL 140
PACK_OPTION=VITAMINC
RTMRMUX_OE_L 150
VITAMIN-C:YES
RX422
20K
5% 1/20W TK 0201
PACK_OPTION=VITAMINC

SEL	OUTPUT
L	VIT-C (M)
H	TYPE-C (D)

VITAMIN-C:NO
RX420
0
0201 0% 1/20W TK
NO_XNET_CONNECTION=1
PACK_OPTION=VITAMINC
140 78 74 ATCRTMR0_RESET_1V2_L — ATCRTMR0_RESET_1V2_1V8_MCW_L 150

VITAMIC-C MK2 CONNECTOR

PACK_OPTION=VITAMINC
516S1074
SILK_PART=VITAMIN-C
VITAMIN-C:YES
JX401
AA25D-S036VA1
F-ST-SM
39 40 41 42

SOC ATC0 DFU
140 USB2_ATC0_VITC_CONN_P
140 USB2_ATC0_VITC_CONN_N
SOC KIS DBG
140 USB_DBG_VITC_CONN_P
140 USB_DBG_VITC_CONN_N
RFU
RFU
RFU

1	2		VITC_RESET_L
3	4		DFUMUX_SEL
5	6		KISMUX_SEL
7	8		SOC_DOCK_CONNECT_VITAMINC
9	10		NC_DC_MUX_SEL
11	12	B1	SWD_SOC_SWDIO
13	14	B1	SWD_SOC_SWCLK
15	16	IN	SOC_JTAG_TDO
17	18	OUT	SOC_JTAG_TDI
19	20	IN	UART_DEBUGPRT_R2D
21	22	OUT	UART_DEBUGPRT_D2R
23	24	IN	UART_SMC_DEBUGPRT_R2D
25	26	OUT	UART_SMC_DEBUGPRT_D2R
27	28		VITC_RTMR_RESET_1V8_L
29	30		VITC_RTMR_PWR_EN
31	32		PP1V8_S2
33	34		PP1V2_S2
35	36		
37	38		

NC NC NC NC NC NC

141 PP3V8_AON
VITAMIN-C:YES
CX405
0.1UF
10% 16V X5R-CERM 0201
BYPASS=JX401::10MM
PACK_OPTION=VITAMINC
VITAMIN-C:YES
CX406
0.1UF
10% 16V X5R-CERM 0201
BYPASS=JX401::10MM
PACK_OPTION=VITAMINC
PP5V_S2_MAIN
VITAMIN-C:YES
CX404
2.2UF
20% 25V X6S-CERM 0402
BYPASS=JX401::9MM
PACK_OPTION=VITAMINC

PACK_OPTION=VITAMINC
NOSTUFF
RX402
1/20W TK 0% 0 0201
141 PP3V3_S2
PACK_OPTION=VITAMINC
VITAMIN-C:YES
RX403
1/20W TK 0% 0 0201
141 140 PP1V2_S2
PP1V2_S2_VITAMINC_Q
VOLTAGE=1.2V
PACK_OPTION=VITAMINC
VITAMIN-C:YES
RX430
100K
5% 1/20W TK 0201
PACK_OPTION=VITAMINC
VITAMIN-C:YES
QX400
DMP2160UWQ
SOT323
S G D
UPC_PMU_RESET_1V2_R IN 136 138 76 84
KOBA
SWD_SOC_SWDIO
SWD_SOC_SWCLK
JTAG_SOC_TDO
JTAG_SOC_TDI
SOC UART
SMC UART

VITAMIN-C:YES CX401 0.1UF 10% 16V X5R-CERM 0201
BYPASS=JX401::5MM PACK_OPTION=VITAMINC
VITAMIN-C:YES CX402 0.1UF 10% 16V X5R-CERM 0201
BYPASS=JX401::5MM PACK_OPTION=VITAMINC
VITAMIN-C:YES CX403 0.1UF 10% 16V X5R-CERM 0201
BYPASS=JX401::5MM PACK_OPTION=VITAMINC

TO SOC
1V2 NUB AOP, S2
47K PD ON SOC PAGE
135 10 OUT SOC_DOCK_CONNECT
PACK_OPTION=VITAMINC
RX491
100
5% 1/20W TK 0201
SOC_DOCK_CONNECT — SOC_DOCK_CONNECT_UPC IN 89
FROM ACE GPIO 7, PMOS OPEN DRAIN
1V2 S2
PACK_OPTION=VITAMINC
VITAMIN-C:YES
RX492
10
5% 1/20W TK 0201
SOC_DOCK_CONNECT_VITAMINC 140
FROM VITAMIN C
GPIO 7, 1V2 S2

BOM_COST_GROUP=DEBUG

SYNC_MASTER=J414_RUENJOU_MLB_C_0.54.1 SYNC_DATE=10/26/2021
PAGE TITLE
DEBUG: VITAMIN-C
Apple Inc.
DRAWING NUMBER 051-08156 SIZE D
REVISION 3.0.0
BRANCH evt-1
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VBAT

PPVBAT_AON
PPVBAT_AON 135
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=13.05V
PPVBAT_AON 27 28

DCIN

73 PPDCIN_AON
82 PPDCIN_AON
PPDCIN_AON 29 135
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=20V
PPDCIN_AON

PBUS

141 28 PPBUS_AON
PPBUS_AON 135
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=13.05V
PPBUS_AON 28 141
PPBUS_AON 42
PPBUS_AON 59
PPBUS_AON 60
PPBUS_AON 60
PPBUS_AON 60
PPBUS_AON 60
PPBUS_AON 61
PPBUS_AON 61
PPBUS_AON 59
PPBUS_AON 59
PPBUS_AON 59
PPBUS_AON 61
PPBUS_AON 61
PPBUS_AON 131
PPBUS_AON 67
PPBUS_AON 36

ICEMAN VMAIN

139 34 PP3V8_AON
PP3V8_AON 135
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=3.8V
PP3V8_AON 26
17 PP3V8_AON
PP3V8_AON 60
PP3V8_AON 60
PP3V8_AON 62
PP3V8_AON 62
PP3V8_AON 62
PP3V8_AON 62
80 PP3V8_AON
88 PP3V8_AON
PP3V8_AON 122
PP3V8_AON 123
PP3V8_AON 123
PP3V8_AON
PP3V8_AON 123
PP3V8_AON 124
PP3V8_AON 124
PP3V8_AON 124
PP3V8_AON 133
PP3V8_AON
PP3V8_AON 63
PP3V8_AON 61
PP3V8_AON
PP3V8_AON
PP3V8_AON 117
PP3V8_AON 63
PP3V8_AON 27
PP3V8_AON 137 138
PP3V8_AON 140
PP3V8_AON 36 64 65
PP3V8_AON 55
PP3V8_AON 94
PP3V8_AON 70

PP5V_S2

55 PP5V_S2_MAIN
PP5V_S2_MAIN 30 135
MAKE_BASE=TRUE
PP5V_S2_MAIN 33
PP5V_S2_MAIN 48
PP5V_S2_MAIN 49 50
PP5V_S2_MAIN 93
PP5V_S2_MAIN 118
PP5V_S2_MAIN 63
PP5V_S2_MAIN 131
PP5V_S2_MAIN 63
PP5V_S2_MAIN
PP5V_S2_MAIN
PP5V_S2_MAIN 29
PP5V_S2_MAIN 36 141
PP5V_S2_MAIN 140
PP5V_S2_MAIN 67
PP5V_S2_MAIN 36 141

PP1V2 AWAKE SYSTEM LOADS

145 41 39 37 PP1V2_AWAKE
SPMU Buck12(8)
PP1V2_AWAKE
PP1V2_AWAKE 99
PP1V2_AWAKE 118
PP1V2_AWAKE 122
PP1V2_AWAKE 122 123
PP1V2_AWAKE 123 124
PP1V2_AWAKE 56
PP1V2_AWAKE 58
PP1V2_AWAKE 116
PP1V2_AWAKE 99

PP1V2 S2 SYSTEM LOADS

144 43 41 37 PP1V2_S2
MPMU Buck8(8)
PP1V2_S2 29
PP1V2_S2 31 32
PP1V2_S2 48
PP1V2_S2 56 57 58 130
PP1V2_S2 73 75 76 79
121 114 PP1V2_S2
PP1V2_S2
78 PP1V2_S2
PP1V2_S2
78 PP1V2_S2
PP1V2_S2 82 84
86 PP1V2_S2
PP1V2_S2
77 PP1V2_S2
PP1V2_S2 101
77 PP1V2_S2
PP1V2_S2
85 PP1V2_S2
PP1V2_S2 126
86 PP1V2_S2
PP1V2_S2 127
78 PP1V2_S2
PP1V2_S2
94 PP1V2_S2
PP1V2_S2 130
66 PP1V2_S2
PP1V2_S2 93
26 PP1V2_S2
PP1V2_S2 138
26 PP1V2_S2
PP1V2_S2
77 PP1V2_S2
PP1V2_S2 122
PP1V2_S2 67
PP1V2_S2 14
PP1V2_S2
PP1V2_S2 132
PP1V2_S2 132
PP1V2_S2 140

SPMU 1V8 S2 SYSTEM LOADS

145 41 39 37 PP1V8_S2
SPMU Buck19(3)
PP1V8_S2 38
PP1V8_S2
PP1V8_S2 28 29
PP1V8_S2
PP1V8_S2
PP1V8_S2 75 76 79
PP1V8_S2 77
85 PP1V8_S2
PP1V8_S2 77
PP1V8_S2 101 139
PP1V8_S2 107
PP1V8_S2 112
PP1V8_S2 116
PP1V8_S2 126
PP1V8_S2 126
PP1V8_S2 14
PP1V8_S2 66
PP1V8_S2
PP1V8_S2 56 57 58
84 PP1V8_S2
PP1V8_S2 87
PP1V8_S2 38
PP1V8_S2 95
PP1V8_S2
PP1V8_S2 140
94 93 PP1V8_S2
PP1V8_S2 58
114 PP1V8_S2
PP1V8_S2

MPMU LDO1 S2 SYSTEM LOADS

144 42 PP3V3_S2
MPMU LDO1
PP3V3_S2 67
PP3V3_S2 99
PP3V3_S2 127
PP3V3_S2 93
PP3V3_S2 138
PP3V3_S2
PP3V3_S2
141 77 PP3V3_S2
PP3V3_S2 29 35
141 77 PP3V3_S2
141 85 PP3V3_S2
PP3V3_S2
PP3V3_S2
89 PP3V3_S2
PP3V3_S2 140
77 PP3V3_S2
PP3V3_S2 73 75 76 79 141
PP3V3_S2 82 84 141

MPMU 3V3 AON SYSTEM LOADS

42 PP3V3_AON
MPMU LDO4
Portable Only
PP3V3_AON 135 137
MAKE_BASE=TRUE
VOLTAGE=3.3V
PP3V3_AON 128
PP3V3_AON
PP3V3_AON 120
PP3V3_AON 27
PP3V3_AON 140
PP3V3_AON 140

PP1V2_ATCRTMR01_VDDIO

135
MAKE_BASE=TRUE
VOLTAGE=1V
PP1V2_ATCRTMR01_VDDIO 73 80
PP1V2_ATCRTMR01_VDDIO 72 74
PP1V2_ATCRTMR01_VDDIO 71 74
PP1V2_ATCRTMR01_VDDIO 71
PP1V2_ATCRTMR01_VDDIO 72
PP1V2_ATCRTMR01_VDDIO 71
PP1V2_ATCRTMR01_VDDIO 72
PP1V2_ATCRTMR01_VDDIO 71
PP1V2_ATCRTMR01_VDDIO 72
PP1V2_ATCRTMR01_VDDIO 71
PP1V2_ATCRTMR01_VDDIO 72
PP1V2_ATCRTMR01_VDDIO 78
PP1V2_ATCRTMR01_VDDIO 78
PP1V2_ATCRTMR01_VDDIO 78

PP1V2_ATCRTMR2_VDDIO

135
MAKE_BASE=TRUE
VOLTAGE=1V
PP1V2_ATCRTMR2_VDDIO 81
PP1V2_ATCRTMR2_VDDIO 81 83
PP1V2_ATCRTMR2_VDDIO 81
PP1V2_ATCRTMR2_VDDIO 86
PP1V2_ATCRTMR2_VDDIO 86
PP1V2_ATCRTMR2_VDDIO 81
PP1V2_ATCRTMR2_VDDIO 81
PP1V2_ATCRTMR2_VDDIO 82 88
PP1V2_ATCRTMR2_VDDIO 86
PP1V2_ATCRTMR2_VDDIO 89

PP0V805_ATCRTMR01_VDD_FIXED

MAKE_BASE=TRUE
VOLTAGE=1V
PP0V805_ATCRTMR01_VDD_FIXED 71
PP0V805_ATCRTMR01_VDD_FIXED 72
PP0V805_ATCRTMR01_VDD_FIXED 80
PP0V805_ATCRTMR01_VDD_FIXED 71
PP0V805_ATCRTMR01_VDD_FIXED 72

PP0V805_ATCRTMR2_VDD_FIXED

MAKE_BASE=TRUE
VOLTAGE=1V
PP0V805_ATCRTMR2_VDD_FIXED 81
PP0V805_ATCRTMR2_VDD_FIXED 88
PP0V805_ATCRTMR2_VDD_FIXED 81

PP0V855_ATCRTMR01_VDD_CIO

MAKE_BASE=TRUE
VOLTAGE=1V
PP0V855_ATCRTMR01_VDD_CIO 71
PP0V855_ATCRTMR01_VDD_CIO 72
PP0V855_ATCRTMR01_VDD_CIO 73 80
GND 71
GND 72

PP0V855_ATCRTMR2_VDD_CIO

MAKE_BASE=TRUE
VOLTAGE=1V
PP0V855_ATCRTMR2_VDD_CIO 81
PP0V855_ATCRTMR2_VDD_CIO 82 88
GND 81

PP1V8_AON SYSTEM LOADS

144 42 PP1V8_AON
MPMU LDO1V8
PP1V8_AON 120
PP1V8_AON 138
PP1V8_AON 29
PP1V8_AON 45
PP1V8_AON
PP1V8_AON 117
PP1V8_AON 121
PP1V8_AON 130
PP1V8_AON 14

PP1V8 AWAKE SYSTEM LOADS

145 38 PP1V8_AWAKE
SPMU SW0
PP1V8_AWAKE 122
PP1V8_AWAKE 123 124
PP1V8_AWAKE 58

PP1V2 SPMU LDO3 AWAKE SYSTEM LOADS

38 PP1V2_AWAKESW_BLC
SPMU_LDO3
PP1V2_AWAKESW_BLC 135
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V2_AWAKESW_BLC 119

PP1V8 SPMU SW1 S2 SYSTEM LOADS

38 PP1V8_S2SW_SNS
SPMU_SW1
PP1V8_S2SW_SNS 136
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V8_S2SW_SNS 59 60 61 62 63

DISPLAY POWER SEQUENCER OUTPUT

117 PPBCON_AWAKESW_BKLTCONN_VIN
PPBCON_AWAKESW_BKLTCONN_VIN
MAKE_BASE=TRUE
VOLTAGE=3.8V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPBCON_AWAKESW_BKLTCONN_VIN 63
117 PPMDB_AWAKESW_TCON
PPMDB_AWAKESW_TCON 135
MAKE_BASE=TRUE
VOLTAGE=10V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPMDB_AWAKESW_TCON 62

ACE Rails

PP3V3_S2
MAKE_BASE=TRUE VOLTAGE=3.3V
Power to Ace2s from LDO7.
PP3V3_S2 OUT 73 75 76 79 141
PP3V3_S2 OUT 82 84 141
PP3V3_S2 OUT 78
PP3V3_S2 OUT 86
PP3V3_S2 OUT 85 141
PP3V3_S2 OUT 77 141
PP3V3_S2 OUT 77 141
PP3V3_S2 OUT 78
PP3V3_S2 OUT 86

33 PP5V_AON_P3V8AON
PP5V_AON_P3V8AON
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP5V_AON_P3V8AON 33

SYNC_MASTER=J416_JAMES_PENG_MLB_C_0.27.1
SYNC_DATE=10/26/2021

PAGE TITLE
POWER ALIASES 1

Apple Inc.

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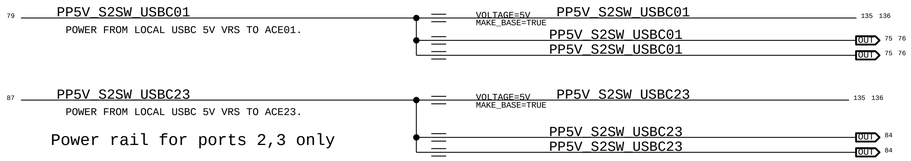
THIS PAGE WILL BE USED FOR SYSTEM / SUBSYSTEM ALIASES

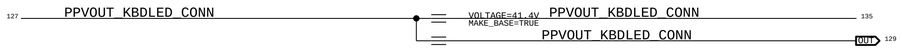
IPD: KEYBOARD / TRACKPAD

PP3V3_S2_IPD (LDO) ALIASES

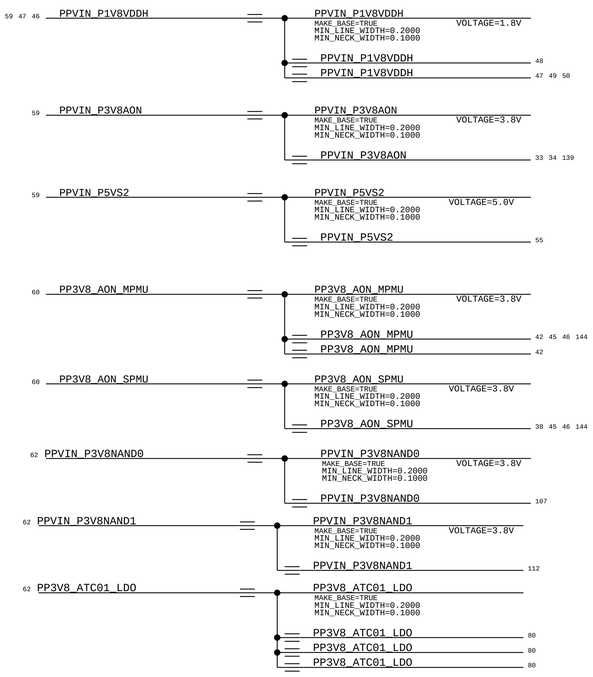
PP1V85_S2_IPD (LDO) ALIASES

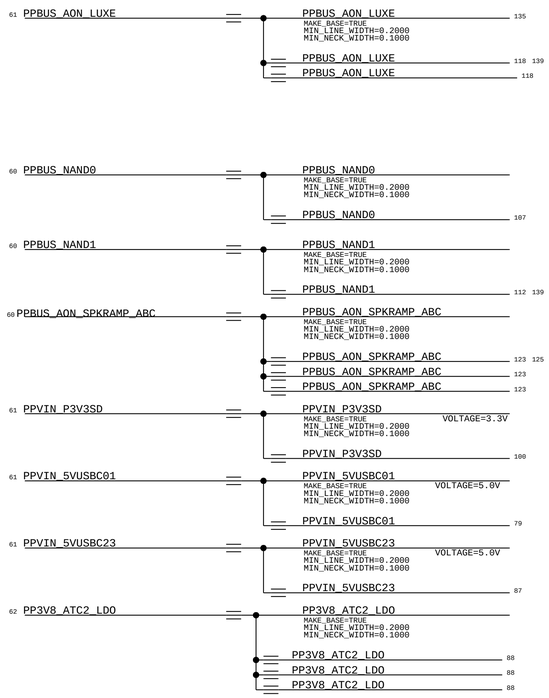


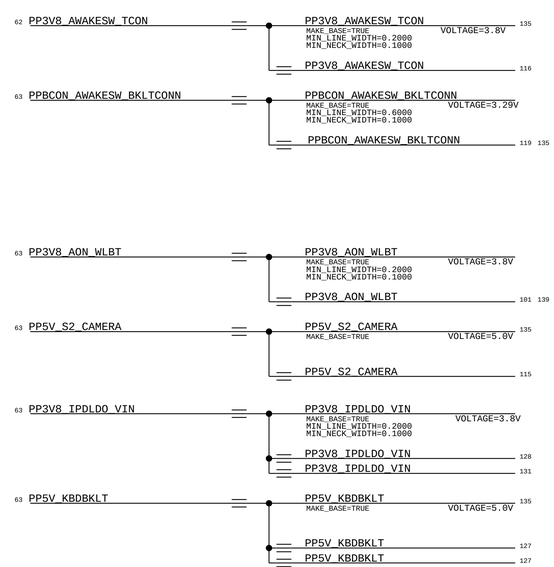
KEYBOARD BACKLIGHT

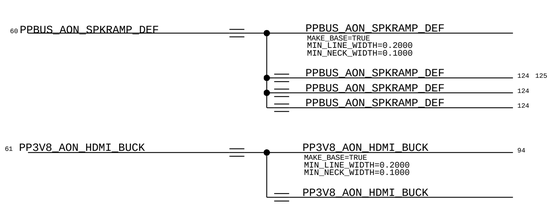


OUTPUT SENSOR ALIASES









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TODO_DT: Update VOLTAGE proporties for H14

CLVR0

51 PPVDD_PCPU1_AWAKESW
CLVR0 Buck0/HP0
PPVDD_PCPU1_AWAKESW (11)
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_PCPU1_AWAKESW (15)

51 PPVDD_PCPU_SRAM1_AWAKESW
CLVR0 Buck1/LP0
PPVDD_PCPU_SRAM1_AWAKESW (11)
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_PCPU_SRAM1_AWAKESW (15)

51 PPVDD_PCPU0_AWAKESW
CLVR0 Buck2/HP1
PPVDD_PCPU0_AWAKESW (11)
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_PCPU0_AWAKESW (15)

51 PPVDD_PCPU_SRAM0_AWAKESW
CLVR0 Buck3/LP1
PPVDD_PCPU_SRAM0_AWAKESW (11)
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_PCPU_SRAM0_AWAKESW (15)

CLVR1

52 PPVDD_GPU0_AWAKESW
CLVR1 Buck0/HP0
PPVDD_GPU0_AWAKESW (11)
MAKE_BASE=TRUE
VOLTAGE=1.00V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_GPU0_AWAKESW (15)

52 PPVDD_GPU_SRAM0_AWAKESW
CLVR1 Buck1/LP0
PPVDD_GPU_SRAM0_AWAKESW (11)
MAKE_BASE=TRUE
VOLTAGE=0.70V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_GPU_SRAM0_AWAKESW (15)

52 PPVDD_GPU1_AWAKESW
CLVR1 Buck2/HP1
PPVDD_GPU1_AWAKESW (11)
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_GPU1_AWAKESW (15)

52 PPVDD_GPU_SRAM1_AWAKESW
CLVR1 Buck3/LP1
PPVDD_GPU_SRAM1_AWAKESW (11)
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_GPU_SRAM1_AWAKESW (15)

CLVR2

53 PPVDD_ANE_AWAKESW
CLVR2 Buck0/HP0
PPVDD_ANE_AWAKESW (11)
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_ANE_AWAKESW (19)

53 PPVDD_ANE_SRAM_AWAKESW
CLVR2 Buck1/LP0
PPVDD_ANE_SRAM_AWAKESW (11)
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_ANE_SRAM_AWAKESW (19)

53 PPVDD_FABRIC_S1
CLVR2 Buck2/HP1
PPVDD_FABRIC_S1 (11)
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_FABRIC_S1 (20)

53 PPVDD_AFR_CS_S1
CLVR2 Buck3/LP1
PPVDD_AFR_CS_S1 (11)
MAKE_BASE=TRUE
VOLTAGE=0.70V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_AFR_CS_S1 (19)

139 50 49 47 46 PP1V8_S1_CLVR_VDDH
VR -> CLVR VDDH
PP1V8_S1_CLVR_VDDH (134 135 136)
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V8_S1_CLVR_VDDH (48)
PP1V8_S1_CLVR_VDDH (59)
PP1V8_S1_CLVR_VDDH (46 51 52 53)

CLVR0

51 PVDDPCPU1_FB — PVDDPCPU1_FB (15) MAKE_BASE=TRUE
51 PVDDPCPUSRAM1_FB — PVDDPCPUSRAM1_FB (15) MAKE_BASE=TRUE
51 PVDDPCPU0_FB — PVDDPCPU0_FB (15) MAKE_BASE=TRUE
51 PVDDPCPUSRAM0_FB — PVDDPCPUSRAM0_FB (15) MAKE_BASE=TRUE

CLVR1

52 PVDDGPU0_FB — PVDDGPU0_FB (15) MAKE_BASE=TRUE
52 PVDDGPUSRAM0_FB — PVDDGPUSRAM0_FB (15) MAKE_BASE=TRUE
52 PVDDGPU1_FB — PVDDGPU1_FB (15) MAKE_BASE=TRUE
52 PVDDGPUSRAM1_FB — PVDDGPUSRAM1_FB (15) MAKE_BASE=TRUE

CLVR2

53 PVDDANE_FB — PVDDANE_FB (19) MAKE_BASE=TRUE
53 PVDDANESRAM_FB — PVDDANESRAM_FB (19) MAKE_BASE=TRUE
53 PVDDFABRIC_FB — PVDDFABRIC_FB (20) MAKE_BASE=TRUE
53 PVDDAFRCS_FB — PVDDAFRCS_FB (19) MAKE_BASE=TRUE

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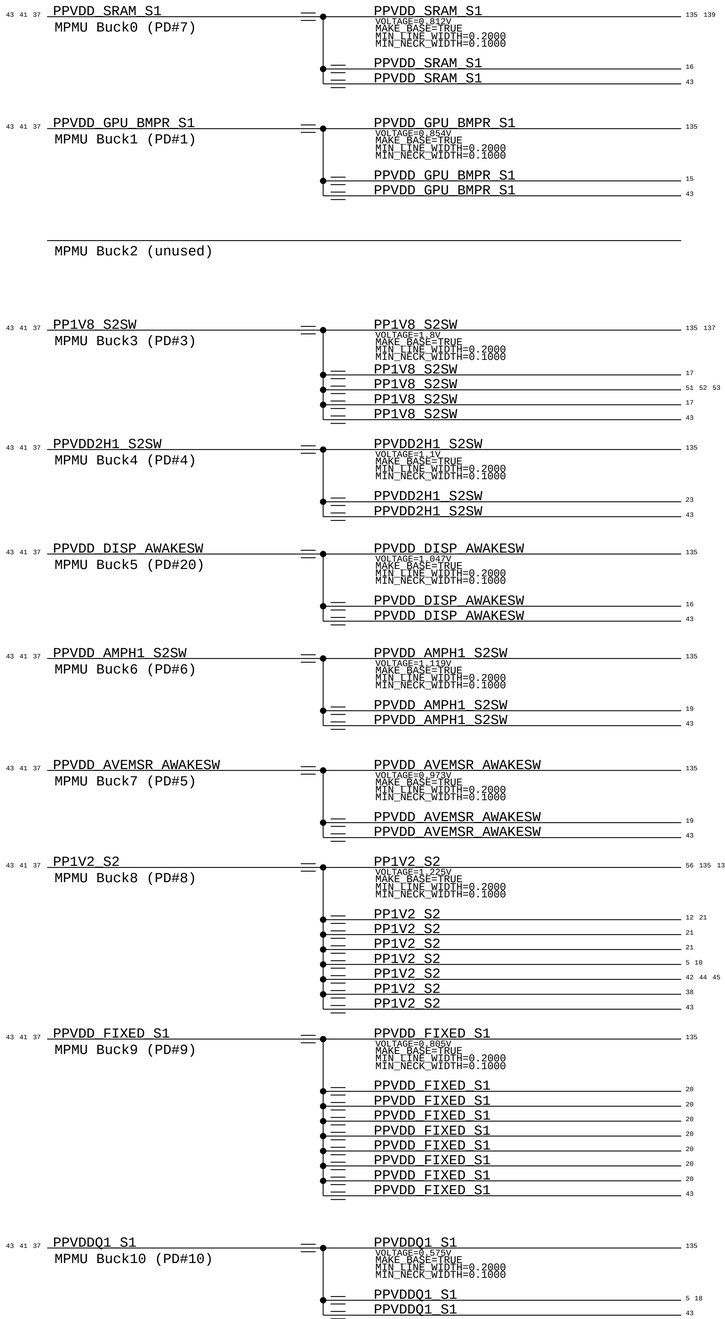
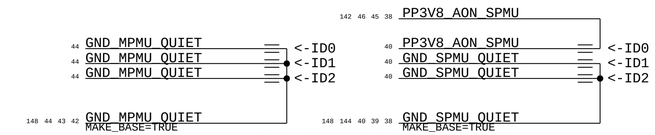


CONF_MS and _ID pin straps

MPMU1:
OTP Bank = MPMU1
SGPIO SID = n/a
SWD TINSTANCE = 0x0

SPMU:
OTP Bank = SPMU
SGPIO SID = 0x5
SWD TINSTANCE = 0x5

CONF_MS[1:0]: b00=SPMU, b01=MPMU2, b11=MPMU1
SPMU is used for both SPMU1 and SPMU2
0b10 setting is invalid



CONF_ID[1:0]: SGPIO SID[1:0] and SWD TINSTANCE[1:0]
CONF_ID[2]: SGPIO SID[3]
SWD TINSTANCE[3:2] is set in OTP: MPMU = b00, SPMU = b01
SGPIO SID[2] is set in OTP: MPMU = n/a, SPMU = b1

VOLTAGE property for SOC rails is based on the max of "Design-intended voltage" defined by Tunables Spec rev0.0.11, Table 13.1
Refer to xPMU BUCK pages for actual boot voltages

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41 39 37 PPVDD_DCS_S1
SPMU Buck0 (PD#17)
PPVDD_DCS_S1 135
VOLTAGE=1.06V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_DCS_S1 16
PPVDD_DCS_S1 39

41 39 37 PPVDDQ0_S1
SPMU Buck1 (PD#13)
PPVDDQ0_S1 135
VOLTAGE=0.575V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDDQ0_S1 5 18
PPVDDQ0_S1 39

41 39 37 PPVDD_ECPU_SRAM_AWAKESW
SPMU Buck2 (PD#2)
PPVDD_ECPU_SRAM_AWAKESW
VOLTAGE=1.06V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_ECPU_SRAM_AWAKESW 15
PPVDD_ECPU_SRAM_AWAKESW 39

41 39 37 141 PP1V8_S2
SPMU Buck3 (PD#19)
PP1V8_S2 135
VOLTAGE=1.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V8_S2 42 44
PP1V8_S2 38
PP1V8_S2 39

41 39 37 PPVDD2H0_S2SW
SPMU Buck4 (PD#14)
PPVDD2H0_S2SW 135
VOLTAGE=1.1V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD2H0_S2SW 12 22
PPVDD2H0_S2SW 39

41 39 37 PPVDD_SOC_S1
SPMU Buck5 (PD#11)
PPVDD_SOC_S1 135
VOLTAGE=0.904V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_SOC_S1 16
PPVDD_SOC_S1 39

41 39 37 PPVDD_CIO_S2SW
SPMU Buck6 (PD#16)
PPVDD_CIO_S2SW 135 139
VOLTAGE=0.855V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_CIO_S2SW 19
PPVDD_CIO_S2SW 39

41 39 37 PPVDD_DISP2_AWAKESW
SPMU Buck7 (PD#15)
Not used on S designs
PPVDD_DISP2_AWAKESW
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.0838
MIN_NECK_WIDTH=0.0838
PPVDD_DISP2_AWAKESW
PPVDD_DISP2_AWAKESW 39

41 39 37 141 PP1V2_AWAKE
SPMU Buck8 (PD#12)
PP1V2_AWAKE 135
VOLTAGE=1.225V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V2_AWAKE 21
PP1V2_AWAKE 21
PP1V2_AWAKE 21
PP1V2_AWAKE 21
PP1V2_AWAKE 21
PP1V2_AWAKE 19 21
PP1V2_AWAKE 4 5 8 9
PP1V2_AWAKE 12
PP1V2_AWAKE 21
PP1V2_AWAKE 12
PP1V2_AWAKE 21
PP1V2_AWAKE 15
PP1V2_AWAKE 38
PP1V2_AWAKE 44
PP1V2_AWAKE 39

41 39 37 PPVDD_AMPH0_S2SW
SPMU Buck9 (PD#21)
PPVDD_AMPH0_S2SW 135
VOLTAGE=1.19V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_AMPH0_S2SW 19
PPVDD_AMPH0_S2SW 39

41 39 37 PPVDD_ECPU_AWAKESW
SPMU Buck10 (PD#0)
PPVDD_ECPU_AWAKESW 135
VOLTAGE=1.06V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_ECPU_AWAKESW 15
PPVDD_ECPU_AWAKESW 39

38 PPVDD_LOW_S2
SPMU LDO0
PPVDD_LOW_S2 136
VOLTAGE=0.72V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_LOW_S2 16
PPVDD_LOW_S2 16

SPMU LDO1

SPMU LDO2

SPMU LDO3

SPMU LDO4

SPMU LDO5

SPMU LDO6

SPMU LDO1V8
-Internal Only-

SPMU LDO1V2
-Internal Only-

141 38 PP1V8_AWAKE
SPMU SW0
PP1V8_AWAKE 135
VOLTAGE=1.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V8_AWAKE 12

SPMU SW1

SPMU SW2

VOLTAGE property for SOC rails is based on the max of "Design-intended voltage" defined by Tunables Spec rev0.0.11, Table 13.1
Refer to xPMU BUCK pages for actual boot voltages

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LPDPTX

93	LPDP_INT_DATA_C_P<0>	LPDP_INT_DATA_C_P<0>	7 116	MAKE_BASE=TRUE
93	LPDP_INT_DATA_C_N<0>	LPDP_INT_DATA_C_N<0>	7 116	MAKE_BASE=TRUE
93	LPDP_INT_DATA_C_P<1>	LPDP_INT_DATA_C_P<1>	7 116	MAKE_BASE=TRUE
93	LPDP_INT_DATA_C_N<1>	LPDP_INT_DATA_C_N<1>	7 116	MAKE_BASE=TRUE
93	LPDP_INT_DATA_C_P<2>	LPDP_INT_DATA_C_P<2>	7 116	MAKE_BASE=TRUE
93	LPDP_INT_DATA_C_N<2>	LPDP_INT_DATA_C_N<2>	7 116	MAKE_BASE=TRUE
93	LPDP_INT_DATA_C_P<3>	LPDP_INT_DATA_C_P<3>	7 116	MAKE_BASE=TRUE
93	LPDP_INT_DATA_C_N<3>	LPDP_INT_DATA_C_N<3>	7 116	MAKE_BASE=TRUE
93	LPDP_INT_AUX_C_P	LPDP_INT_AUX_C_P	7 116	MAKE_BASE=TRUE
93	LPDP_INT_AUX_C_N	LPDP_INT_AUX_C_N	7 116	MAKE_BASE=TRUE
148	LPDP_INT_HPD	LPDP_INT_HPD	7 116 135 148	MAKE_BASE=TRUE

NAND

8	NC_PCIE_CLK100M_NAND0_1P	NC_PCIE_CLK100M_NAND0_1P	MAKE_BASE=TRUE
8	NC_PCIE_CLK100M_NAND0_1N	NC_PCIE_CLK100M_NAND0_1N	MAKE_BASE=TRUE
8	NC_PCIE_CLK100M_NAND0_3P	NC_PCIE_CLK100M_NAND0_3P	MAKE_BASE=TRUE
8	NC_PCIE_CLK100M_NAND0_3N	NC_PCIE_CLK100M_NAND0_3N	MAKE_BASE=TRUE
8	NC_PCIE_CLK100M_NAND1_1P	NC_PCIE_CLK100M_NAND1_1P	MAKE_BASE=TRUE
8	NC_PCIE_CLK100M_NAND1_1N	NC_PCIE_CLK100M_NAND1_1N	MAKE_BASE=TRUE
8	NC_PCIE_CLK100M_NAND1_3P	NC_PCIE_CLK100M_NAND1_3P	MAKE_BASE=TRUE
8	NC_PCIE_CLK100M_NAND1_3N	NC_PCIE_CLK100M_NAND1_3N	MAKE_BASE=TRUE
103	SWD_NAND0_S5E0_S5E1_SWCLK	SWD_NAND0_S5E0_S5E1_SWCLK	MAKE_BASE=TRUE
104	SWD_NAND0_S5E0_S5E1_SWCLK		
105	SWD_NAND0_S5E2_S5E3_SWCLK	SWD_NAND0_S5E2_S5E3_SWCLK	MAKE_BASE=TRUE
106	SWD_NAND0_S5E2_S5E3_SWCLK		
103	SWD_NAND0_S5E0_S5E1_SWDIO	SWD_NAND0_S5E0_S5E1_SWDIO	MAKE_BASE=TRUE
104	SWD_NAND0_S5E0_S5E1_SWDIO		
105	SWD_NAND0_S5E2_S5E3_SWDIO	SWD_NAND0_S5E2_S5E3_SWDIO	MAKE_BASE=TRUE
106	SWD_NAND0_S5E2_S5E3_SWDIO		
108	SWD_NAND1_S5E0_S5E1_SWCLK	SWD_NAND1_S5E0_S5E1_SWCLK	MAKE_BASE=TRUE
109	SWD_NAND1_S5E0_S5E1_SWCLK		
110	SWD_NAND1_S5E2_S5E3_SWCLK	SWD_NAND1_S5E2_S5E3_SWCLK	MAKE_BASE=TRUE
111	SWD_NAND1_S5E2_S5E3_SWCLK		
108	SWD_NAND1_S5E0_S5E1_SWDIO	SWD_NAND1_S5E0_S5E1_SWDIO	MAKE_BASE=TRUE
109	SWD_NAND1_S5E0_S5E1_SWDIO		
110	SWD_NAND1_S5E2_S5E3_SWDIO	SWD_NAND1_S5E2_S5E3_SWDIO	MAKE_BASE=TRUE
111	SWD_NAND1_S5E2_S5E3_SWDIO		

USB3

	SWD_UPC_SWDIO3_R	SWD_UPC_SWDIO3_R	MAKE_BASE=TRUE

ATC3 - HDMI

9	DP_DP2HDMI_DATA_P<2>	DP_DP2HDMI_DATA_P<2>	
93	DP_DP2HDMI_DATA_P<2>		MAKE_BASE=TRUE
9	DP_DP2HDMI_DATA_N<2>	DP_DP2HDMI_DATA_N<2>	
93	DP_DP2HDMI_DATA_N<2>		MAKE_BASE=TRUE
9	DP_DP2HDMI_DATA_P<3>	DP_DP2HDMI_DATA_P<3>	
93	DP_DP2HDMI_DATA_P<3>		MAKE_BASE=TRUE
9	DP_DP2HDMI_DATA_N<3>	DP_DP2HDMI_DATA_N<3>	
93	DP_DP2HDMI_DATA_N<3>		MAKE_BASE=TRUE
9	DP_DP2HDMI_DATA_P<1>	DP_DP2HDMI_DATA_P<1>	
93	DP_DP2HDMI_DATA_P<1>		MAKE_BASE=TRUE
9	DP_DP2HDMI_DATA_N<1>	DP_DP2HDMI_DATA_N<1>	
93	DP_DP2HDMI_DATA_N<1>		MAKE_BASE=TRUE
9	DP_DP2HDMI_DATA_P<0>	DP_DP2HDMI_DATA_P<0>	
93	DP_DP2HDMI_DATA_P<0>		MAKE_BASE=TRUE
9	DP_DP2HDMI_DATA_N<0>	DP_DP2HDMI_DATA_N<0>	
93	DP_DP2HDMI_DATA_N<0>		MAKE_BASE=TRUE
9	DP_DP2HDMI_AUX_P	DP_DP2HDMI_AUX_P	
93	DP_DP2HDMI_AUX_P		MAKE_BASE=TRUE
9	DP_DP2HDMI_AUX_N	DP_DP2HDMI_AUX_N	
93	DP_DP2HDMI_AUX_N		MAKE_BASE=TRUE

USBC

9	NC_USB_C0_HPD	NC_USB_C0_HPD	MAKE_BASE=TRUE
9	NC_USB_C1_HPD	NC_USB_C1_HPD	MAKE_BASE=TRUE
9	NC_USB_C2_HPD	NC_USB_C2_HPD	MAKE_BASE=TRUE

ENET

SD

8	PCIE_SD_UHS2_R2D_C_P	PCIE_SD_UHS2_R2D_C_P	97 MAKE_BASE=TRUE
8	PCIE_SD_UHS2_R2D_C_N	PCIE_SD_UHS2_R2D_C_N	97 MAKE_BASE=TRUE
8	PCIE_SD_UHS2_D2R_P	PCIE_SD_UHS2_D2R_P	97 MAKE_BASE=TRUE
8	PCIE_SD_UHS2_D2R_N	PCIE_SD_UHS2_D2R_N	97 MAKE_BASE=TRUE
8	PCIE_CLK100M_SD_UHS2_P	PCIE_CLK100M_SD_UHS2_P	97 MAKE_BASE=TRUE
8	PCIE_CLK100M_SD_UHS2_N	PCIE_CLK100M_SD_UHS2_N	97 MAKE_BASE=TRUE
8	SD_UHS2_RESET_L	SD_UHS2_RESET_L	99 MAKE_BASE=TRUE
8	SD_UHS2_CLKREQ_L	SD_UHS2_CLKREQ_L	99 MAKE_BASE=TRUE
146 6	NC_SDEXP_SEL	NC_SDEXP_SEL	146 MAKE_BASE=TRUE

Deleted SDEXP_RESET_L alias Checking with Harshi

146 6	NC_SDEXP_SEL	NC_SDEXP_SEL	146 MAKE_BASE=TRUE

			MAKE_BASE=TRUE
9	NC_EUSB_ATC3P	NC_EUSB_ATC3P	
9	NC_EUSB_ATC3N	NC_EUSB_ATC3N	

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SIGNAL ALIASES - 1 (HIGH SPEED)

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LSRX/TX Monitor for Columbus.

89	IN	CIO_ATC2_LSRX_3V3	MAKE_BASE=TRUE	CIO_ATC2_LSRX_3V3	OUT 95
89	IN	CIO_ATC2_LSTX_3V3	MAKE_BASE=TRUE	CIO_ATC2_LSTX_3V3	OUT 95

I2C (3V3) for Columbus.

136 86 84 82	BI	I2C_UPC2_ATCRTMR2_SDA		I2C_UPC2_ATCRTMR2_SDA	BI 95
136 86 84 82	BI	I2C_UPC2_ATCRTMR2_SCL		I2C_UPC2_ATCRTMR2_SCL	BI 95

HDMI ARKANOID ALIASING

147 82		I2C_HDMI_DEBUG_SCL		I2C_HDMI_DEBUG_SCL	92 148
147		I2C_HDMI_DEBUG_SCL			
147 82		I2C_HDMI_DEBUG_SDA		I2C_HDMI_DEBUG_SDA	92 148
147		I2C_HDMI_DEBUG_SDA			
147 82		DP2HDMI_RESET_R_L		DP2HDMI_RESET_R_L	92 93 147
			MAKE_BASE=TRUE		
147 93 92		DP2HDMI_RESET_R_L		DP2HDMI_RESET_R_L	82 147
147		I2C_HDMI_DEBUG_SCL	MAKE_BASE=TRUE	I2C_HDMI_DEBUG_SCL	82 147
147		I2C_HDMI_DEBUG_SDA	MAKE_BASE=TRUE	I2C_HDMI_DEBUG_SDA	82 147
93 92 90		HDMI_HPD_IN	MAKE_BASE=TRUE	HDMI_HPD_IN	82
148 92		DPRX_INT_HPD	MAKE_BASE=TRUE	DPRX_INT_HPD	82
93 92		DPRX_AUX_N	MAKE_BASE=TRUE	DPRX_AUX_N	82
92		TP_COBRA_GPIO6	MAKE_BASE=TRUE	TP_COBRA_GPIO6	
93 92		DPRX_AUX_P	MAKE_BASE=TRUE	DPRX_AUX_P	82
92 90		HDMI_DDC_5V_SDA	MAKE_BASE=TRUE	HDMI_DDC_5V_SDA	82
92 90		HDMI_DDC_5V_SCL	MAKE_BASE=TRUE	HDMI_DDC_5V_SCL	82
			MAKE_BASE=TRUE		

COLUMBUS_REDRIVER_ALIASING

95	IN	USBC_ATC2_R2D_LS_C_P<1>	MAKE_BASE=TRUE	USBC_ATC2_R2D_LS_C_P<1>	81
95	IN	USBC_ATC2_R2D_LS_C_N<1>	MAKE_BASE=TRUE	USBC_ATC2_R2D_LS_C_N<1>	81
95	IN	USBC_ATC2_R2D_LS_C_P<2>	MAKE_BASE=TRUE	USBC_ATC2_R2D_LS_C_P<2>	81
95	IN	USBC_ATC2_R2D_LS_C_N<2>	MAKE_BASE=TRUE	USBC_ATC2_R2D_LS_C_N<2>	81
95	BI	USBC_ATC2_D2R_LS_P<1>	MAKE_BASE=TRUE	USBC_ATC2_D2R_LS_P<1>	81
95	BI	USBC_ATC2_D2R_LS_N<1>	MAKE_BASE=TRUE	USBC_ATC2_D2R_LS_N<1>	81
95	BI	USBC_ATC2_D2R_LS_P<2>	MAKE_BASE=TRUE	USBC_ATC2_D2R_LS_P<2>	81
95	BI	USBC_ATC2_D2R_LS_N<2>	MAKE_BASE=TRUE	USBC_ATC2_D2R_LS_N<2>	81

Internal signal aliases - Copied or debug circuitry added between.

	USB2_ATC1_LS_P	MAKE_BASE=TRUE	USB2_ATC1_LS_P	77 89
	USB2_ATC1_LS_N	MAKE_BASE=TRUE	USB2_ATC1_LS_N	77 89
	USB2_ATC2_LS_P	MAKE_BASE=TRUE	USB2_ATC2_LS_P	85 89
	USB2_ATC2_LS_N	MAKE_BASE=TRUE	USB2_ATC2_LS_N	85 89

89 9	EUSB_ATC0_P	MAKE_BASE=TRUE	EUSB_ATC0_P	BI 77
89 9	EUSB_ATC0_N	MAKE_BASE=TRUE	EUSB_ATC0_N	BI 77
89 9	EUSB_ATC1_P	MAKE_BASE=TRUE	EUSB_ATC1_P	BI 77
89 9	EUSB_ATC1_N	MAKE_BASE=TRUE	EUSB_ATC1_N	BI 77
89 9	EUSB_ATC2_P	MAKE_BASE=TRUE	EUSB_ATC2_P	BI 85
89 9	EUSB_ATC2_N	MAKE_BASE=TRUE	EUSB_ATC2_N	BI 85

100 45	SD_PWR_EN	MAKE_BASE=TRUE	SD_PWR_EN	

5	NC_CLVR_GPIO2		NC_CLVR_GPIO2	MAKE_BASE=TRUE
5	NC_CLVR_GPIO5		NC_CLVR_GPIO5	MAKE_BASE=TRUE
5	NC_CLVR_GPIO9		NC_CLVR_GPIO9	MAKE_BASE=TRUE
5	NC_CLVR_SPMI3_SCLK		NC_CLVR_SPMI3_SCLK	MAKE_BASE=TRUE
5	NC_CLVR_SPMI3_SDATA		NC_CLVR_SPMI3_SDATA	MAKE_BASE=TRUE
5	NC_CLVR_SPMI4_SCLK		NC_CLVR_SPMI4_SCLK	MAKE_BASE=TRUE
5	NC_CLVR_SPMI4_SDATA		NC_CLVR_SPMI4_SDATA	MAKE_BASE=TRUE
6	NC_AP_GPIO35		NC_AP_GPIO35	MAKE_BASE=TRUE
6	NC_AP_GPIO36		NC_AP_GPIO36	MAKE_BASE=TRUE
6	NC_AP_UART2_R2D		NC_AP_UART2_R2D	MAKE_BASE=TRUE
6	NC_AP_UART2_D2R		NC_AP_UART2_D2R	MAKE_BASE=TRUE
6	NC_AP_UART2_R2D_RTS_L		NC_AP_UART2_R2D_RTS_L	MAKE_BASE=TRUE
6	NC_AP_UART2_D2R_CTS_L		NC_AP_UART2_D2R_CTS_L	MAKE_BASE=TRUE
6	NC_AP_I2S2_MCK		NC_AP_I2S2_MCK	MAKE_BASE=TRUE
6	NC_AP_I2S3_DIN		NC_AP_I2S3_DIN	MAKE_BASE=TRUE
6	NC_AP_I2S3_DOUT		NC_AP_I2S3_DOUT	MAKE_BASE=TRUE
6	NC_AP_I2S3_BCLK		NC_AP_I2S3_BCLK	MAKE_BASE=TRUE
6	NC_AP_I2S3_LRCK		NC_AP_I2S3_LRCK	MAKE_BASE=TRUE
149 6	NC_AP_I2S3_MCK		NC_AP_I2S3_MCK 149	MAKE_BASE=TRUE
7	NC_LPDPRX_RX_D1_P		NC_LPDPRX_RX_D1_P	MAKE_BASE=TRUE
7	NC_LPDPRX_RX_D1_N		NC_LPDPRX_RX_D1_N	MAKE_BASE=TRUE
7	NC_LPDPRX_AUX_D0P		NC_LPDPRX_AUX_D0P	MAKE_BASE=TRUE
7	NC_LPDPRX_AUX_D1P		NC_LPDPRX_AUX_D1P	MAKE_BASE=TRUE
7	NC_SENSOR0_CLK		NC_SENSOR0_CLK	MAKE_BASE=TRUE
8	NC_GP_PCIE_TX2_P		NC_GP_PCIE_TX2_P	MAKE_BASE=TRUE
8	NC_GP_PCIE_TX2_N		NC_GP_PCIE_TX2_N	MAKE_BASE=TRUE
8	NC_GP_PCIE_RX2_P		NC_GP_PCIE_RX2_P	MAKE_BASE=TRUE
8	NC_GP_PCIE_RX2_N		NC_GP_PCIE_RX2_N	MAKE_BASE=TRUE
8	NC_GP_PCIE_REF_CLK2_P		NC_GP_PCIE_REF_CLK2_P	MAKE_BASE=TRUE
8	NC_GP_PCIE_REF_CLK2_N		NC_GP_PCIE_REF_CLK2_N	MAKE_BASE=TRUE
8	NC_GP_PCIE_CLKREQ2_L		NC_GP_PCIE_CLKREQ2_L	MAKE_BASE=TRUE
8	NC_GP_PCIE_PERST2_L		NC_GP_PCIE_PERST2_L	MAKE_BASE=TRUE
10	NC_AOP_SPI1_SSIN		NC_AOP_SPI1_SSIN	MAKE_BASE=TRUE
10	NC_AOP_UART2_RXD		NC_AOP_UART2_RXD	MAKE_BASE=TRUE
10	NC_AOP_UART2_TXD		NC_AOP_UART2_TXD	MAKE_BASE=TRUE
10	NC_SMC_GPIO6		NC_SMC_GPIO6	MAKE_BASE=TRUE
10	NC_SMC_GPIO7		NC_SMC_GPIO7	MAKE_BASE=TRUE
10	NC_SMC_GPIO8		NC_SMC_GPIO8	MAKE_BASE=TRUE
10	NC_NUB_GPIO0		NC_NUB_GPIO0	MAKE_BASE=TRUE
10	NC_NUB_GPIO6		NC_NUB_GPIO6	MAKE_BASE=TRUE
26	NC_SE_K1		NC_SE_K1 MAKE_BASE=TRUE	
26	NC_SE_K8		NC_SE_K8 MAKE_BASE=TRUE	

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FTCAM_ENABLE_1V8_OUT — FTCAM_ENABLE_1V8_OUT (MAKE_BASE=TRUE) — 115, 114, 135

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AMR1_OR_ND_1V8 — AMR1_OR_ND_1V8 (MAKE_BASE=TRUE) — 121, 148
AMR1_OR_ND_1V8 — AMR1_OR_ND_1V8 (MAKE_BASE=TRUE) — 121, 148
AMR1_OR_ND_1V8 — AMR1_OR_ND_1V8 (MAKE_BASE=TRUE) — 120, 135, 148
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NAND0_RESET_L — 106

NAND1_RESET_L — NAND1_RESET_L (MAKE_BASE=TRUE) — 108, 112, 134
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NAND1_RESET_L — 110
NAND1_RESET_L — 111

IPD

SMC_I2C5

IN NC_I2C_SMC_SNS1_SCL — NC_I2C_SMC_SNS1_SCL (MAKE_BASE=TRUE) — 10, NO_TEST=1
BI NC_I2C_SMC_SNS1_SDA — NC_I2C_SMC_SNS1_SDA (MAKE_BASE=TRUE) — 10, NO_TEST=1

AP_I2C6

IN I2C_ATCRTMR_SCL (MAKE_BASE=TRUE) — 56, 6
I2C_ATCRTMR_SCL — 71
I2C_ATCRTMR_SCL — 72
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BI I2C_ATCRTMR_SDA (MAKE_BASE=TRUE) — 56, 6
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I2C_ATCRTMR_SDA — 72
I2C_ATCRTMR_SDA — 81

GND — GND (MAKE_BASE=TRUE)

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NC_CHGR_EN_VR1 — NC_CHGR_EN_VR1 (MAKE_BASE=TRUE, NO_TEST=1) — 28

NC_NAND0_OCARINA_WP_L — NC_NAND0_OCARINA_WP_L (MAKE_BASE=TRUE) — 107

NC_CHGR_SMC_RST_L — NC_CHGR_SMC_RST_L (MAKE_BASE=TRUE, NO_TEST=1) — 28
NC_CHGR_CBC_ON — NC_CHGR_CBC_ON (MAKE_BASE=TRUE, NO_TEST=1) — 28

NC_MPMU_AMUX_AY — NC_MPMU_AMUX_AY (MAKE_BASE=TRUE, NO_TEST=1) — 45, 44, 45
NC_SPMU_AMUX_BY — NC_SPMU_AMUX_BY (MAKE_BASE=TRUE, NO_TEST=1) — 45, 40, 45
NC_SPMU_PRE_UVLO — NC_SPMU_PRE_UVLO (MAKE_BASE=TRUE, NO_TEST=1) — 40
NC_MPMU_AMUX_BY — NC_MPMU_AMUX_BY (MAKE_BASE=TRUE, NO_TEST=1) — 45, 44, 45
NC_SPMU_AMUX_AY — NC_SPMU_AMUX_AY (MAKE_BASE=TRUE, NO_TEST=1) — 45, 40, 45
NC_MPMU_LDOX_EN — NC_MPMU_LDOX_EN (MAKE_BASE=TRUE, NO_TEST=1) — 45, 44, 45

NC_NAND1_OCARINA_WP_L — NC_NAND1_OCARINA_WP_L (MAKE_BASE=TRUE, NO_TEST=1) — 112
NC_CIO_ATC3_LSRX_1V2 — NC_CIO_ATC3_LSRX_1V2 (MAKE_BASE=TRUE, NO_TEST=1) — 9
NC_CIO_ATC3_LSTX_1V2 — NC_CIO_ATC3_LSTX_1V2 (MAKE_BASE=TRUE, NO_TEST=1) — 9

NC_MPMU_VDDHI_PRE_UPO — NC_MPMU_VDDHI_PRE_UPO (MAKE_BASE=TRUE, NO_TEST=1) — 44

NC_HDMI_CEC_IRQ — NC_HDMI_CEC_IRQ (MAKE_BASE=TRUE, NO_TEST=1) — 92

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GND_MPMU_QUIET — GND_MPMU_QUIET (MAKE_BASE=TRUE) — 65, 42, 43, 44, 144
GND_SPMU_QUIET — GND_SPMU_QUIET (MAKE_BASE=TRUE) — 65, 38, 39, 40, 144

SPI_TCON_CS_R_L — SPI_TCON_CS_R_L (MAKE_BASE=TRUE) — 6, 13

SE//need check??@!!

NC_SE_SE_GPIO0 — NC_SE_SE_GPIO0 (MAKE_BASE=TRUE) — 26
NC_SE_SE_GPIO1 — NC_SE_SE_GPIO1 (MAKE_BASE=TRUE) — 26
NC_I2C_SE_SE_SCL — NC_I2C_SE_SE_SCL (MAKE_BASE=TRUE) — 26
NC_I2C_SE_SE_SDA — NC_I2C_SE_SE_SDA (MAKE_BASE=TRUE) — 26
NC_I3C_SE_SE_SCL — NC_I3C_SE_SE_SCL (MAKE_BASE=TRUE) — 26
NC_I3C_SE_SE_SDA — NC_I3C_SE_SE_SDA (MAKE_BASE=TRUE) — 26
TP_SE_NFC_GPIO0 — TP_SE_NFC_GPIO0 (MAKE_BASE=TRUE) — 26
TP_SE_NFC_GPIO1 — TP_SE_NFC_GPIO1 (MAKE_BASE=TRUE) — 26
SE_NFC_GPIO3 — SE_NFC_GPIO3 (MAKE_BASE=TRUE) — 26
SE_NFC_GPIO3 — 10
NC_I3C_SE_NFC_SCL — NC_I3C_SE_NFC_SCL (MAKE_BASE=TRUE) — 26
NC_I3C_SE_NFC_SDA — NC_I3C_SE_NFC_SDA (MAKE_BASE=TRUE) — 26

SPMI

SPMI_WLBT_CLK_R — SPMI_WLBT_CLK_R (MAKE_BASE=TRUE) — 10, 13
SPMI_WLBT_DATA_R — SPMI_WLBT_DATA_R (MAKE_BASE=TRUE) — 10, 13
SPMI_SE_CLK_R — SPMI_SE_CLK_R (MAKE_BASE=TRUE) — 10, 13
SPMI_SE_DATA_R — SPMI_SE_DATA_R (MAKE_BASE=TRUE) — 10, 13

NC_SD_PRSNT_L — NC_SD_PRSNT_L (MAKE_BASE=TRUE, NO_TEST=1) — 6

TP_TOUCHID_BKLT_PWM — TP_TOUCHID_BKLT_PWM (MAKE_BASE=TRUE) — 6
IPD_MTP_FUNC_1 — IPD_MTP_FUNC_1 (MAKE_BASE=TRUE) — 136, 6, 130

HDMI Debug I2C

I2C_HDMI_DEBUG_SCL — I2C_HDMI_DEBUG_SCL (MAKE_BASE=TRUE) — 147, 92, 6, 56
I2C_HDMI_DEBUG_SDA — I2C_HDMI_DEBUG_SDA (MAKE_BASE=TRUE) — 147, 92, 6, 56

SWD_NUB_ATCRTMR0_SWDIO (MAKE_BASE=TRUE) — 11
SWD_NUB_ATCRTMR0_SWDIO — 71
SWD_NUB_ATCRTMR0_SWDIO — 72

SWD_NUB_ATCRTMR0_SWCLK (MAKE_BASE=TRUE) — 11
SWD_NUB_ATCRTMR0_SWCLK — 71
SWD_NUB_ATCRTMR0_SWCLK — 72

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SWD_NUB_ATCRTMR1_SWCLK (MAKE_BASE=TRUE) — 11 — SWD_NUB_ATCRTMR1_SWCLK — 81

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ISP GPIO

AOP IO

NC_AOP_I2CM1_SCL	NC_AOP_I2CM1_SCL	MAKE_BASE=TRUE
NC_AOP_I2CM1_SDA	NC_AOP_I2CM1_SDA	MAKE_BASE=TRUE
NC_AOP_I2S0_MCK	NC_AOP_I2S0_MCK	MAKE_BASE=TRUE
NC_AOP_I2S0_LRCK	NC_AOP_I2S0_LRCK	MAKE_BASE=TRUE
NC_AOP_I2S0_DOUT	NC_AOP_I2S0_DOUT	MAKE_BASE=TRUE
NC_AOP_I2S0_DIN	NC_AOP_I2S0_DIN	MAKE_BASE=TRUE
NC_AOP_I2S0_BCLK	NC_AOP_I2S0_BCLK	MAKE_BASE=TRUE

SMC GPIO

MAKE_BASE=TRUE

SOC_DOMAIN_MGPIO_AOP1	SOC_DOMAIN_MGPIO_AOP1	149
NC_SMC_GPIO2	NC_SMC_GPIO2	
NC_SMC_GPIO3	NC_SMC_GPIO3	
NC_SMC_GPIO4	NC_SMC_GPIO4	
NC_SMC_I2CM6_SCL	NC_SMC_I2CM6_SCL	
NC_SMC_I2CM6_SDA	NC_SMC_I2CM6_SDA	

SEP

MAKE_BASE=TRUE

SOC_DOMAIN_SGPIO_GRP1	SOC_DOMAIN_SGPIO_GRP1	149

ENET GPIO

MAKE_BASE=TRUE

NC_ENET_SYNC_1588	NC_ENET_SYNC_1588	

NUB GPIO

MAKE_BASE=TRUE

SOC_DOMAIN_NGPIO_AOP1_0	SOC_DOMAIN_NGPIO_AOP1_0	149

NC_AP_UART3_R2D	NC_AP_UART3_R2D	MAKE_BASE=TRUE
NC_AP_UART3_D2R	NC_AP_UART3_D2R	MAKE_BASE=TRUE
NC_AP_UART3_R2D_RTS_L	NC_AP_UART3_R2D_RTS_L	MAKE_BASE=TRUE
NC_AP_UART3_D2R_CTS_L	NC_AP_UART3_D2R_CTS_L	MAKE_BASE=TRUE
NC_AP_UART4_D2R	NC_AP_UART4_D2R NO_TEST=1	MAKE_BASE=TRUE
NC_AP_UART4_R2D	NC_AP_UART4_R2D NO_TEST=1	MAKE_BASE=TRUE
NC_AP_UART4_R2D_RTS_L	NC_AP_UART4_R2D_RTS_L	MAKE_BASE=TRUE
NC_AP_UART4_D2R_CTS_L	NC_AP_UART4_D2R_CTS_L	MAKE_BASE=TRUE

NAND

SOC_DOMAIN_HGPIO_GRP0_0	SOC_DOMAIN_HGPIO_GRP0_0	MAKE_BASE=TRUE
SOC_DOMAIN_HGPIO_GRP0_1	SOC_DOMAIN_HGPIO_GRP0_1	MAKE_BASE=TRUE

NC SPN's

NC_DISP_TOUCH_BSYNC0	NC_DISP_TOUCH_BSYNC0	MAKE_BASE=TRUE
NC_DISP_TOUCH_BSYNC1	NC_DISP_TOUCH_BSYNC1	MAKE_BASE=TRUE
NC_DISP_TOUCH_EB	NC_DISP_TOUCH_EB	MAKE_BASE=TRUE

NC_SENSOR1_CLK	NC_SENSOR1_CLK	MAKE_BASE=TRUE
NC_SENSOR2_CLK	NC_SENSOR2_CLK	MAKE_BASE=TRUE
NC_SENSOR3_CLK	NC_SENSOR3_CLK	MAKE_BASE=TRUE

ISP SPMI

NC_ISP_I2C1_SCL	NC_ISP_I2C1_SCL	MAKE_BASE=TRUE
NC_ISP_I2C1_SDA	NC_ISP_I2C1_SDA	MAKE_BASE=TRUE

VIPER PWM

NC_P1V8VDDH_DRMOS_PWM6	NC_P1V8VDDH_DRMOS_PWM6	MAKE_BASE=TRUE
NC_P1V8VDDH_DRMOS_PWM7	NC_P1V8VDDH_DRMOS_PWM7	MAKE_BASE=TRUE
NC_P1V8VDDH_DRMOS_PWM8	NC_P1V8VDDH_DRMOS_PWM8	MAKE_BASE=TRUE

D2D IO

NC_A2A_SYNC_ACK	NC_A2A_SYNC_ACK	MAKE_BASE=TRUE
NC_A2A_SYNC_REQ	NC_A2A_SYNC_REQ	MAKE_BASE=TRUE
NC_A2A_WAKEUP	NC_A2A_WAKEUP	MAKE_BASE=TRUE
NC_C2C_CLK_24_IN	NC_C2C_CLK_24_IN	MAKE_BASE=TRUE
NC_C2C_CLK_24_OUT	NC_C2C_CLK_24_OUT	MAKE_BASE=TRUE
NC_C2C_TIME_SYNC_IN	NC_C2C_TIME_SYNC_IN	MAKE_BASE=TRUE
NC_C2C_TIME_SYNC_OUT	NC_C2C_TIME_SYNC_OUT	MAKE_BASE=TRUE
NC_GTRIG_TX_REQ	NC_GTRIG_TX_REQ	MAKE_BASE=TRUE
NC_GTRIG_TX_ACK	NC_GTRIG_TX_ACK	MAKE_BASE=TRUE
NC_GTRIG_TX_LN0	NC_GTRIG_TX_LN0	MAKE_BASE=TRUE
NC_GTRIG_TX_LN1	NC_GTRIG_TX_LN1	MAKE_BASE=TRUE
NC_GTRIG_RX_REQ	NC_GTRIG_RX_REQ	MAKE_BASE=TRUE
NC_GTRIG_RX_ACK	NC_GTRIG_RX_ACK	MAKE_BASE=TRUE
NC_GTRIG_RX_LN0	NC_GTRIG_RX_LN0	MAKE_BASE=TRUE
NC_GTRIG_RX_LN1	NC_GTRIG_RX_LN1	MAKE_BASE=TRUE

NC SPN's

NC_AP_I2S3_MCK	NC_AP_I2S3_MCK	147 MAKE_BASE=TRUE
NC_AP_I2S0_MCK	NC_AP_I2S0_MCK	MAKE_BASE=TRUE
NC_AP_I2S1_MCK	NC_AP_I2S1_MCK	MAKE_BASE=TRUE
NC_AP_GPIO28	NC_AP_GPIO28	MAKE_BASE=TRUE
NC_AP_GPIO29	NC_AP_GPIO29	MAKE_BASE=TRUE
NC_AP_GPIO30	NC_AP_GPIO30	MAKE_BASE=TRUE
NC_AP_GPIO31	NC_AP_GPIO31	MAKE_BASE=TRUE
NC_AP_GPIO32	NC_AP_GPIO32	MAKE_BASE=TRUE
SOC_DOMAIN_GPIO_GRP0	SOC_DOMAIN_GPIO_GRP0	149 MAKE_BASE=TRUE
SOC_DOMAIN_GPIO_GRP1_1	SOC_DOMAIN_GPIO_GRP1_1	149 MAKE_BASE=TRUE
NC_AP_SPI2_SSIN	NC_AP_SPI2_SSIN	MAKE_BASE=TRUE

NC_DISP_POL	NC_DISP_POL	MAKE_BASE=TRUE

SOC GPIO TPs BY DOMAIN

Nonused SOC pins pulled out by functional/power domains

SOC_DOMAIN_GPIO_GRP0 SM P2MM PLACE_SIDE=TOP	PP	PPZZ01
SOC_DOMAIN_GPIO_GRP1_1 SM P2MM PLACE_SIDE=TOP	PP	PPZZ05
SOC_DOMAIN_MGPIO_AOP1 SM P2MM PLACE_SIDE=TOP	PP	PPZZ11
SOC_DOMAIN_NGPIO_AOP1_0 SM P2MM PLACE_SIDE=TOP	PP	PPZZ02
SOC_DOMAIN_HGPIO_GRP0_0 SM P2MM PLACE_SIDE=TOP	PP	PPZZ08
SOC_DOMAIN_HGPIO_GRP0_1 SM P2MM PLACE_SIDE=TOP	PP	PPZZ10
SOC_DOMAIN_SGPIO_GRP1 SM P2MM PLACE_SIDE=TOP	PP	PPZZ12

NC SOC

NC_AP_GPIO6	NC_AP_GPIO6	MAKE_BASE=TRUE
NC_AP_GPIO18	NC_AP_GPIO18	MAKE_BASE=TRUE
NC_AP_GPIO19	NC_AP_GPIO19	MAKE_BASE=TRUE
NC_AP_GPIO20	NC_AP_GPIO20	MAKE_BASE=TRUE
NC_AP_GPIO23	NC_AP_GPIO23	MAKE_BASE=TRUE
NC_AP_GPIO24	NC_AP_GPIO24	MAKE_BASE=TRUE
NC_AP_GPIO25	NC_AP_GPIO25	MAKE_BASE=TRUE
NC_AP_UART0_RTS_L	NC_AP_UART0_RTS_L	MAKE_BASE=TRUE
NC_AP_UART0_CTS_L	NC_AP_UART0_CTS_L	MAKE_BASE=TRUE
NC_AP_UART1_R2D	NC_AP_UART1_R2D	MAKE_BASE=TRUE
NC_AP_UART1_D2R	NC_AP_UART1_D2R	MAKE_BASE=TRUE
NC_AP_UART1_R2D_RTS_L	NC_AP_UART1_R2D_RTS_L	MAKE_BASE=TRUE
NC_AP_UART1_D2R_CTS_L	NC_AP_UART1_D2R_CTS_L	MAKE_BASE=TRUE
NC_AP_UART5_TXD	NC_AP_UART5_TXD	MAKE_BASE=TRUE
NC_AP_UART5_RTS_L	NC_AP_UART5_RTS_L	MAKE_BASE=TRUE
NC_AP_UART5_CTS_L	NC_AP_UART5_CTS_L	MAKE_BASE=TRUE
NC_AP_UART6_RTS_L	NC_AP_UART6_RTS_L	MAKE_BASE=TRUE
NC_AP_UART6_CTS_L	NC_AP_UART6_CTS_L	MAKE_BASE=TRUE

NC_AP_SPI3_MOSI	NC_AP_SPI3_MOSI	MAKE_BASE=TRUE
NC_AP_SPI3_MISO	NC_AP_SPI3_MISO	MAKE_BASE=TRUE
NC_AP_SPI3_SCLK	NC_AP_SPI3_SCLK	MAKE_BASE=TRUE
NC_AP_SPI3_SSIN	NC_AP_SPI3_SSIN	MAKE_BASE=TRUE
NC_AP_SPI5_MOSI	NC_AP_SPI5_MOSI	MAKE_BASE=TRUE
NC_AP_SPI5_MISO	NC_AP_SPI5_MISO	MAKE_BASE=TRUE
NC_AP_SPI5_SCLK	NC_AP_SPI5_SCLK	MAKE_BASE=TRUE
NC_AP_SPI5_SSIN	NC_AP_SPI5_SSIN	MAKE_BASE=TRUE
NC_AP_SGPIO1	NC_AP_SGPIO1	MAKE_BASE=TRUE

NC_AP_SSPI0_MISO	NC_AP_SSPI0_MISO	MAKE_BASE=TRUE
NC_AP_SSPI0_SCLK	NC_AP_SSPI0_SCLK	MAKE_BASE=TRUE
NC_AP_SPMI0_SCLK	NC_AP_SPMI0_SCLK	MAKE_BASE=TRUE
NC_AP_SPMI0_SDATA	NC_AP_SPMI0_SDATA	MAKE_BASE=TRUE
NC_AP_SPMI1_SCLK	NC_AP_SPMI1_SCLK	MAKE_BASE=TRUE
NC_AP_SPMI1_SDATA	NC_AP_SPMI1_SDATA	MAKE_BASE=TRUE
NC_AP_SPMI2_SCLK	NC_AP_SPMI2_SCLK	MAKE_BASE=TRUE
NC_AP_SPMI2_SDATA	NC_AP_SPMI2_SDATA	MAKE_BASE=TRUE
NC_ISP_GPIO_1	NC_ISP_GPIO_1	MAKE_BASE=TRUE
NC_ISP_GPIO_2	NC_ISP_GPIO_2	MAKE_BASE=TRUE
NC_ISP_GPIO_3	NC_ISP_GPIO_3	MAKE_BASE=TRUE
NC_GE_PCIE_TX0P	NC_GE_PCIE_TX0P	MAKE_BASE=TRUE
NC_GE_PCIE_TX0N	NC_GE_PCIE_TX0N	MAKE_BASE=TRUE
NC_GE_PCIE_RX0P	NC_GE_PCIE_RX0P	MAKE_BASE=TRUE
NC_GE_PCIE_RX0N	NC_GE_PCIE_RX0N	MAKE_BASE=TRUE
NC_GE_PCIE_TX1P	NC_GE_PCIE_TX1P	MAKE_BASE=TRUE
NC_GE_PCIE_TX1N	NC_GE_PCIE_TX1N	MAKE_BASE=TRUE
NC_GE_PCIE_RX1P	NC_GE_PCIE_RX1P	MAKE_BASE=TRUE
NC_GE_PCIE_RX1N	NC_GE_PCIE_RX1N	MAKE_BASE=TRUE
NC_GE_PCIE_REF_CLKN	NC_GE_PCIE_REF_CLKN	MAKE_BASE=TRUE
NC_GE_PCIE_REF_CLKP	NC_GE_PCIE_REF_CLKP	MAKE_BASE=TRUE
NC_GE_PCIE_CLKREQ_L	NC_GE_PCIE_CLKREQ_L	MAKE_BASE=TRUE
NC_GE_PCIE_PERST_L	NC_GE_PCIE_PERST_L	MAKE_BASE=TRUE
NC_GE_PCIE_RCALP	NC_GE_PCIE_RCALP	MAKE_BASE=TRUE
NC_GE_PCIE_RCALN	NC_GE_PCIE_RCALN	MAKE_BASE=TRUE
NC_GP_PCIE_TX3_P	NC_GP_PCIE_TX3_P	MAKE_BASE=TRUE
NC_GP_PCIE_TX3_N	NC_GP_PCIE_TX3_N	MAKE_BASE=TRUE
NC_GP_PCIE_RX3_P	NC_GP_PCIE_RX3_P	MAKE_BASE=TRUE
NC_GP_PCIE_RX3_N	NC_GP_PCIE_RX3_N	MAKE_BASE=TRUE
NC_GP_PCIE_REF_CLK3_P	NC_GP_PCIE_REF_CLK3_P	MAKE_BASE=TRUE
NC_GP_PCIE_REF_CLK3_N	NC_GP_PCIE_REF_CLK3_N	MAKE_BASE=TRUE
NC_GP_PCIE_CLKREQ3_L	NC_GP_PCIE_CLKREQ3_L	MAKE_BASE=TRUE
NC_GP_PCIE_PERST3_L	NC_GP_PCIE_PERST3_L	MAKE_BASE=TRUE
NC_GE_PCIE_TX2P	NC_GE_PCIE_TX2P	MAKE_BASE=TRUE
NC_GE_PCIE_TX2N	NC_GE_PCIE_TX2N	MAKE_BASE=TRUE
NC_GE_PCIE_RX2P	NC_GE_PCIE_RX2P	MAKE_BASE=TRUE
NC_GE_PCIE_RX2N	NC_GE_PCIE_RX2N	MAKE_BASE=TRUE
NC_GE_PCIE_TX3P	NC_GE_PCIE_TX3P	MAKE_BASE=TRUE
NC_GE_PCIE_TX3N	NC_GE_PCIE_TX3N	MAKE_BASE=TRUE
NC_GE_PCIE_RX3P	NC_GE_PCIE_RX3P	MAKE_BASE=TRUE
NC_GE_PCIE_RX3N	NC_GE_PCIE_RX3N	MAKE_BASE=TRUE
NC_AOP_FUNC9	NC_AOP_FUNC9	

NC_AOP_FUNC11	NC_AOP_FUNC11	MAKE_BASE=TRUE
NC_AOP_FUNC12	NC_AOP_FUNC12	MAKE_BASE=TRUE
NC_AOP_I2CM2_SCL	NC_AOP_I2CM2_SCL	MAKE_BASE=TRUE
NC_AOP_I2CM2_SDA	NC_AOP_I2CM2_SDA	MAKE_BASE=TRUE
NC_SMC_GPIO5	NC_SMC_GPIO5	MAKE_BASE=TRUE
NC_JTAG_SLV_TCK	NC_JTAG_SLV_TCK	MAKE_BASE=TRUE
NC_JTAG_SLV_TMS	NC_JTAG_SLV_TMS	MAKE_BASE=TRUE
NC_JTAG_SLV_TDI	NC_JTAG_SLV_TDI	MAKE_BASE=TRUE
NC_JTAG_SLV_TDO	NC_JTAG_SLV_TDO	MAKE_BASE=TRUE
NC_JTAG_SLV_TRSTN	NC_JTAG_SLV_TRSTN	MAKE_BASE=TRUE
NC_NUB_SWD_TMS2	NC_NUB_SWD_TMS2	MAKE_BASE=TRUE
NC_NUB_GPIO9	NC_NUB_GPIO9	MAKE_BASE=TRUE
NC_NUB_GPIO10	NC_NUB_GPIO10	MAKE_BASE=TRUE
NC_NUB_GPIO12	NC_NUB_GPIO12	MAKE_BASE=TRUE

SYNC_MASTER=J416_BBABADI_MLB_C_0.27.6 SYNC_DATE=10/26/2021

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VITAMIN C

ATCRTMR0_RESET_1V2_1V8_MCW_L (140) = ATCRTMR0_RESET_1V2_1V8_MCW_L (89, 136) MAKE_BASE=TRUE
ATCRTMR0_RESET_1V2_1V8_MCW_L =

SOC_JTAG_TDO (140) = SOC_JTAG_TDO MAKE_BASE=TRUE
SOC_JTAG_TDO (134, 10) =

SOC_JTAG_TDI (140) = SOC_JTAG_TDI MAKE_BASE=TRUE
SOC_JTAG_TDI (134, 10) =

NC_DC_MUX_SEL (140) = NC_DC_MUX_SEL NO_TEST=1 MAKE_BASE=TRUE

USB0_3V3_LDO_EN_VITC (140) = USB0_3V3_LDO_EN_VITC (135) MAKE_BASE=TRUE
USB0_3V3_LDO_EN_VITC (140) =

I2C CKPLUS WAIVER

I2C_KBD_SCL (135, 131, 129) BI
I2C_KBD_SCL CKPLUS_WAIVE=I2C_PULLUP

I2C_KBD_SDA (135, 131, 128) BI
I2C_KBD_SDA CKPLUS_WAIVE=I2C_PULLUP

USB LEVEL SHIFTER

EUSB_ATC1_DBG_N (77) = EUSB_ATC1_DBG_N MAKE_BASE=TRUE
EUSB_ATC1_DBG_P (77) = EUSB_ATC1_DBG_P MAKE_BASE=TRUE
PD_UPC1_USBP2_RN (77) = PD_UPC1_USBP2_RN MAKE_BASE=TRUE
PD_UPC1_USBP2_RP (77) = PD_UPC1_USBP2_RP MAKE_BASE=TRUE

USB_DBG_LS_P (140) = USB_DBG_LS_P MAKE_BASE=TRUE (74, 135)
USB_DBG_LS_N (140) = USB_DBG_LS_N MAKE_BASE=TRUE (74, 135)

USB_DBG_LS_MUX_P (140) = USB_DBG_LS_MUX_P MAKE_BASE=TRUE
USB_DBG_LS_MUX_P (77) =
USB_DBG_LS_MUX_N (140) = USB_DBG_LS_MUX_N MAKE_BASE=TRUE
USB_DBG_LS_MUX_N (77) =

USB2_ATC0_LS_MUX_P (77) = USB2_ATC0_LS_MUX_P MAKE_BASE=TRUE
USB2_ATC0_LS_MUX_P (140) =
USB2_ATC0_LS_MUX_N (77) = USB2_ATC0_LS_MUX_N MAKE_BASE=TRUE
USB2_ATC0_LS_MUX_N (140) =

USB2_ATC0_LS_P (89) = USB2_ATC0_LS_P MAKE_BASE=TRUE (135)
USB2_ATC0_LS_P (140) =
USB2_ATC0_LS_N (89) = USB2_ATC0_LS_N MAKE_BASE=TRUE (135)
USB2_ATC0_LS_N (140) =

ATC3 NC NETS

DUAL KIS ONLY aliases

TP0500 TP-P5 (TP 1) PD_UPC1_USBP2_RP MAKE_BASE=TRUE = PD_UPC1_USBP2_RP (B1) (73, 77)
TP0501 TP-P5 (TP 1) PD_UPC1_USBP2_RN MAKE_BASE=TRUE = PD_UPC1_USBP2_RN (B1) (73, 77)

EUSB_ATC1_DBG_P (77) MAKE_BASE=TRUE = EUSB_ATC1_DBG_P (B1) (77)
EUSB_ATC1_DBG_N (77) MAKE_BASE=TRUE = EUSB_ATC1_DBG_N (B1) (77)

M1_BUCK2_3_SVSS = M1_BUCK2_3_SVSS MAKE_BASE=TRUE (52)
M1_BUCK0_1_SVSS = M1_BUCK0_1_SVSS MAKE_BASE=TRUE (52)

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Signal Aliases - SGA/CGA Diffs

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SCSET RULES

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_(N)X Calculates dielectric distance from viabug, shortest distance is used unless "L" is defined	EXAMPLE: 1,3-5,7L,9L-10L 2-10
A_DIELECTRIC_(N)XD XV,XVL,X Calculates dielectric distance from hybrid tabs and viabugs, shortest distance is used unless "L" defined	EXAMPLE: 1,3V,5VL,7,9-10 PLEASE USE HYBRID TABLE
A_DIELECTRIC_(N)XIN_(N)XOUT Calculates dielectric distance from viabug, shortest distance is used unless "L" is defined	EXAMPLE: 2,4,6L,8L

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17.2 RULES

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BOM VARIANT TABLES

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SOC/CPU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-28566	1	SOC,RH-S A0+16G,1Y,8C,BIN1,LP,AX,H,B3103	U0600	CRITICAL	SOC:A0_16G
998-28567	1	SOC,RH-S A0+32G,1Y,8C,BIN1,LP,AX,H,B3103	U0600	CRITICAL	SOC:A0_32G
939-12686	1	PCBA, Taipei, X2371	U0600	CRITICAL	SOC:SOCKET

USBC page BOM

Select options as needed.

Multi-protocol Retimer (Lifuka)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-21959	3	IC,RTMR,A0,USB-C RETIMER,FCCSP154	UF000,UF100,UG000	CRITICAL	ATCRTMR:A0
998-25504	3	IC,RTMR,B0,USB-C RETIMER,CSP154	UF000,UF100,UG000	CRITICAL	ATCRTMR:B0
338S00773	3	IC,RTMR,B0,USB-C RETIMER,CSP154	UF000,UF100,UG000	CRITICAL	ATCRTMR:B0_MP
998-27476	3	IC,RTMR,B1,USB-C RETIMER	UF000,UF100,UG000	CRITICAL	ATCRTMR:B1
338S00888	3	C,LIFUKA,B1,USB-C RETIMER,ATK,CSP154	UF000,UF100,UG000	CRITICAL	ATCRTMR:B1_ATK_PROD
338S00889	3	IC,LIFUKA,B1,USB-C RETIMER,SCK,CSP154	UF000,UF100,UG000	CRITICAL	ATCRTMR:B1_SCK_PROD
338S00890	3	IC,LIFUKA,B1,USB-C RETIMER,ASE,CSP154	UF000,UF100,UG000	CRITICAL	ATCRTMR:B1_ASE_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S00889	338S00888		UF000,UF100,UG000	
338S00890	338S00888		UF000,UF100,UG000	

Ace2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02993	3	IC,CD3217,ACE2,B2,USB PWR SW W/HV,BGA123	UF400,UF500,UG400	CRITICAL	

eUSB level shifter

U5500 BOM table on CSA 55

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00914	3	IC,MACAW,CYUSB2402,A2,CSP24	UF600,UF650,UG650	CRITICAL	

Re-timer Sequencer

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00530	2	IC,SLG4AP44593,PWR RAIL SEQUENCER,QFN8	UF790,UG790	CRITICAL	

Re-timer ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-22993	3	IC,FLASH,64MBIT,1.2V,QE=1,W,4X4MM,SON8	UF090,UF190,UG090	CRITICAL	ATCRTMR_ROM:WINBOND
998-22994	3	IC,FLASH,64MBIT,1.2V,QE=1,W,4X4MM,SON8	UF090,UF190,UG090	CRITICAL	ATCRTMR_ROM:MACRONIX
335S00574	3	IC,FLASH,64MBIT,1.2V,QE=1,W,4X4MM,SON8	UF090,UF190,UG090	CRITICAL	ATCRTMR_ROM:WINDBOND_MP

Programmble parts: ACE ROMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
341S02220	1	ROM,ACE-P0 (V.3.020.0.7) DVT,X2293	UF260	CRITICAL		<-LEFT
341S02221	1	ROM,ACE-P1 (V.3.020.0.7) DVT,X2293	UF250	CRITICAL		<-LEFT
341S02222	1	ROM,ACE-P2 (V.3.020.0.7) DVT,X2293	UG260	CRITICAL		<-RIGHT
341S02223	1	ROM,ACE-P5 (V.3.020.0.1) DVT,X2293	U5660	CRITICAL		<-MAGSAFE

HDMI CONNECTOR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514S00359	1	CONN,RCPT,HDMI,X2094	JH500	CRITICAL	

SD CARD CONNECTOR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-00180	1	CONN,RCPT,SD,X2094	JK600	CRITICAL	

OCARINA0

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00600	1	IC,PMU,OCARINA,D2499A0,OPT-BC,WLCSP56	UN400	CRITICAL	OCARINA0:A0_OTPBC

OCARINA1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00600	1	IC,PMU,OCARINA,D2499A0,OPT-BC,WLCSP56	UN900	CRITICAL	OCARINA1:A0_OTPBC

SECURE ELEMENT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00877	1	IC,EOS,SN300V,B1,DEV,Y50,WLCSP79	U5000	CRITICAL	EOS:B1_DEV

NAND PARTS

	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
512GB	335S00552	2	NAND,BC5T,256GB,S5E,XX.X,512G,K,ULGA315	UN000,UN100	CRITICAL	NAND:TS-512
	335S00581	2	NAND,3DV7T,256GB,S5E,XX.X,512G,H,ULGA315	UN000,UN100	CRITICAL	NAND:HY-512
1TB	335S00552	4	NAND,BC5T,256GB,S5E,XX.X,512G,K,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:TS-1TB
	335S00581	4	NAND,3DV7T,256GB,S5E,XX.X,512G,H,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:HY-1TB
	335S00620	4	NAND,BC5T,256GB,S5E,11.0,512G,W,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:WD-1TB
2TB	335S00553	4	NAND,BC5T,512GB,S5E,XX.X,512G,K,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:TS-2TB
	335S00583	4	NAND,3DV7T,512GB,S5E,XX.X,512G,H,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:HY-2TB
4TB	335S00553	4	NAND,BC5T,512GB,S5E,XX.X,512G,K,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:TS-4TB
	335S00553	4	NAND,BC5T,512GB,S5E,XX.X,512G,K,ULGA315	UN500,UN600,UN700,UN800	CRITICAL	NAND:TS-4TB
	335S00550	4	NAND,BC5T,512GB,S5E,XX.X,512G,W,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:WD-4TB
	335S00550	4	NAND,BC5T,512GB,S5E,XX.X,512G,W,ULGA315	UN500,UN600,UN700,UN800	CRITICAL	NAND:WD-4TB
8TB	335S00561	4	NAND,BC5T,1TB,S5E,XX.X,512G,K,MLGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:TS-8TB
	335S00561	4	NAND,BC5T,1TB,S5E,XX.X,512G,K,MLGA315	UN500,UN600,UN700,UN800	CRITICAL	NAND:TS-8TB
	335S00584	4	NAND,3DV7T,1TB,S5E,XX.X,512G,H,MLGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:HY-8TB
	335S00584	4	NAND,3DV7T,1TB,S5E,XX.X,512G,H,MLGA315	UN500,UN600,UN700,UN800	CRITICAL	NAND:HY-8TB
	335S00567	4	NAND,BC5ST,1TB,S5E,XX.X,512G,W,LGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:WD-8TB
	335S00567	4	NAND,Bc5ST,1TB,S5E,XX.X,512G,W,LGA315	UN500,UN600,UN700,UN800	CRITICAL	NAND:WD-8TB

NAND SOCKET

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
939-11766	4	PCBA,MANAS,X2371	UN000	CRITICAL	NAND:SOCKET
939-11766	4	PCBA,MANAS,X2371	UN500	CRITICAL	NAND:SOCKET

SOC A0 Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-28570	998-28566	ANY	ALL	A0 16G BIN2 ALT HY
998-28571	998-28567	ANY	ALL	A0 32G BIN2 ALT HY
998-28568	998-28566	ANY	ALL	A0 16G BIN1 ALT MI
998-28569	998-28567	ANY	ALL	A0 32G BIN1 ALT MI
998-28572	998-28566	ANY	ALL	A0 16G BIN2 ALT MI
998-28573	998-28567	ANY	ALL	A0 32G BIN2 ALT MI

Bin3: 30FSTP

Bin1: 38FSTP

ICEMAN
---> CSA 57

VIPER
---> CSA 93

MONACO
---> CSA 101,102,103,104,105

HDMI ROM
---> CSA 178

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BOM OPTION TABLES

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MLB Common/Dev BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00476	1	COMMON PARTS,MLB-S,X2527	BASE	CRITICAL	BOM_BASE
985-01782	1	DEV PARTS,MLB-S,X2527	DEVEL	CRITICAL	BOM_DEV

MLB Common/Dev BOM Definitions

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00476	COMMON PARTS,MLB-S,X2527	MLB_COMMON
985-01782	DEV PARTS,MLB-S,2527	MLB_DEVEL:ENG

MLB Common BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	SCH,PCB,COMMON,ALTERNATE,MLB_COMMON1,MLB_COMMON2,MLB_COMMON3,MLB_PROGPARTS,MLB_MAGSAFE
MLB_COMMON1	BOARD_ID:0x06,BOARD_REV:2,MLB_USBC,MLB_HDMI,MLB_PWR,MLB_BLC,BOOTCFG2
MLB_COMMON2	RF_CONN,EOS:B1_DEV,DRAMRST:PMUIO
MLB_COMMON3	P5VS2_DSCHG,P5VUSB_DSCHG,VDD1SW:1777,REFIMU_IC:BMI286
MLB_PROGPARTS	HDMI_ROM:PREP,ATCRTMR_ROM:WINDBOND_MP
MLB_USBC	MAGSAFE_EXTRD_DEL,ATCRTMR:B1_ATK_PROD,ACE_WILL_BE_OTPED:YES,LFKA_TEST_MODE:YES,USBC_DUAL_KIS:YES,MACAW_I2C_MASK
MLB_HDMI	DATA_FILT,HDMI_CLC_FILT:YES,HDMI_SPF_AND:STUFF,COBRAPART:1
MLB_BLC	BLC_BEN_IC:V4,BLC_5V_SERIES:10_OHM,BLC_5V_CAP:4P7_UF
MLB_MAGSAFE	MAGSAFE_UV:YES,MAGSAFE_GDC,3V8_DLY:YES
MLB_PWR	P3V8AON_IC:A2_R170,P3V8AON_LPM,MLB_PWR2,WHAMOLA_UVLO,P3V8ILIM:BOM1_5V,PMU32K:OSC_QRTZ
MLB_PWR2	PBUS:3S,MVK_OTP:FJ,LDO_HDMI:5V,WHAMOLA:1A,5VS2TPS_VOUT:5V232,MLB_PWR3
MLB_PWR3	CONTROLLER:AUSTRINGER,EKARA:A1,AUSTRINGER:A1_0_3PH_SPM

Dev BOM Groups

BOM GROUP	BOM OPTIONS
MLB_DEVEL:ENG	USBC_DBG,DBG_BTN,DBG_LED,VITAMIN-C:YES,DBG:FAN,SNSRES_DEV,DEV_IPD,BATT_DBG

Board Revs

* Tentative Board Rev

BOM GROUP	BOM OPTIONS	Build
BOARD_REV:0	BOARDREV3,BOARDREV2,BOARDREV1,BOARDREV0	P1bu
BOARD_REV:1	BOARDREV3,BOARDREV2,BOARDREV1	P1bu
BOARD_REV:2	BOARDREV3,BOARDREV2,BOARDREV0	P1bu
BOARD_REV:3	BOARDREV3,BOARDREV2	P1bu
BOARD_REV:4	BOARDREV3,BOARDREV1,BOARDREV0	P1a
BOARD_REV:5	BOARDREV3,BOARDREV1	P1a
BOARD_REV:6	BOARDREV3,BOARDREV0	P1a
BOARD_REV:7	BOARDREV3	P1b
BOARD_REV:8	BOARDREV2,BOARDREV1,BOARDREV0	P1b

Board ID

MLB_C Board ID is 0x0A (rdar://74602645)

BOM GROUP	BOM OPTIONS
BOARD_ID:0x06	BOARDID2,BOARDID1
BOARD_ID:0x3F	BOARDID5,BOARDID4,BOARDID3,BOARDID2,BOARDID1,BOARDID0

**** No More 5 Landings. UPDATE

SSD Config Table

Controls NAND ICs and SSD support BOMs

BOM GROUP	Landings	BOM OPTIONS
SSD:TS-512	2	NAND:TS-512,OCARINA0:A0_OTPBC,BOM_SSD:2L
SSD:HY-512	2	NAND:HY-512,OCARINA0:A0_OTPBC,BOM_SSD:2L
SSD:TS-1TB	4	NAND:TS-1TB,OCARINA0:A0_OTPBC,BOM_SSD:4L
SSD:WD-1TB	4	NAND:WD-1TB,OCARINA0:A0_OTPBC,BOM_SSD:4L
SSD:HY-1TB	4	NAND:HY-1TB,OCARINA0:A0_OTPBC,BOM_SSD:4L
SSD:TS-2TB	4	NAND:TS-2TB,OCARINA0:A0_OTPBC,BOM_SSD:4L
SSD:HY-2TB	4	NAND:HY-2TB,OCARINA0:A0_OTPBC,BOM_SSD:4L
SSD:TS-4TB	8	NAND:TS-4TB,OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:8L
SSD:WD-4TB	8	NAND:WD-4TB,OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:8L
SSD:TS-8TB	8	NAND:TS-8TB,OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:8L
SSD:HY-8TB	8	NAND:HY-8TB,OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:8L
SSD:WD-8TB	8	NAND:WD-8TB,OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:8L
SSD:NOS5E	0	OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC
SSD:8L-DCDC	8	OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:8L

Parts to support Landings 0-4 are in common BOM

SSD Support BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00496	1	SSD PARTS,L1-L2,MLB-S,X2527	SSD	CRITICAL	BOM_SSD:2L
685-00487	1	SSD PARTS,L1-L4,MLB-S,X2527	SSD	CRITICAL	BOM_SSD:4L
685-00488	1	SSD PARTS,L5-L8,MLB-S,X2527	SSD	CRITICAL	BOM_SSD:8L

SSD Support BOM Definitions

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00496	SSD PARTS,L1-L2,MLB-S,X2527	ALTERNATE,SSD_SUPPORT:L2
685-00487	SSD PARTS,L1-L4,MLB-S,X2527	ALTERNATE,SSD_SUPPORT:L4
685-00488	SSD PARTS,L5-L8,MLB-S,X2527	ALTERNATE,SSD_SUPPORT:L8

SSD Support BOM Groups

BOM GROUP	Host BOM	BOM OPTIONS
SSD_SUPPORT:L2		SSD_2L
SSD_SUPPORT:L4	Common BOM	SSD_2L,SSD_4L
SSD_SUPPORT:L8	8L Support BOM	SSD_OC1VR1,SSD_2L,SSD_4L,SSD_8L

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BOM GROUPS

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BOM VARIANT TABLES

SoC 16GB, FSTP-19

BOM NUMBER	BOM NAME	BOM OPTIONS
639-16829	PCBA,MLB-S,8C,16GB,FSTP-19,TS-512,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_16G,SSD:TS-512
639-16946	PCBA,MLB-S,8C,16GB,FSTP-19,TS-1TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_16G,SSD:TS-1TB
639-16974	PCBA,MLB-S,8C,16GB,FSTP-19,TS-2TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_16G,SSD:TS-2TB
639-16948	PCBA,MLB-S,8C,16GB,FSTP-19,TS-4TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_16G,SSD:TS-4TB
639-16950	PCBA,MLB-S,8C,16GB,FSTP-19,TS-8TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_16G,SSD:TS-8TB
639-16976	PCBA,MLB-S,8C,16GB,FSTP-19,HY-512,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_16G,SSD:HY-512
639-16978	PCBA,MLB-S,8C,16GB,FSTP-19,HY-1TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_16G,SSD:HY-1TB
639-16980	PCBA,MLB-S,8C,16GB,FSTP-19,HY-2TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_16G,SSD:HY-2TB
639-16982	PCBA,MLB-S,8C,16GB,FSTP-19,HY-8TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_16G,SSD:HY-8TB
639-16984	PCBA,MLB-S,8C,16GB,FSTP-19,WD-1TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_16G,SSD:WD-1TB
639-16986	PCBA,MLB-S,8C,16GB,FSTP-19,WD-4TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_16G,SSD:WD-4TB
639-16988	PCBA,MLB-S,8C,16GB,FSTP-19,WD-8TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_16G,SSD:WD-8TB

SoC 32GB, FSTP-19

BOM NUMBER	BOM NAME	BOM OPTIONS
639-16717	PCBA,MLB-S,8C,32GB,FSTP-19,TS-512,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:TS-512
639-16947	PCBA,MLB-S,8C,32GB,FSTP-19,TS-1TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:TS-1TB
639-16975	PCBA,MLB-S,8C,32GB,FSTP-19,TS-2TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:TS-2TB
639-16949	PCBA,MLB-S,8C,32GB,FSTP-19,TS-4TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:TS-4TB
639-16951	PCBA,MLB-S,8C,32GB,FSTP-19,TS-8TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:TS-8TB
639-16977	PCBA,MLB-S,8C,32GB,FSTP-19,HY-512,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:HY-512
639-16979	PCBA,MLB-S,8C,32GB,FSTP-19,HY-1TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:HY-1TB
639-16981	PCBA,MLB-S,8C,32GB,FSTP-19,HY-2TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:HY-2TB
639-16983	PCBA,MLB-S,8C,32GB,FSTP-19,HY-8TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:HY-8TB
639-16985	PCBA,MLB-S,8C,32GB,FSTP-19,WD-1TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:WD-1TB
639-16987	PCBA,MLB-S,8C,32GB,FSTP-19,WD-4TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:WD-4TB
639-16989	PCBA,MLB-S,8C,32GB,FSTP-19,WD-8TB,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SOC:A0_32G,SSD:WD-8TB

DEV Boms

BOM NUMBER	BOM NAME	BOM OPTIONS
939-13339	PCBA,MLB-S,DCDC-1,X2527	BOM_BASE,BOM_DEV,ALTERNATE,SSD:NOSSE,SOC:SOCKET
939-13340	PCBA,MLB-S,DCDC-2,X2527	BOM_BASE,BOM_DEV,SSD:8L-DCDC,NAND:SOCKET

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BOM VARIANT TABLES

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S00015	107S00011	ANY	ALL	<RDAR://68783373>
107S00041	107S00039	ANY	ALL	<RDAR://64239409>
107S00056	107S00096	ANY	ALL	<RDAR://82700303>
107S00057	107S00100	ANY	ALL	<RDAR://64239601>
107S00076	107S00044	ANY	ALL	<RDAR://64238938>
107S00101	107S00005	ANY	ALL	<RDAR://68782630>
107S00102	107S00017	ANY	ALL	<RDAR://64239315>
107S00103	107S00058	ANY	ALL	<RDAR://64241086>
107S00104	107S00061	ANY	ALL	<RDAR://64241122>
107S00105	107S00062	ANY	ALL	<RDAR://64241228>
107S00234	107S00235	ANY	ALL	<RDAR://64240586>
107S00297	107S00344	ANY	ALL	<RDAR://64239077>
107S00298	107S00460	ANY	ALL	<RDAR://68783859>
107S00365	107S00373	ANY	ALL	<RDAR://85945300>
107S00391	107S00392	ANY	ALL	<RDAR://68783810>
107S00479	107S00478	ANY	ALL	<RDAR://83333047>
107S00491	107S00061	ANY	ALL	<RDAR://82693685>
107S00491	107S00104	ANY	ALL	<RDAR://82693685>
107S00493	107S00096	ANY	ALL	<RDAR://82700303>
107S00494	107S00058	ANY	ALL	<RDAR://82840871>
107S00494	107S00103	ANY	ALL	<RDAR://82840871>
107S0150	107S00460	ANY	ALL	<RDAR://68783859>
107S0240	107S0255	ANY	ALL	<RDAR://69891889>
107S0276	107S00020	ANY	ALL	<RDAR://57126636>
128S00039	128S00038	ANY	ALL	<RDAR://56380033>
128S00058	128S00098	ANY	ALL	<RDAR://71999316>
128S00069	128S00067	ANY	ALL	<RDAR://65153232>
128S00069	128S00094	ANY	ALL	<RDAR://68779373>
128S00093	128S00009	ANY	ALL	<RDAR://68780181>
128S00094	128S00067	ANY	ALL	<RDAR://68779373>
128S00103	128S00009	ANY	ALL	<RDAR://68780181>
128S00103	128S00093	ANY	ALL	<RDAR://73509196>
128S00105	128S00098	ANY	ALL	<RDAR://71999316>
128S00119	128S00016	ANY	ALL	<RDAR://68780181>
128S0302	128S00038	ANY	ALL	<RDAR://56380033>
128S0445	128S0436	ANY	ALL	<RDAR://68808630>
131S00213	131S0556	ANY	ALL	<RDAR://82687224>
132S00064	132S0409	ANY	ALL	<RDAR://69816432>
132S00176	132S0640	ANY	ALL	<RDAR://65054797>
132S0409	132S00064	ANY	ALL	<RDAR://69816432>
138S00022	138S00020	ANY	ALL	<RDAR://86546888>
138S00047	138S00073	ANY	ALL	<RDAR://56380033>
138S00049	138S0831	ANY	ALL	<RDAR://86546538>
138S00087	138S1086	ANY	ALL	<RDAR://69510573>
138S00097	138S0750	ANY	ALL	<RDAR://65198710>
138S00104	138S0978	ANY	ALL	<RDAR://65054584>
138S00139	138S00138	ANY	ALL	<RDAR://64426076>
138S00148	138S00149	ANY	ALL	<RDAR://82688006>
138S00150	138S00149	ANY	ALL	<RDAR://82688006>
138S00151	138S00149	ANY	ALL	<RDAR://82688006>
138S00164	138S00138	ANY	ALL	<RDAR://64426076>
138S00167	138S00237	ANY	ALL	<RDAR://86547518>
138S00181	138S0835	ANY	ALL	<RDAR://57161300>

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00229	138S00107	ANY	ALL	<RDAR://64381231>
138S00280	138S00138	ANY	ALL	<RDAR://64426076>
138S00284	138S00136	ANY	ALL	<RDAR://57134599>
138S00291	138S0835	ANY	ALL	<RDAR://57161300>
138S00330	138S00081	ANY	ALL	<RDAR://64425893>
138S00332	138S00328	ANY	ALL	<RDAR://57328643>
138S00343	138S00329	ANY	ALL	<RDAR://64426266>
138S00364	138S00290	ANY	ALL	<RDAR://64910444>
138S00385	138S00377	ANY	ALL	<RDAR://73670288>
138S00396	138S00392	ANY	ALL	<RDAR://71453199>
138S00397	138S00035	ANY	ALL	<RDAR://83120865>
138S00416	138S00328	ANY	ALL	<RDAR://82683126>
138S00416	138S00332	ANY	ALL	<RDAR://82683126>
138S00437	138S00392	ANY	ALL	<RDAR://83121201>
138S00437	138S00396	ANY	ALL	<RDAR://83121201>
138S0734	138S0838	ANY	ALL	<RDAR://86548925>
138S0746	138S0705	ANY	ALL	<RDAR://65194259>
138S0772	138S00013	ANY	ALL	<RDAR://69408404>
138S0786	138S0705	ANY	ALL	<RDAR://65194259>
138S0789	138S0941	ANY	ALL	<RDAR://56380033>
138S0852	138S0818	ANY	ALL	<RDAR://57137990>
138S1068	138S00215	ANY	ALL	<RDAR://64909886>
138S1103	138S0719	ANY	ALL	<RDAR://65199121>
152S00182	152S00703	ANY	ALL	<RDAR://64435747>
152S00708	152S00265	ANY	ALL	<RDAR://56380033>
152S00700	152S00285	ANY	ALL	<RDAR://68780181>
152S00785	152S00477	ANY	ALL	<RDAR://69846739>
152S00801	152S00695	ANY	ALL	<RDAR://64386631>
152S00812	152S1701	ANY	ALL	<RDAR://55465318>
152S00841	152S00238	ANY	ALL	<RDAR://64476987>
152S00963	152S00885	ANY	ALL	<RDAR://56380033>
152S01023	152S00384	ANY	ALL	<RDAR://64458983>
152S01024	152S00386	ANY	ALL	NA
152S01037	152S00887	ANY	ALL	<RDAR://65152741>
152S01070	152S00887	ANY	ALL	<RDAR://65152741>
152S01344	152S00883	ANY	ALL	<RDAR://64434865>
152S01410	152S01300	ANY	ALL	<RDAR://64173241>
152S01415	152S01280	ANY	ALL	<RDAR://64722980>
152S01451	152S00883	ANY	ALL	<RDAR://64434865>
155S00018	155S0664	ANY	ALL	<RDAR://68810276>
155S00155	155S0441	ANY	ALL	<RDAR://65043740>
155S00309	155S0831	ANY	ALL	<RDAR://65054290>
155S00648	155S00647	ANY	ALL	<RDAR://68810066>
155S0275	155S00188	ANY	ALL	<RDAR://68809979>
155S0660	155S0513	ANY	ALL	<RDAR://68810203>
155S0823	155S0644	ANY	ALL	<RDAR://65045206>
197S00046	197S00036	ANY	ALL	<RDAR://57229594>
197S00047	197S00036	ANY	ALL	<RDAR://57229594>
197S00048	197S00036	ANY	ALL	<RDAR://57229594>
197S00318	197S00323	ANY	ALL	<RDAR://73373069>
197S00335	197S00323	ANY	ALL	<RDAR://83334197>
197S0588	197S0591	ANY	ALL	<RDAR://78480268>
197S0590	197S0588	ANY	ALL	<RDAR://65008354>
197S0590	197S0591	ANY	ALL	<RDAR://65008354>

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0591	197S0588	ANY	ALL	<RDAR://65008354>
311S00392	311S00129	ANY	ALL	<RDAR://57167823>
311S00267	311S00244	ANY	ALL	<RDAR://63954013>
311S00268	311S00246	ANY	ALL	<RDAR://64048026>
311S00271	311S00286	ANY	ALL	<RDAR://83503679>
311S00279	311S00285	ANY	ALL	<RDAR://68811697>
311S00310	311S00306	ANY	ALL	<RDAR://69815666>
311S00312	311S0278	ANY	ALL	<RDAR://78128916>
311S00322	311S00321	ANY	ALL	<RDAR://82699167>
311S00335	311S00155	ANY	ALL	<RDAR://83334823>
335S00575	335S00574	ANY	ALL	<RDAR://82686273>
353S00878	353S00599	ANY	ALL	<RDAR://57173083>
353S01792	353S3901	ANY	ALL	<RDAR://73727836>
353S02175	353S00882	ANY	ALL	<RDAR://68820393>
353S02402	353S1429	ANY	ALL	<RDAR://73727544>
353S02407	353S02212	ANY	ALL	<RDAR://63861706>
353S02434	353S3332	ANY	ALL	<RDAR://68820512>
353S02624	353S01595	ANY	ALL	<RDAR://73592667>
353S02787	353S01211	ANY	ALL	<RDAR://85945088>
353S02789	353S3021	ANY	ALL	<RDAR://73885143>
353S02897	353S02402	ANY	ALL	<RADR://83122707>
353S02897	353S1429	ANY	ALL	<RDAR://83122707>
371S00085	371S00325	ANY	ALL	<RDAR://64913914>
371S00217	371S00079	ANY	ALL	<RDAR://55465318>
371S00220	371S00307	ANY	ALL	<RDAR://73728616>
371S00302	371S00241	ANY	ALL	<RDAR://69526283>
371S00306	371S00305	ANY	ALL	<RDAR://73728520>
371S00311	371S00312	ANY	ALL	<RDAR://68821167>
371S00322	371S00047	ANY	ALL	<RDAR://74200997>
371S00328	371S00310	ANY	ALL	<RDAR://73627030>
371S0602	371S00245	ANY	ALL	<RDAR://69900570>
371S0730	371S00172	ANY	ALL	<RDAR://73629317>
372S00040	372S00039	ANY	ALL	<RDAR://68821275>
372S0082	372S00023	ANY	ALL	<RDAR://65196180>
376S00001	376S0659	ANY	ALL	<RDAR://68821306>
376S00021	376S00263	ANY	ALL	<RDAR://85086426>
376S00036	376S00328	ANY	ALL	<RDAR://74352845>
376S00086	376S0761	ANY	ALL	<RDAR://71998792>
376S00292	376S00294	ANY	ALL	<RDAR://73731835>
376S00303	376S00012	ANY	ALL	<RDAR://56380033>
376S00321	376S00397	ANY	ALL	<RDAR://74354869>
376S00466	376S00463	ANY	ALL	<RDAR://64047597>
376S00485	376S00455	ANY	ALL	<RDAR://74654584>
376S00514	376S00510	ANY	ALL	<RDAR://73954493>
376S00544	376S1112	ANY	ALL	<RDAR://78593594>
376S0636	376S1004	ANY	ALL	<RDAR://64910759>
377S00165	377S00031	ANY	ALL	<RDAR://64912300>
377S00166	377S00160	ANY	ALL	<RDAR://64047091>
377S00186	377S00060	ANY	ALL	<RDAR://68822222>
377S00210	377S00172	ANY	ALL	<RDAR://64899432>
377S0155	377S0184	ANY	ALL	<RDAR://57230484>

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
740S00081	740S00053	ANY	ALL	<RDAR://69166742>
740S0118	740S00028	ANY	ALL	<RDAR://64196448>
377S00196	377S00185	ANY	ALL	RADAR://86546159
371S0602	371S00245	ANY	ALL	
376S00469	376S0761	ANY	ALL	RADAR://89575424
376S00600	376S0761	ANY	ALL	RADAR://89575424
376S00328	376S00263	ANY	ALL	RADAR://
353S4160	353S01615	ANY	UT000	RADAR://
353S02787	353S01211	ANY	ALL	RADAR://85945135
353S03028	353S01211	ANY	ALL	RADAR://85945135
107S00373	107S00365	ANY	ALL	RADAR://85945438
107S0255	107S0240	ANY	ALL	RADAR://85945575
116S00044	116S00014	ANY	ALL	RADAR://88050687
117S00040	117S00012	ANY	ALL	RADAR://88244101
131S00691	131S00365	ANY	ALL	RADAR://88198474
155S00754	155S00098	ANY	ALL	RADAR://88051361
311S00304	311S00301	ANY	ALL	RADAR://88052235
353S00636	353S4037	ANY	ALL	rdar://87798238
371S00370	371S00062	ANY	ALL	rdar://88047546
377S00223	377S00040	ANY	ALL	rdar://88510972
377S00240	377S00201	ANY	ALL	rdar://88511711
376S00469	376S0761	ANY	ALL	rdar://89575424
376S00600	376S0761	ANY	ALL	rdar://89575424
338S00888	998-27476	ANY	ALL	rdar://90338289
338S00889	998-27476	ANY	ALL	rdar://90338289
338S00890	998-27476	ANY	ALL	rdar://90338289
107S00055	107S00090	ANY	R5820,R5840	
376S1147	376S00281	ANY	Q5820,Q5840	
152S00367	152S01248	ANY	L5820,L5840	
152S01452	152S01248	ANY	L5820,L5840	
376S0855	376S00078	ANY	ALL	rdar://
376S00002	376S00078	ANY	ALL	rdar://
376S00588	376S00078	ANY	ALL	rdar://
376S0855	376S00074	ANY	ALL	rdar://
376S00002	376S00074	ANY	ALL	rdar://
376S00078	376S00074	ANY	ALL	rdar://
376S00588	376S00074	ANY	ALL	rdar://
376S00332	376S00074	ANY	ALL	rdar://
376S00224	376S1128	ANY	ALL	rdar://93994092
376S00282	376S1128	ANY	ALL	rdar://93994092
376S00292	376S1140	ANY	ALL	rdar://93993732
376S00294	376S1140	ANY	ALL	rdar://93993732
376S00224	376S00282	ANY	ALL	rdar://93994092
376S1128	376S00282	ANY	ALL	rdar://93994092

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REF_CLVR_MIRABEAU

PACK_OPTIONS TO INCLUDE IN NETLIST

REF_VR_ICEMAN

PACK_OPTIONS TO INCLUDE IN NETLIST
P3V8ILIM_MUX:Y
3V8_AON_PBUS-B12
3V8_AON_I2C-POR
3V8_INDUCTOR:2P4MM
3V8_AON_MLCC-STD
3V8_AON_LG_R:YES
3V8_AON_CTRL_PKG:QFN_THICKSTENCIL

REF_VR_AUSTRINGER

PACK_OPTIONS TO INCLUDE IN NETLIST
VDDH_DBG
VDDH_L3MM
VDDH_C9543
VDDH_B12
VDDH_PORTABLE_CAPS
VDDH_3PH

REF_VR_5V_TPS62130

PACK_OPTIONS TO INCLUDE IN NETLIST
5VS2TPS_PBUS-B12

REF_USBC_ACE2

PACK_OPTIONS TO INCLUDE IN NETLIST
USBC_LAPTOP
USBC_DEBUG_UPC0
PKGS:BGA
USBC_LAPTOP_CC_PRT
KEEP_SMALL_ARKANOID_CONN
ACE2_SS_CAP
ACTIVE_READY:LARGE_PITCH
DUAL_KIS:YES
FLIPPED
ATC_VR_PG-RES
ATC_VR_DSCHG-EN-R:YES
ATC_VR_MLCC-DSCHG
ATC01_VR_MLCC-REGULAR
ATC2_VR_MLCC-REGULAR

REF_VR_5V_LT8642

PACK_OPTIONS TO INCLUDE IN NETLIST
5VUSBC01_PBUS-B12
5VUSBC01_THICKSTNCL
5VUSBC01_AND:PP

REF_STORAGE_S5E

PACK_OPTIONS TO INCLUDE IN NETLIST
2V5_NAND_PBUS-B12-16V

REF_SECDIS_SAK

PACK_OPTIONS TO INCLUDE IN NETLIST
PROD_SECDIS_NOTMIPI

REF_SPKRAMP_SN012776

PACK_OPTIONS TO INCLUDE IN NETLIST
SPKRAMP_A
SPKRAMP_B
SPKRAMP_C
SPKRAMP_D
SPKRAMP_E
SPKRAMP_F
SPKRAMP_ICC_GB

REF_IMU_SOVEREIGN

PACK_OPTIONS TO INCLUDE IN NETLIST
REFIMU_VDD:LCFILT
REFIMU_TEST:YES

REF_WIRELESS

PACK_OPTIONS TO INCLUDE IN NETLIST
WLBT_PCIE_TP_RHODES
3X_ANTENNA
SUNWAY
WLBT_D2R_CAP_STATEN_RHODES

REF_PMIC_MAVERICKS_H14

PACK_OPTIONS TO INCLUDE IN NETLIST
SPMU_LDO3
MPMU_LDO4
SPMU_SW1
PMUOTP:GND
PMU_DISP2:N
PMU32K:OSC_QRTZ
PMU_BBAT:N

REF_HDMI_COBRA

PACK_OPTIONS TO INCLUDE IN NETLIST
HDMICONN:PORT
HDMI14UF:THICK

PACK_OPTIONS TO INCLUDE IN NETLIST
PKGS:TOUCH_LARGER_PITCH
5VS2TPS_THICKSTNCL
SDCARD
SD_VR_3V3:THICKSTNCL
5VUSBC23_PBUS-B12
POLY_PBUS:16V
RF_CONN
LPDPRX_RCAL

PACK_OPTIONS TO INCLUDE IN NETLIST
VITAMINC
3V8_DELAY:YES

SYNC_DATE=

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PACK OPTIONS

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