8	7	6	5	4	3	2	1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
C	0000734528	PRODUCTION RELEASED	2009-06-04

K24 MLB SCHEMATIC

6/12/2009

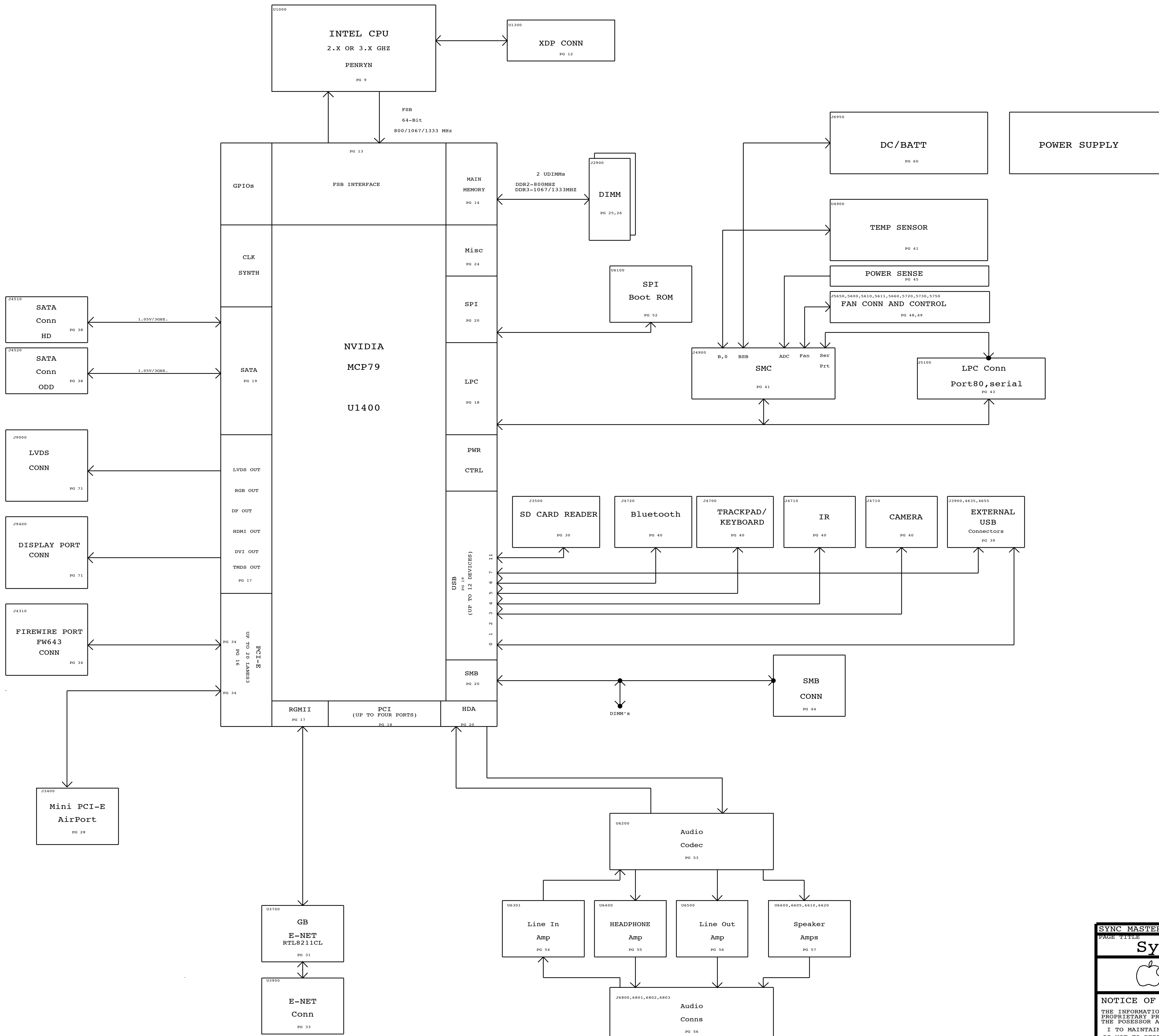
Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7898	1	SCHEM,MLB,K24	SCH	CRITICAL	
820-2530	1	PCBF,MLB,K24	PCB	CRITICAL	

DRAWING TITLE
SCHEM,MLB,K24

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH



SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

PAGE TITLE

System Block Diagram

Apple Inc.

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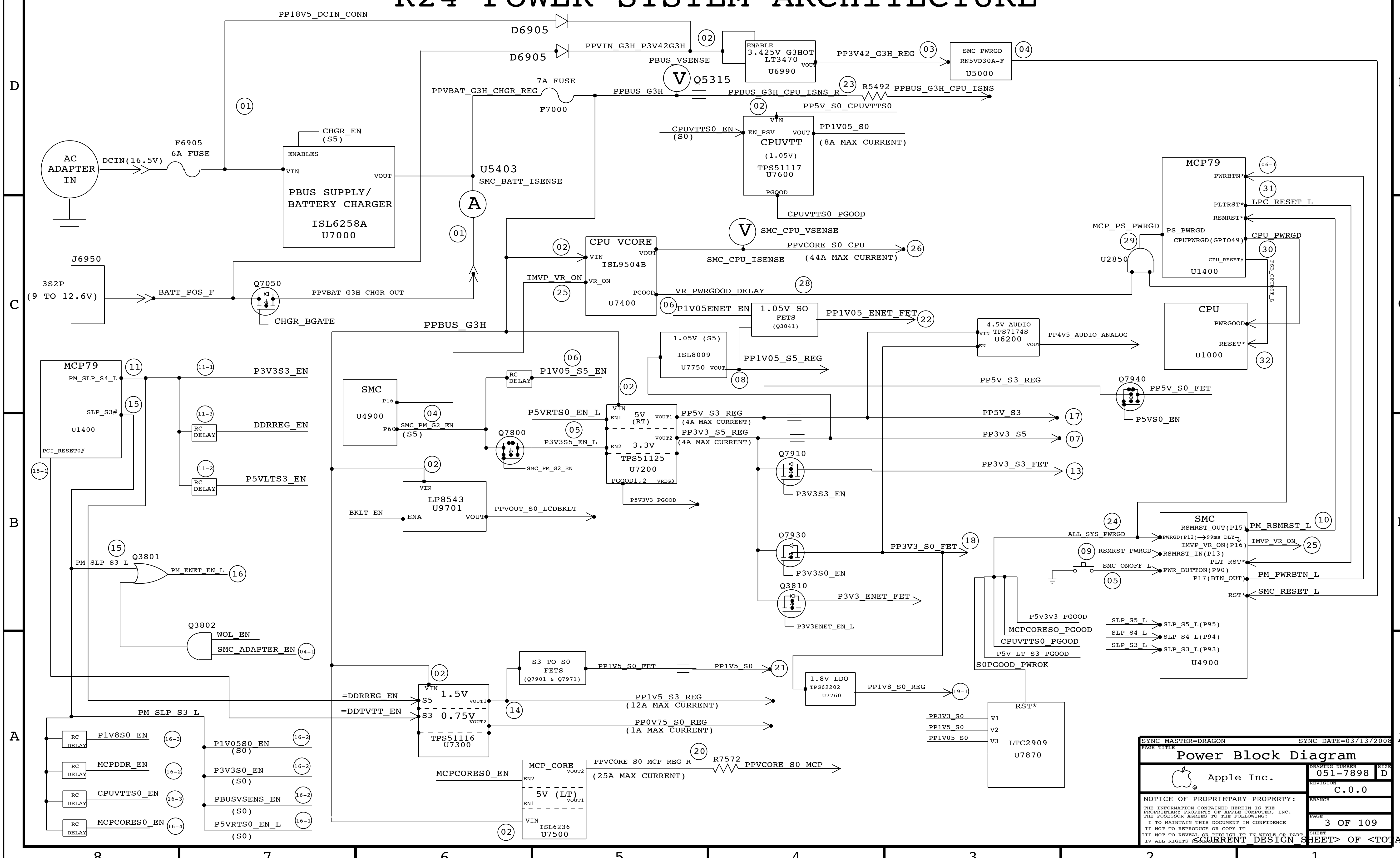
K24 POWER SYSTEM ARCHITECTURE



BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9923	PCBA,MLB,BETTER,K24	K24_COMMON,CPU_2_26GHZ,EEE_6GC,KB_BL
630-9924	PCBA,MLB,BEST,K24	K24_COMMON,CPU_2_53GHZ,EEE_6GD,KB_BL

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6G4]	CRITICAL	EEE_6G4
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6GC]	CRITICAL	EEE_6GC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6GD]	CRITICAL	EEE_6GD

BOM Groups

BOM GROUP	BOM OPTIONS
K24_COMMON	COMMON,ALTERNATE,K24_MCP,K24_MISC,K24_DEBUG_PROD,K24_PROGPARTS
K24_MCP	MCP_B03,BOOT_MODE_USER,MCPSEQ_SMC
K24_MISC	ONEWIRE_PU,DP_ESD,MIKEY,BKLT_PROD,SUPERCAP_NO,LDO_NO
K24_PROGPARTS	BOOTROM_PROG,SMC_PROG,IR_PROG,WELLSPRING_PROG
K24_DEBUG_ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K24_DEBUG_PVT	DEVEL_BOM,BMON_PROD,SMC_DEBUG_YES,XDP,NO_VREFMRGN
K24_DEBUG_PROD	BMON_PROD,SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN
K24_DEVEL_ENG	BMON_ENG,XDP_CONN,LPCPLUS,VREFMRGN,FWPHY_WAKE_YES
K24_DEVEL_PVT	LPCPLUS

K24 BOARD STACK-UP

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3646	1	PDC,SLG8E,PRQ,2.0,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3704	1	PDC,SLGE2,PRQ,2.26,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_26GHZ
337S3639	1	PDC,SLB4N,PRQ,2.4,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3756	1	PDC,SLGFG,PRQ,2.53,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3761	1	PDC,SLGLA,PRQ,2.66,25W,1066,E0,3M,BGA	U1000	CRITICAL	CPU_2_66GHZ
338S0710	1	IC,GMCP,MCP79,35X35MM,BGA1437,B03	U1400	CRITICAL	MCP_B03

Programmable Parts

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
341S2445	1	IC,SMC,K24	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2441	1	IC,PRGRM,EFI BOOTROM,UNLOCK,K24	U6100	CRITICAL	BOOTROM_PROG
338S0375	1	IC,CY7C63833,ENCORE II,USB CONTROLLER	U4800	CRITICAL	IR_BLANK
341S2093	1	IC,IR CONTROLLER,M97	U4800	CRITICAL	IR_PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2503	1	IC,PRGRM,WELLSPRING CONTROLLER	U5701	CRITICAL	WELLSPRING_PROG

LOCKED BOOTROM APN IS 341S2443

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
152S1025	152S1024		ALL	TOKO AS ALTERNATE
337S3769	337S3704		ALL	INTEL P7550 CPU AS ALTERNATE
353S2718	353S2310		ALL	INTERSIL AS ALTERNATE

DEVELOPMENT BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0741	1	K24 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM

SYNC MASTER=M97 MLB

PAGE TITLE
BOM Configuration

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Revision History

NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

SYNC MASTER=M97 MLB

PAGE TITLE

Revision History

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DRAWING NUMBER 051-7898

SIZE D

REVISION C.0.0

BRANCH

Functional Test Points

Fan Connectors

TRUE PP5V_S0 (NEED 3 TP)
TRUE FAN_RT_PWM
TRUE FAN_RT_TACH
(NEED TO ADD 3 GND TP)

MIC FUNC_TEST

TRUE BI_MIC_LO
TRUE BI_MIC_HI
TRUE BI_MIC_SHIELD

SPEAKER FUNC_TEST

TRUE SPKRAMP_L_N_OUT
TRUE SPKRAMP_L_P_OUT
TRUE SPKRAMP_R_N_OUT
TRUE SPKRAMP_R_P_OUT
TRUE SPKRAMP_SUB_N_OUT
TRUE SPKRAMP_SUB_P_OUT

THERMAL FUNC_TEST

TRUE MCPTHMSNS_D2_P
TRUE MCPTHMSNS_D2_N

LVDS FUNC_TEST

TRUE PP3V3_LCDVDD_SW_F
TRUE PP3V3_S0_LCD_F
TRUE PPVOUT_S0_LCDBKLT
TRUE LVDS_IG_DDC_CLK
TRUE LVDS_IG_DDC_DATA
TRUE LVDS_IG_A_DATA_N<0>
TRUE LVDS_IG_A_DATA_P<0>
TRUE LVDS_IG_A_DATA_N<1>
TRUE LVDS_IG_A_DATA_P<1>
TRUE LVDS_IG_A_DATA_N<2>
TRUE LVDS_IG_A_DATA_P<2>
TRUE LVDS_IG_A_CLK_F_N
TRUE LVDS_IG_A_CLK_F_P
TRUE LED_RETURN_1
TRUE LED_RETURN_2
TRUE LED_RETURN_3
TRUE LED_RETURN_4
TRUE LED_RETURN_5
TRUE LED_RETURN_6
TRUE TP_BKL_SYNC
(NEED TO ADD 5 GND TP)

SATA ODD CONN

TRUE PP5V_SW_ODD (NEED 4 TP)
TRUE SMC_ODD_DETECT
TRUE SATA_ODD_D2R_C_P
TRUE SATA_ODD_D2R_C_N
TRUE SATA_ODD_R2D_P
TRUE SATA_ODD_R2D_N
(NEED TO ADD 4 GND TP)

SATA HDD/IR/SIL

TRUE PP5V_S0_HDD_FLT (NEED 4 TP)
TRUE SATA_HDD_R2D_P
TRUE SATA_HDD_R2D_N
TRUE SATA_HDD_D2R_C_P
TRUE SATA_HDD_D2R_C_N
TRUE SYS_LED_ANODE_R
TRUE IR_RX_OUT
TRUE PP5V_S3_IR_R
(NEED TO ADD 4 GND TP)

BATT POWER CONN

TRUE SMBUS_SMC_BSA_SCL
TRUE SMBUS_SMC_BSA_SDA
TRUE SYS_DETECT_L
TRUE BATT_POS_F (NEED 3 TP)
(NEED TO ADD 3 GND TP)

BATT SIGNAL CONN

TRUE PP3V42_G3H (NEED 3 TP)
TRUE SMBUS_SMC_BSA_SCL
TRUE SMBUS_SMC_BSA_SCL
TRUE SMC_BIL_BUTTON_L
TRUE SMC_LID_R
(NEED TO ADD 5 GND TP)

RIGHT CLUTCH CONN

TRUE PP5V_S3_BTCAMERA_F
TRUE PCIE_MINI_D2R_P
TRUE PCIE_MINI_D2R_N
TRUE PCIE_MINI_R2D_P
TRUE PCIE_MINI_R2D_N
TRUE PCIE_CLK100M_MINI_CONN_P
TRUE PCIE_CLK100M_MINI_CONN_N
TRUE USB_CAMERA_CONN_P
TRUE USB_CAMERA_CONN_N
TRUE PP5V_WLAN (NEED 2 TP)
TRUE PCIE_WAKE_L
TRUE SMBUS_SMC_A_S3_SCL
TRUE SMBUS_SMC_A_S3_SDA
TRUE CONN_USB2_BT_P
TRUE CONN_USB2_BT_N
TRUE MINI_CLKREQ_Q_L
TRUE MINI_RESET_CONN_L
(NEED TO ADD 6 GND TP)

IPD_FLEX_CONN

TRUE PP3V3_S3_LDO
TRUE PP18V5_S3
TRUE Z2_CS_L
TRUE Z2_DEBUG3
TRUE Z2_MOSI
TRUE Z2_MISO
TRUE Z2_SCLK
TRUE Z2_BOOST_EN
TRUE Z2_HOST_INTN
TRUE Z2_CLKIN
TRUE Z2_KEY_ACT_L
TRUE Z2_RESET
TRUE PSOC_MISO
TRUE PSOC_MOSI
TRUE PSOC_SCLK
TRUE SMBUS_SMC_A_S3_SDA
TRUE SMBUS_SMC_A_S3_SCL
TRUE PSOC_F_CS_L
TRUE PICKB_L

KEYBOARD CONN

TRUE PP3V3_S3
TRUE PP3V42_G3H
TRUE WS_KBD1
TRUE WS_KBD2
TRUE WS_KBD3
TRUE WS_KBD4
TRUE WS_KBD5
TRUE WS_KBD6
TRUE WS_KBD7
TRUE WS_KBD8
TRUE WS_KBD9
TRUE WS_KBD10
TRUE WS_KBD11
TRUE WS_KBD12
TRUE WS_KBD13
TRUE WS_KBD14
TRUE WS_KBD15_CAP
TRUE WS_KBD16_NUM
TRUE WS_KBD17
TRUE WS_KBD18
TRUE WS_KBD19
TRUE WS_KBD20
TRUE WS_KBD21
TRUE WS_KBD22
TRUE WS_KBD23
TRUE WS_KBD_ONOFF_L
TRUE WS_LEFT_SHIFT_KBD
TRUE WS_LEFT_OPTION_KBD
TRUE WS_CONTROL_KBD
(NEED TO ADD 1 GND TP)

KBD BACKLIGHT CONN

TRUE KBDLED_ANODE (NEED 2 TP)
TRUE SMC_KDBLED_PRESENT_L
(NEED TO ADD 2 GND TP)

DEBUG VOLTAGE

TRUE PPVCORE_S0_CPU
TRUE PPVCORE_S0_MCP
TRUE PP0V75_S0
TRUE PP1V05_S0
TRUE PP1V5_S0
TRUE PP1V8_S0
TRUE PP5V_S0
TRUE PP3V3_S0
TRUE PP1V5_S3
TRUE PP3V3_S3
TRUE PP5V_S3
TRUE PP1V1R1V05_S5
TRUE PP3V3_S5
TRUE PP3V42_G3H
TRUE PPBUS_G3H
TRUE PP3V3_ENET_PHY
TRUE PP1V2R1V05_ENET
TRUE PP3V3_G3_RTC
TRUE PP5V_WLAN
TRUE PP5V_SW_ODD
TRUE PP5V_S0_HDD_FLT
TRUE PP3V3_S5_AVREF_SMC
TRUE PP18V5_S3
TRUE PP3V3_S3_LDO
TRUE PP3V3_LCDVDD_SW_F
TRUE PPVOUT_S0_LCDBKLT
TRUE PP4V5_AUDIO_ANALOG
TRUE SMC_PM_G2_EN
TRUE PM_SLP_S4_L
TRUE PM_SLP_S3_L
(NEED TO ADD 4 GND TP)

DC POWER CONN

TRUE PP18V5_DCIN_FUSE (NEED 3 TP)
TRUE ADAPTER_SENSE
(NEED TO ADD 4 GND TP)

SYNC_MASTER=M97_MLB

PAGE TITLE: FUNC TEST

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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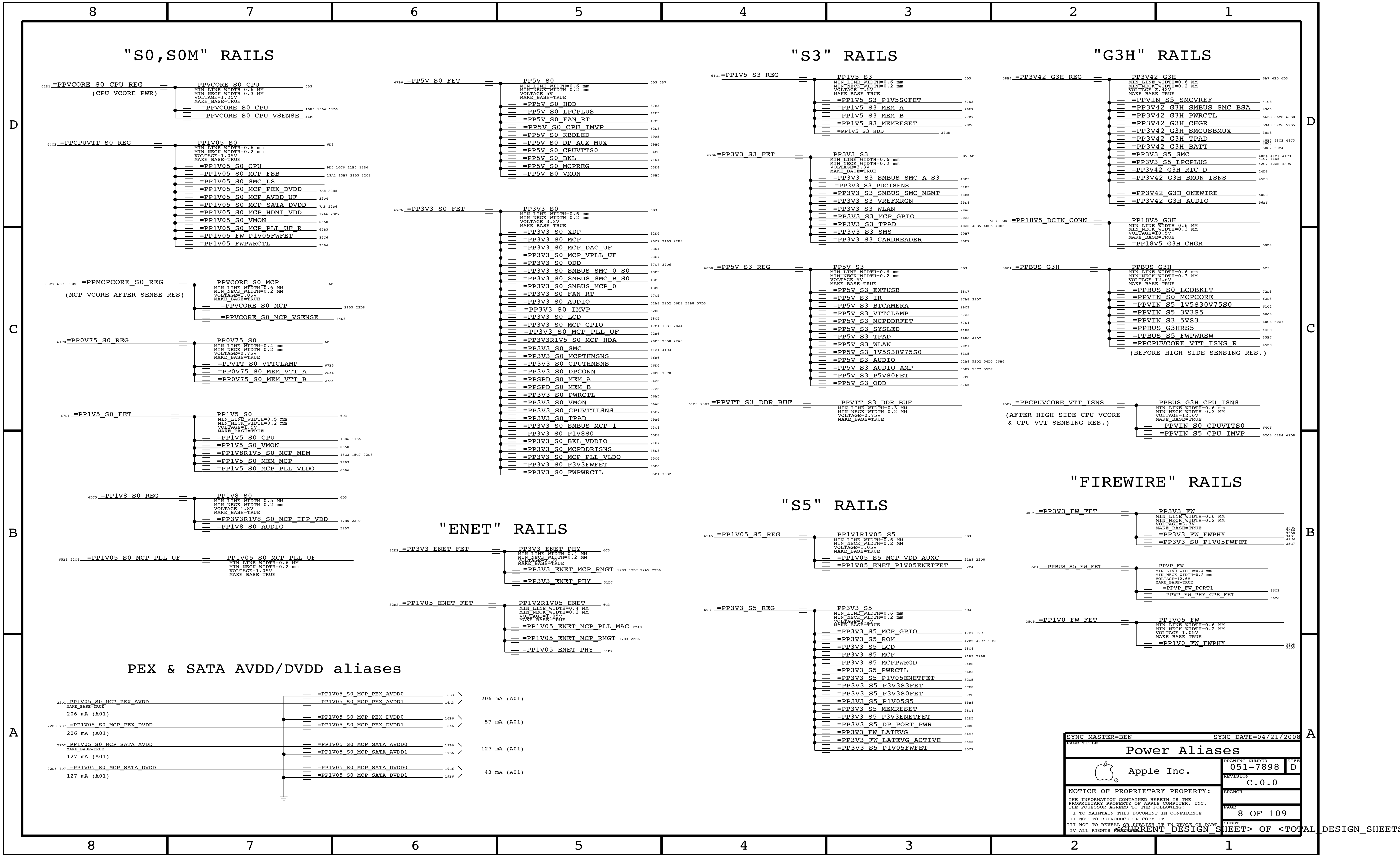
"S0,S0M" RAILS
=PPVCORE_S0_CPU_REG
(CPU VCORE PWR)
PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU
=PPVCORE_S0_CPU_VSENSE
=PPCPUVTT_S0_REG
PP1V05_S0
=PP1V05_S0_CPU
=PP1V05_S0_MCP_FSB
=PP1V05_S0_SMC_LS
=PP1V05_S0_MCP_PEX_DVDD
=PP1V05_S0_MCP_AVDD_UF
=PP1V05_S0_MCP_SATA_DVDD
=PP1V05_S0_MCP_HDMI_VDD
=PP1V05_S0_VMON
=PP1V05_S0_MCP_PLL_UF_R
=PP1V05_FW_P1V05FWFET
=PP1V05_FWPWRCTL
=PPMCPCORE_S0_REG
(MCP VCORE AFTER SENSE RES)
PPVCORE_S0_MCP
=PPVCORE_S0_MCP
=PPVCORE_S0_MCP_VSENSE
=PP0V75_S0_REG
PP0V75_S0
=PPVTT_S0_VTTCLAMP
=PP0V75_S0_MEM_VTT_A
=PP0V75_S0_MEM_VTT_B
=PP1V5_S0_FET
PP1V5_S0
=PP1V5_S0_CPU
=PP1V5_S0_VMON
=PP1V8R1V5_S0_MCP_MEM
=PP1V5_S0_MEM_MCP
=PP1V5_S0_MCP_PLL_VLDO
=PP1V8_S0_REG
PP1V8_S0
=PP3V3R1V8_S0_MCP_IFP_VDD
=PP1V8_S0_AUDIO
=PP1V05_S0_MCP_PLL_UF
PP1V05_S0_MCP_PLL_UF
=PP5V_S0_FET
PP5V_S0
=PP5V_S0_HDD
=PP5V_S0_LPCPLUS
=PP5V_S0_FAN_RT
=PP5V_S0_CPU_IMVP
=PP5V_S0_KBDLED
=PP5V_S0_DP_AUX_MUX
=PP5V_S0_CPUVTTS0
=PP5V_S0_BKL
=PP5V_S0_MCPREG
=PP5V_S0_VMON
=PP3V3_S0_FET
PP3V3_S0
=PP3V3_S0_XDP
=PP3V3_S0_MCP
=PP3V3_S0_MCP_DAC_UF
=PP3V3_S0_MCP_VPLL_UF
=PP3V3_S0_ODD
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_SMBUS_SMC_B_S0
=PP3V3_S0_SMBUS_MCP_0
=PP3V3_S0_FAN_RT
=PP3V3_S0_AUDIO
=PP3V3_S0_IMVP
=PP3V3_S0_LCD
=PP3V3_S0_MCP_GPIO
=PP3V3_S0_MCP_PLL_UF
=PP3V3R1V5_S0_MCP_HDA
=PP3V3_S0_SMC
=PP3V3_S0_MCPTHMSNS
=PP3V3_S0_CPUTHMSNS
=PP3V3_S0_DPCONN
=PPSPD_S0_MEM_A
=PPSPD_S0_MEM_B
=PP3V3_S0_PWRCTL
=PP3V3_S0_VMON
=PP3V3_S0_CPUVTTISNS
=PP3V3_S0_TPAD
=PP3V3_S0_SMBUS_MCP_1
=PP3V3_S0_P1V8S0
=PP3V3_S0_BKL_VDDIO
=PP3V3_S0_MCPDDRISNS
=PP3V3_S0_MCP_PLL_VLDO
=PP3V3_S0_P3V3FWFET
=PP3V3_S0_FWPWRCTL
"ENET" RAILS
=PP3V3_ENET_FET
PP3V3_ENET_PHY
=PP3V3_ENET_MCP_RMGT
=PP3V3_ENET_PHY
=PP1V05_ENET_FET
PP1V2R1V05_ENET
=PP1V05_ENET_MCP_PLL_MAC
=PP1V05_ENET_MCP_RMGT
=PP1V05_ENET_PHY
PEX & SATA AVDD/DVDD aliases
PP1V05_S0_MCP_PEX_AVDD
206 mA (A01)
=PP1V05_S0_MCP_PEX_AVDD0
=PP1V05_S0_MCP_PEX_AVDD1
206 mA (A01)
=PP1V05_S0_MCP_PEX_DVDD
206 mA (A01)
=PP1V05_S0_MCP_PEX_DVDD0
=PP1V05_S0_MCP_PEX_DVDD1
57 mA (A01)
PP1V05_S0_MCP_SATA_AVDD
127 mA (A01)
=PP1V05_S0_MCP_SATA_AVDD0
=PP1V05_S0_MCP_SATA_AVDD1
127 mA (A01)
=PP1V05_S0_MCP_SATA_DVDD
127 mA (A01)
=PP1V05_S0_MCP_SATA_DVDD0
=PP1V05_S0_MCP_SATA_DVDD1
43 mA (A01)
"S3" RAILS
=PP1V5_S3_REG
PP1V5_S3
=PP1V5_S3_P1V5S0FET
=PP1V5_S3_MEM_A
=PP1V5_S3_MEM_B
=PP1V5_S3_MEMRESET
=PP1V5_S3_HDD
=PP3V3_S3_FET
PP3V3_S3
=PP3V3_S3_SMBUS_SMC_A_S3
=PP3V3_S3_PDCISENS
=PP3V3_S3_SMBUS_SMC_MGMT
=PP3V3_S3_VREFMRGN
=PP3V3_S3_WLAN
=PP3V3_S3_MCP_GPIO
=PP3V3_S3_TPAD
=PP3V3_S3_SMS
=PP3V3_S3_CARDREADER
=PP5V_S3_REG
PP5V_S3
=PP5V_S3_EXTUSB
=PP5V_S3_IR
=PP5V_S3_BTCAMERA
=PP5V_S3_VTTCLAMP
=PP5V_S3_MCPDDRFET
=PP5V_S3_SYSLED
=PP5V_S3_TPAD
=PP5V_S3_WLAN
=PP5V_S3_1V5S30V75S0
=PP5V_S3_AUDIO
=PP5V_S3_AUDIO_AMP
=PP5V_S3_P5VS0FET
=PP5V_S3_ODD
=PPVTT_S3_DDR_BUF
PPVTT_S3_DDR_BUF
"S5" RAILS
=PP1V05_S5_REG
PP1V1R1V05_S5
=PP1V05_S5_MCP_VDD_AUXC
=PP1V05_ENET_P1V05ENETFET
=PP3V3_S5_REG
PP3V3_S5
=PP3V3_S5_MCP_GPIO
=PP3V3_S5_ROM
=PP3V3_S5_LCD
=PP3V3_S5_MCP
=PP3V3_S5_MCPPWRGD
=PP3V3_S5_PWRCTL
=PP3V3_S5_P1V05ENETFET
=PP3V3_S5_P3V3S3FET
=PP3V3_S5_P3V3S0FET
=PP3V3_S5_P1V05S5
=PP3V3_S5_MEMRESET
=PP3V3_S5_P3V3ENETFET
=PP3V3_S5_DP_PORT_PWR
=PP3V3_FW_LATEVG
=PP3V3_FW_LATEVG_ACTIVE
=PP3V3_S5_P1V05FWFET
"G3H" RAILS
=PP3V42_G3H_REG
PP3V42_G3H
=PPVIN_S5_SMCVREF
=PP3V42_G3H_SMBUS_SMC_BSA
=PP3V42_G3H_PWRCTL
=PP3V42_G3H_CHGR
=PP3V42_G3H_SMCUSBMUX
=PP3V42_G3H_TPAD
=PP3V42_G3H_BATT
=PP3V3_S5_SMC
=PP3V3_S5_LPCPLUS
=PP3V42_G3H_RTC_D
=PP3V42_G3H_BMON_ISNS
=PP3V42_G3H_ONEWIRE
=PP3V42_G3H_AUDIO
=PP18V5_DCIN_CONN
PP18V5_G3H
=PP18V5_G3H_CHGR
=PPBUS_G3H
PPBUS_G3H
=PPBUS_S0_LCDBKLT
=PPVIN_S0_MCPCORE
=PPVIN_S5_1V5S30V75S0
=PPVIN_S5_3V3S5
=PPVIN_S3_5VS3
=PPBUS_G3HRS5
=PPBUS_S5_FWPWRSW
=PPCPUVCORE_VTT_ISNS_R
(BEFORE HIGH SIDE SENSING RES.)
=PPCPUVCORE_VTT_ISNS
(AFTER HIGH SIDE CPU VCORE & CPU VTT SENSING RES.)
PPBUS_G3H_CPU_ISNS
=PPVIN_S0_CPUVTTS0
=PPVIN_S5_CPU_IMVP
"FIREWIRE" RAILS
=PP3V3_FW_FET
PP3V3_FW
=PP3V3_FW_FWPHY
=PP3V3_S0_P1V05FWFET
=PPBUS_S5_FW_FET
PPVP_FW
=PPVP_FW_PORT1
=PPVP_FW_PHY_CPS_FET
=PP1V0_FW_FET
PP1V05_FW
=PP1V0_FW_FWPHY
SYNC_MASTER=BEN
SYNC_DATE=04/21/2008
PAGE TITLE
Power Aliases
Apple Inc.
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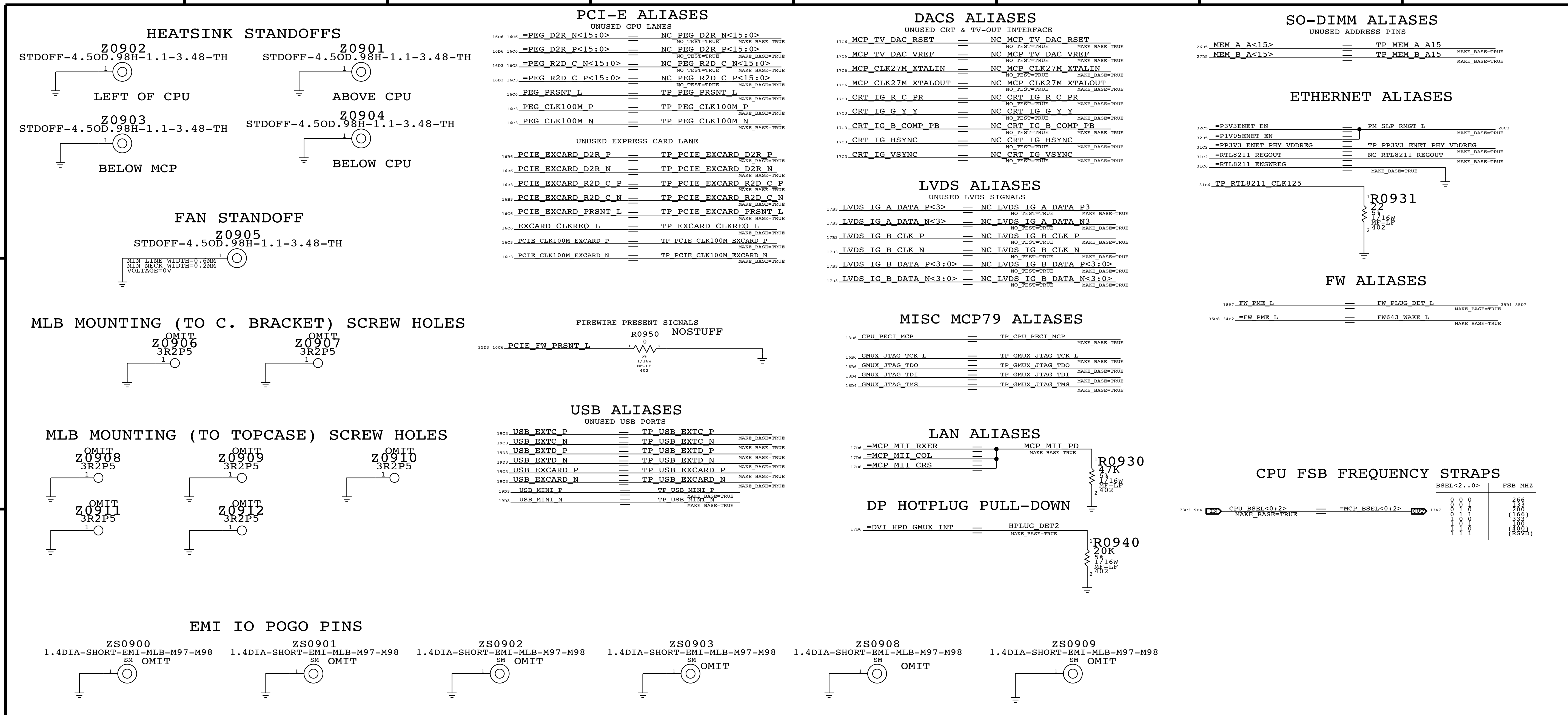
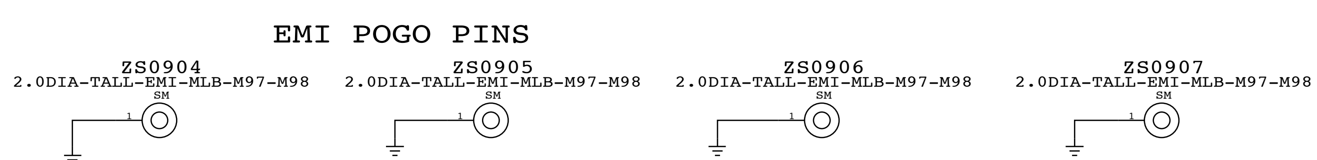


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
870-1801	6	POGO PIN,SHORT,EMI,MLB,K19/K24	ZS0900,ZS0901,ZS0902,ZS0903,ZS0908,ZS0909	CRITICAL	



SYNC_MASTER=M97_MLB

PAGE TITLE

SIGNAL ALIAS

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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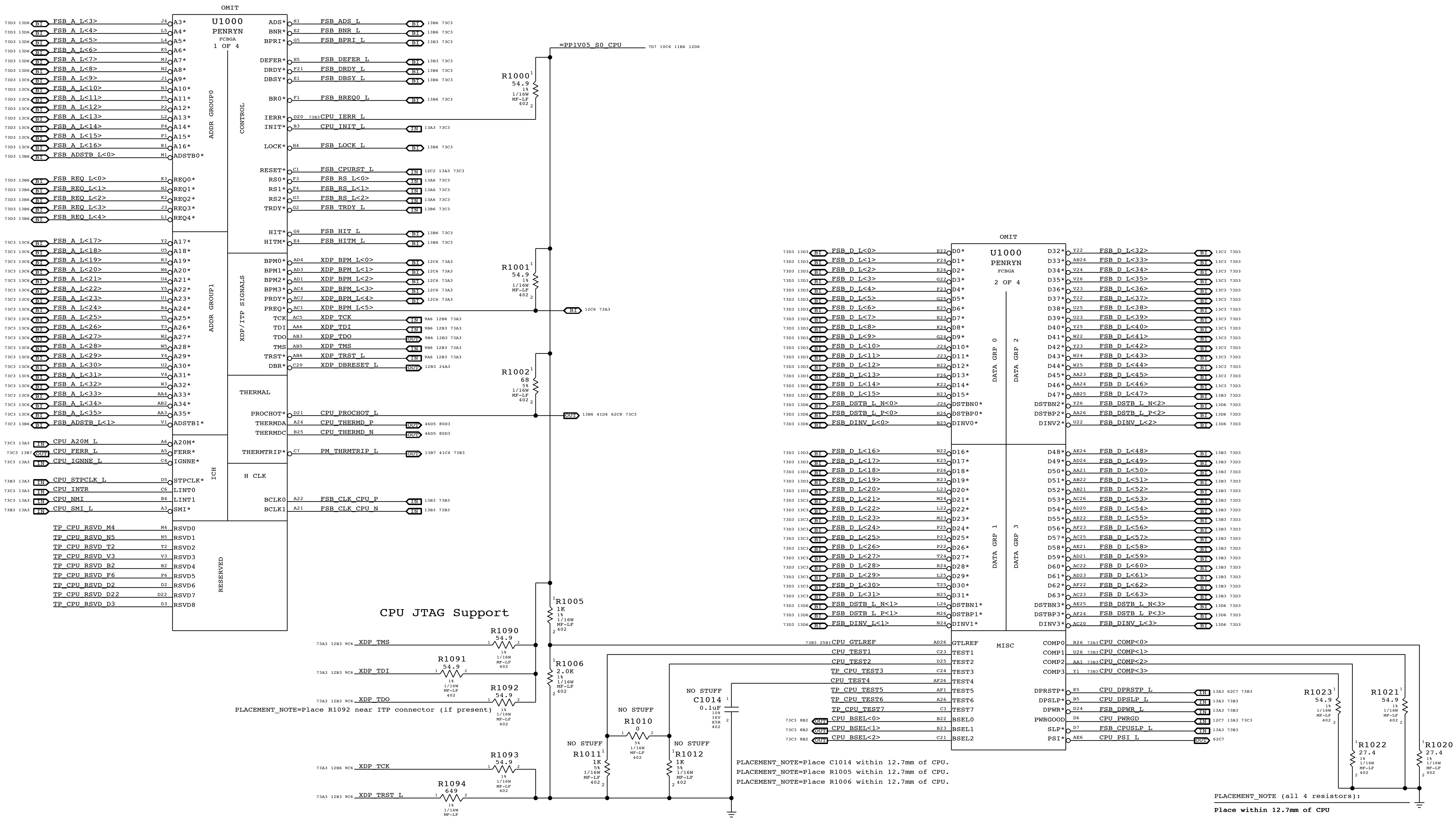
PAGE 9 OF 109

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

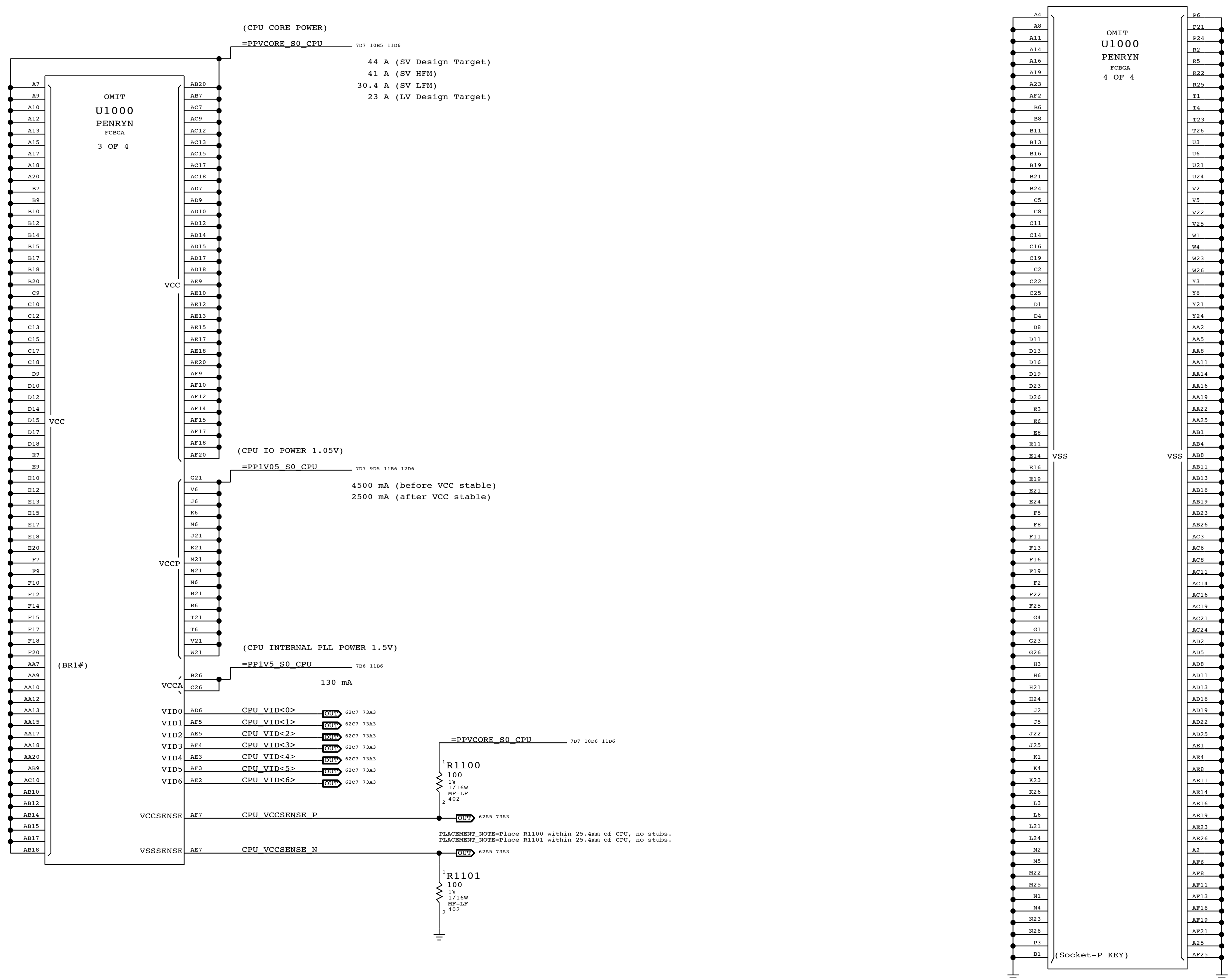


PLACEMENT_NOTE=Place C1014 within 12.7mm of CPU.
PLACEMENT_NOTE=Place R1005 within 12.7mm of CPU.
PLACEMENT_NOTE=Place R1006 within 12.7mm of CPU.

PLACEMENT_NOTE (all 4 resistors):
Place within 12.7mm of CPU

SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC_MASTER=T18_MLB	SYNC_DATE=12/12/2007
PAGE TITLE	CPU FSB
Apple Inc.	DRAWING NUMBER 051-7898, SIZE D
	REVISION C.0.0
	BRANCH
	PAGE 10 OF 109
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

PAGE TITLE
CPU Power & Ground

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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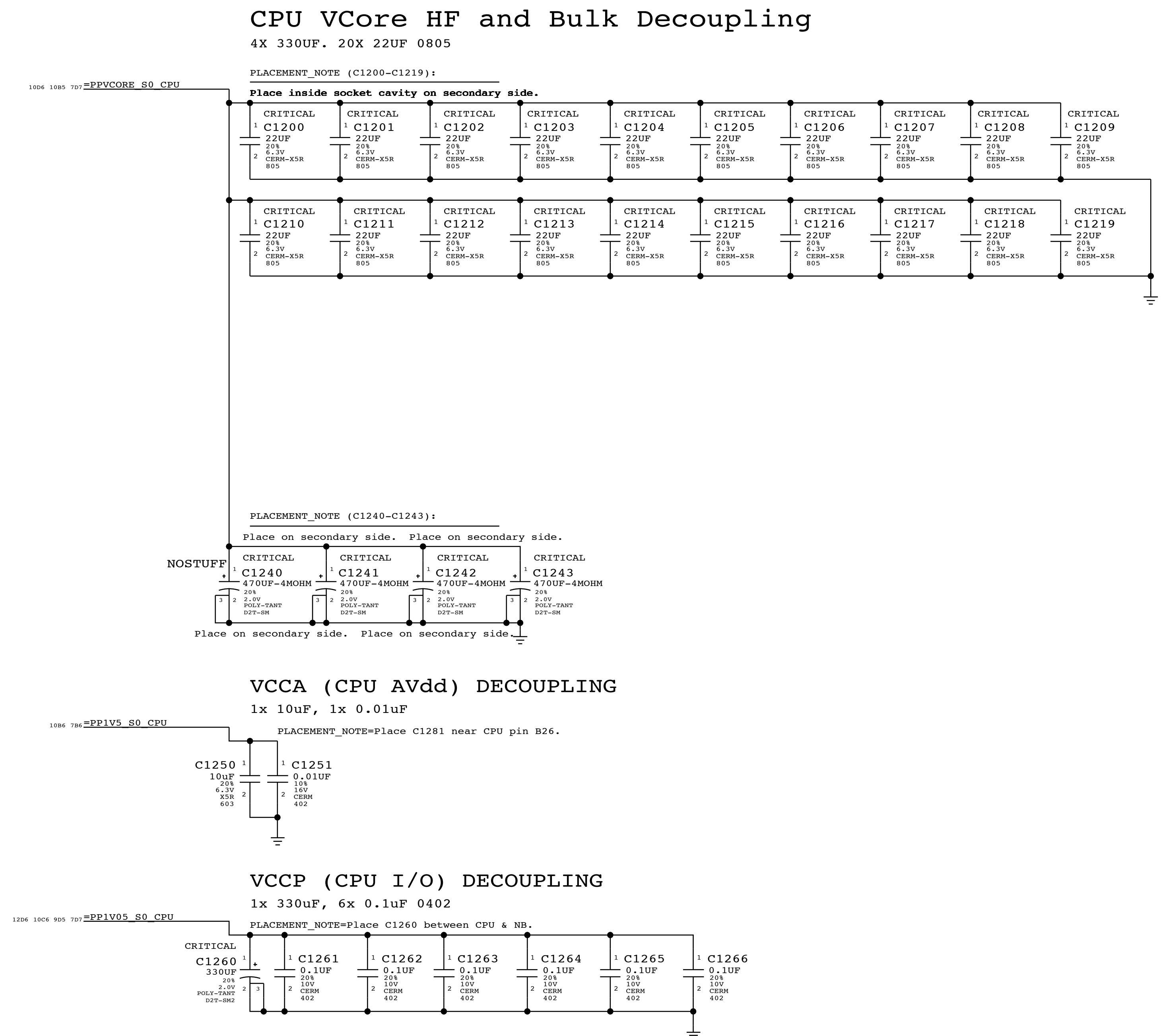


SYNC FROM T18
REMOVE NO STUFF CAPS C1220 TO C1231
REMOVE C1244 & C1245
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

SYNC_MASTER=RAYMOND SYNC_DATE=03/31/2008

PAGE TITLE: CPU Decoupling

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH

PAGE: 12 OF 109

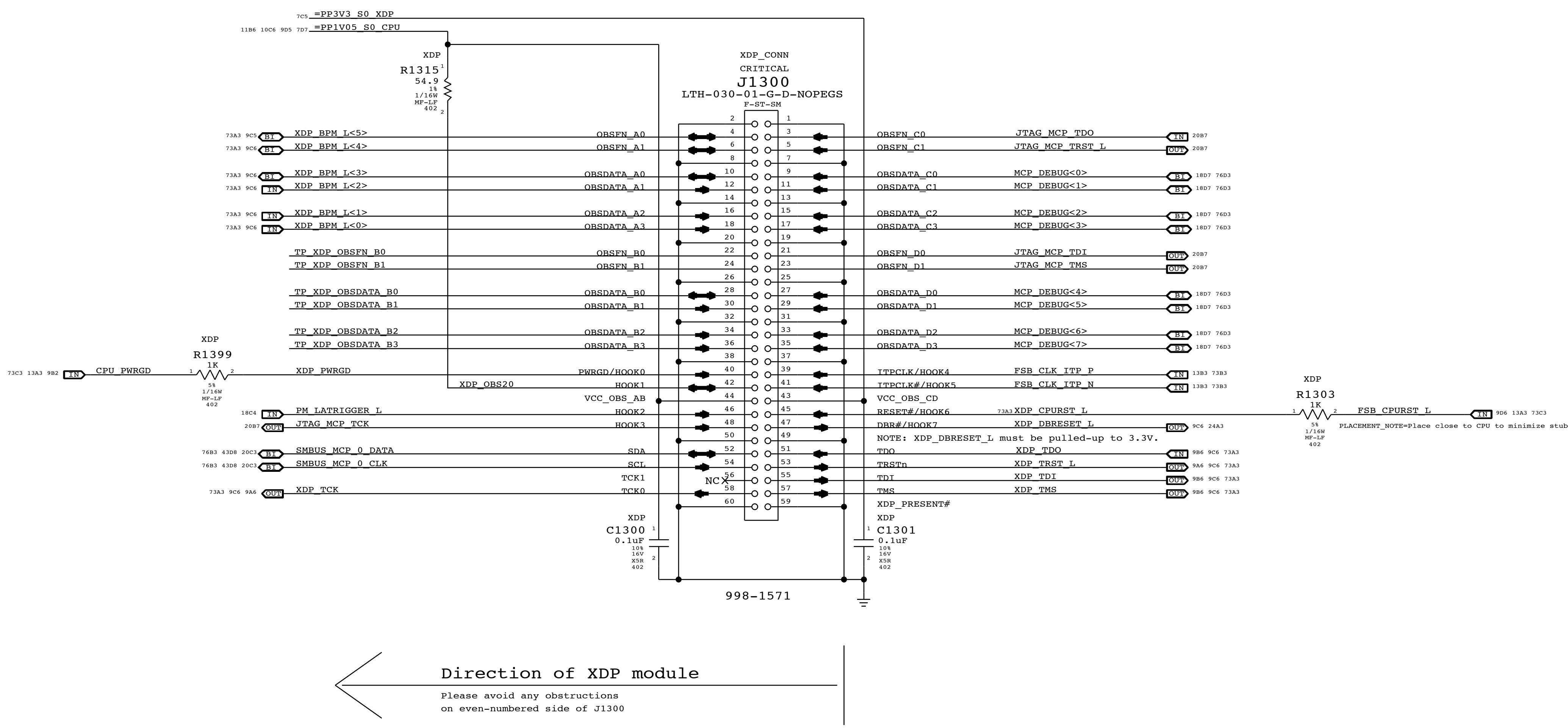
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



SYNC_MASTER=K19_MLB SYNC_DATE=11/07/2008

PAGE TITLE

eXtended Debug Port(MiniXDP)

Apple Inc.

DRAWING NUMBER	SIZE
051-7898	D
REVISION C.0.0	
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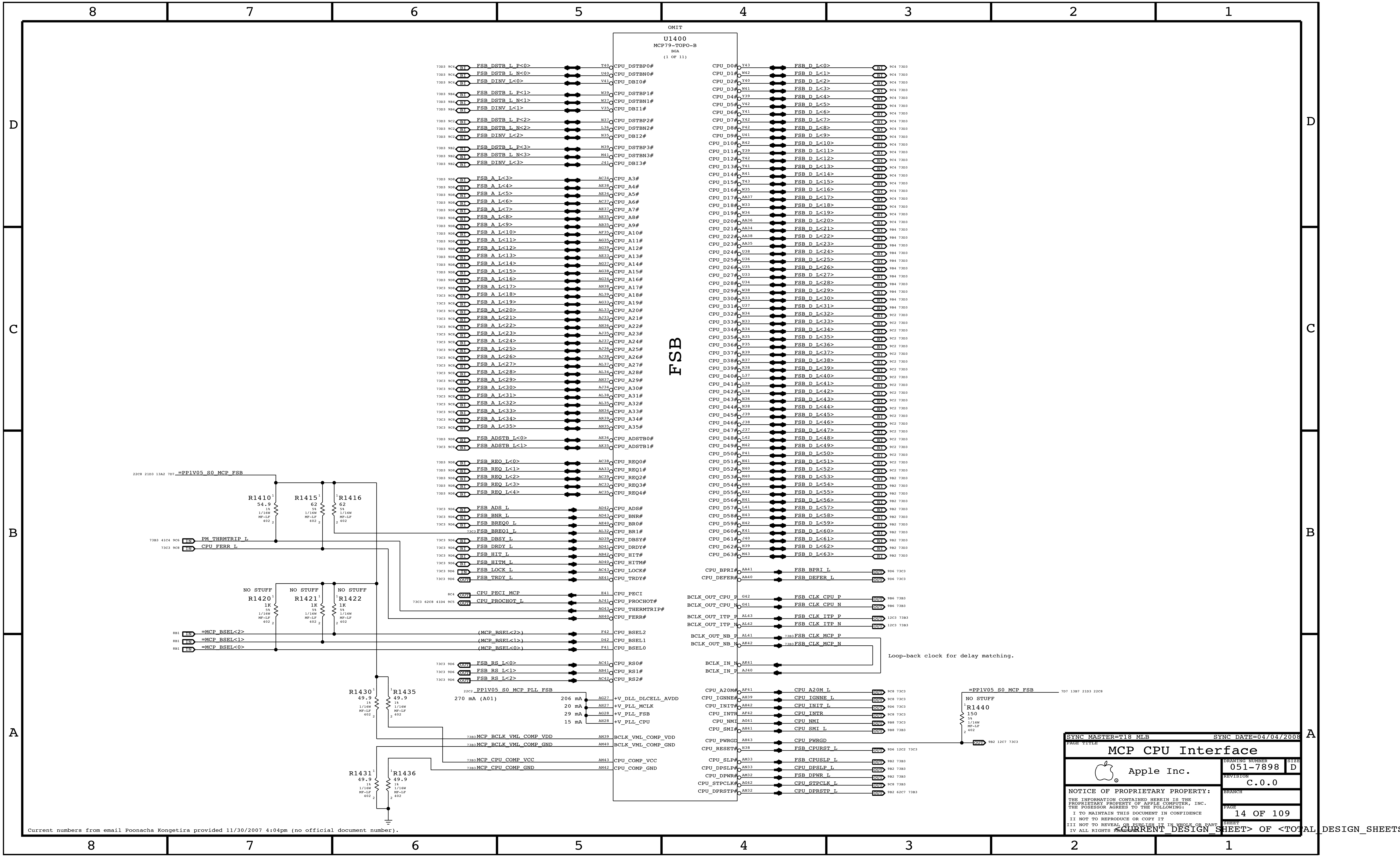
PAGE 13 OF 109	
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	


OMIT
U1400
MCP79-TOPO-B
BGA
(1 OF 11)
FSB
FSB_DSTB_L_P<0>
FSB_DSTB_L_N<0>
FSB_DINV_L<0>
CPU_DSTBP0#
CPU_DSTBN0#
CPU_DBI0#
FSB_A_L<3>
CPU_A3#
FSB_A_L<35>
CPU_A35#
FSB_ADSTB_L<0>
FSB_ADSTB_L<1>
CPU_ADSTB0#
CPU_ADSTB1#
FSB_REQ_L<0>
CPU_REQ0#
FSB_REQ_L<4>
CPU_REQ4#
FSB_ADS_L
FSB_BNR_L
FSB_BREQ0_L
FSB_BREQ1_L
FSB_DBSY_L
FSB_DRDY_L
FSB_HIT_L
FSB_HITM_L
FSB_LOCK_L
FSB_TRDY_L
CPU_ADS#
CPU_BNR#
CPU_BR0#
CPU_BR1#
CPU_DBSY#
CPU_DRDY#
CPU_HIT#
CPU_HITM#
CPU_LOCK#
CPU_TRDY#
CPU_PECI_MCP
CPU_PROCHOT_L
CPU_PECI
CPU_PROCHOT#
CPU_THERMTRIP#
CPU_FERR#
PM_THRMTRIP_L
CPU_FERR_L
=PP1V05_S0_MCP_FSB
R1410
54.9
R1415
62
R1416
62
NO STUFF
R1420
1K
R1421
1K
R1422
1K
=MCP_BSEL<2>
=MCP_BSEL<1>
=MCP_BSEL<0>
(MCP_BSEL<2>)
(MCP_BSEL<1>)
(MCP_BSEL<0>)
CPU_BSEL2
CPU_BSEL1
CPU_BSEL0
FSB_RS_L<0>
FSB_RS_L<1>
FSB_RS_L<2>
CPU_RS0#
CPU_RS1#
CPU_RS2#
PP1V05_S0_MCP_PLL_FSB
270 mA (A01)
206 mA
20 mA
29 mA
15 mA
+V_DLL_DLCELL_AVDD
+V_PLL_MCLK
+V_PLL_FSB
+V_PLL_CPU
R1430
49.9
R1435
49.9
MCP_BCLK_VML_COMP_VDD
MCP_BCLK_VML_COMP_GND
BCLK_VML_COMP_VDD
BCLK_VML_COMP_GND
MCP_CPU_COMP_VCC
MCP_CPU_COMP_GND
CPU_COMP_VCC
CPU_COMP_GND
R1431
49.9
R1436
49.9
CPU_D0#
FSB_D_L<0>
CPU_D63#
FSB_D_L<63>
CPU_BPRI#
CPU_DEFER#
FSB_BPRI_L
FSB_DEFER_L
BCLK_OUT_CPU_P
BCLK_OUT_CPU_N
FSB_CLK_CPU_P
FSB_CLK_CPU_N
BCLK_OUT_ITP_P
BCLK_OUT_ITP_N
FSB_CLK_ITP_P
FSB_CLK_ITP_N
BCLK_OUT_NB_P
BCLK_OUT_NB_N
FSB_CLK_MCP_P
FSB_CLK_MCP_N
BCLK_IN_N
BCLK_IN_P
Loop-back clock for delay matching.
CPU_A20M#
CPU_IGNNE#
CPU_INIT#
CPU_INTR
CPU_NMI
CPU_SMI#
CPU_A20M_L
CPU_IGNNE_L
CPU_INIT_L
CPU_INTR
CPU_NMI
CPU_SMI_L
CPU_PWRGD
CPU_RESET#
CPU_PWRGD
FSB_CPURST_L
CPU_SLP#
CPU_DPSLP#
CPU_DPWR#
CPU_STPCLK#
CPU_DPRSTP#
FSB_CPUSLP_L
FSB_DPSLP_L
FSB_DPWR_L
CPU_STPCLK_L
CPU_DPRSTP_L
=PP1V05_S0_MCP_FSB
NO STUFF
R1440
150
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).
SYNC_MASTER=T18_MLB
SYNC_DATE=04/04/2008
PAGE TITLE
MCP CPU Interface
Apple Inc.
DRAWING NUMBER
051-7898
SIZE
D
REVISION
C.0.0
BRANCH
PAGE
14 OF 109
SHEET
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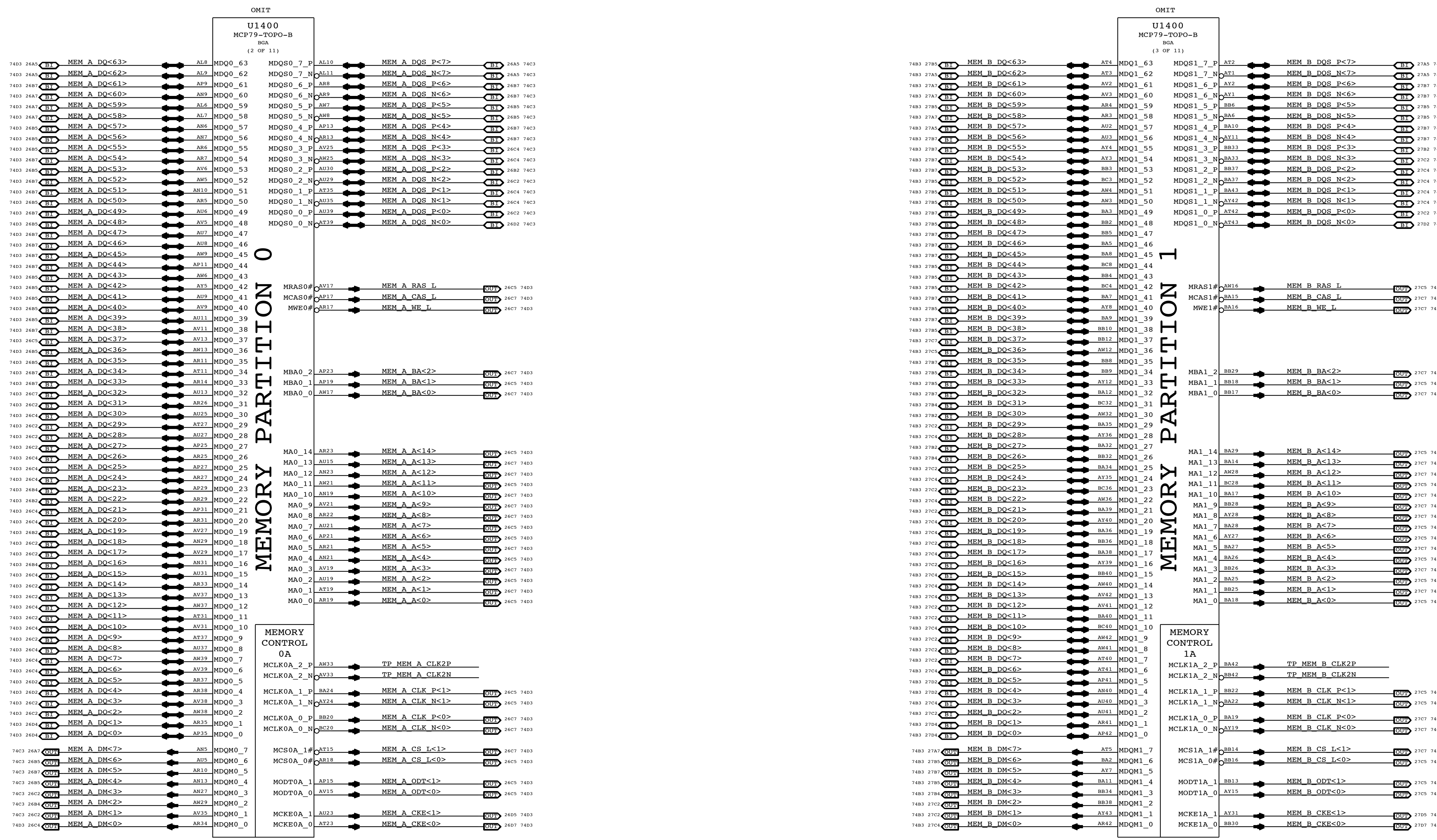

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE

MCP Memory Interface

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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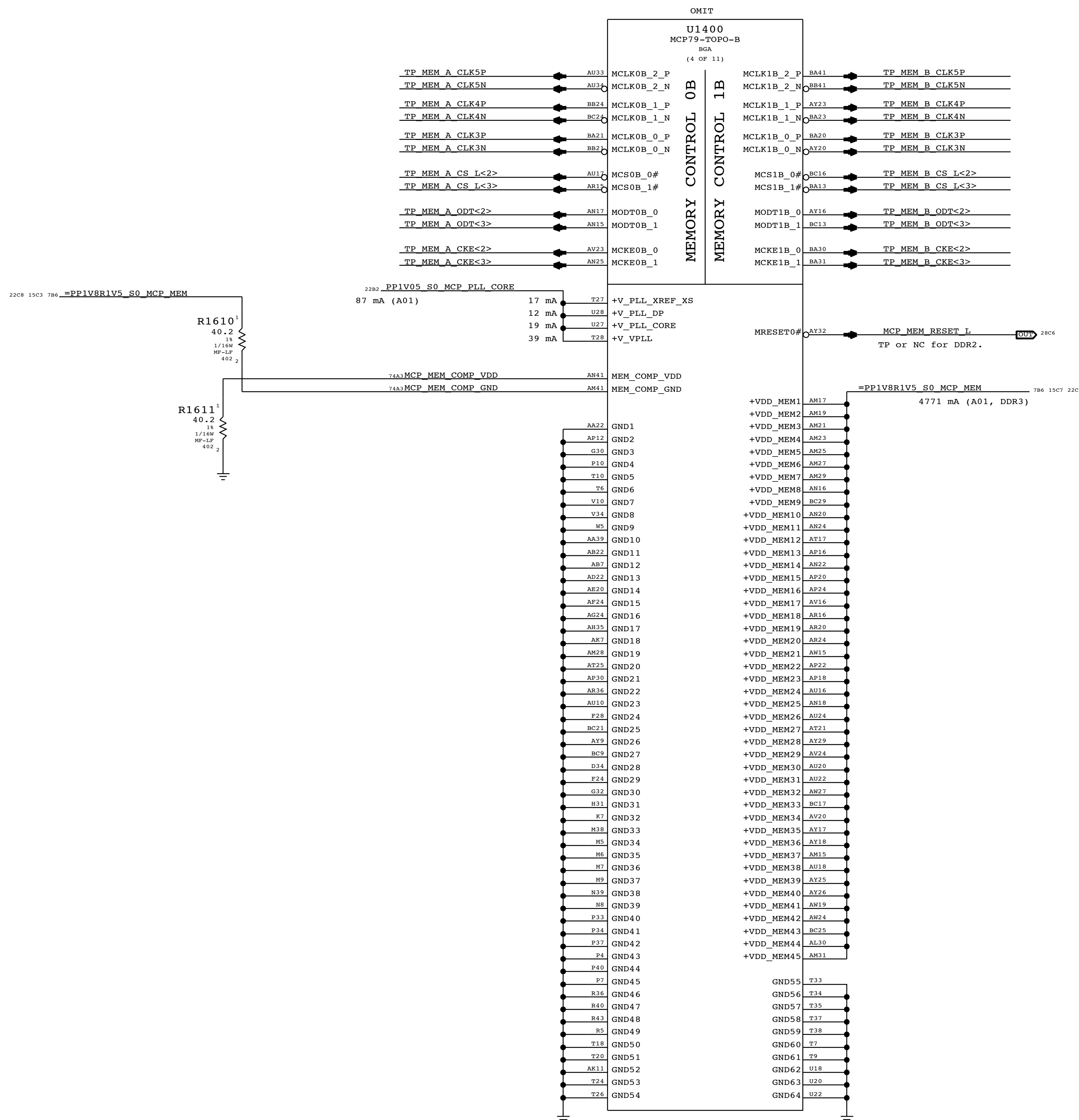
PAGE 15 OF 109

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



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SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE

MCP Memory Misc

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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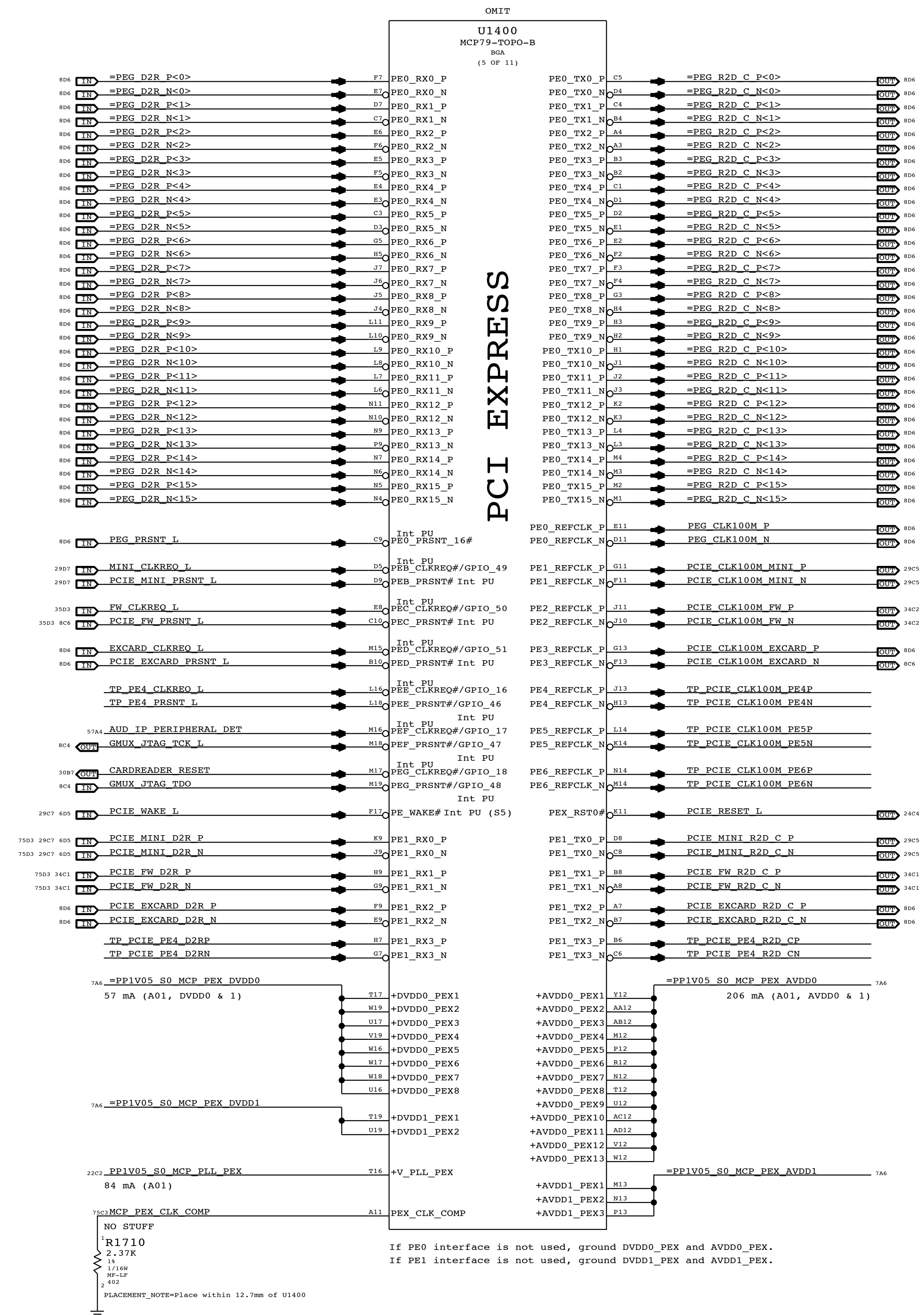
PAGE 16 OF 109

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.
If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.

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SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE
MCP PCIe Interfaces

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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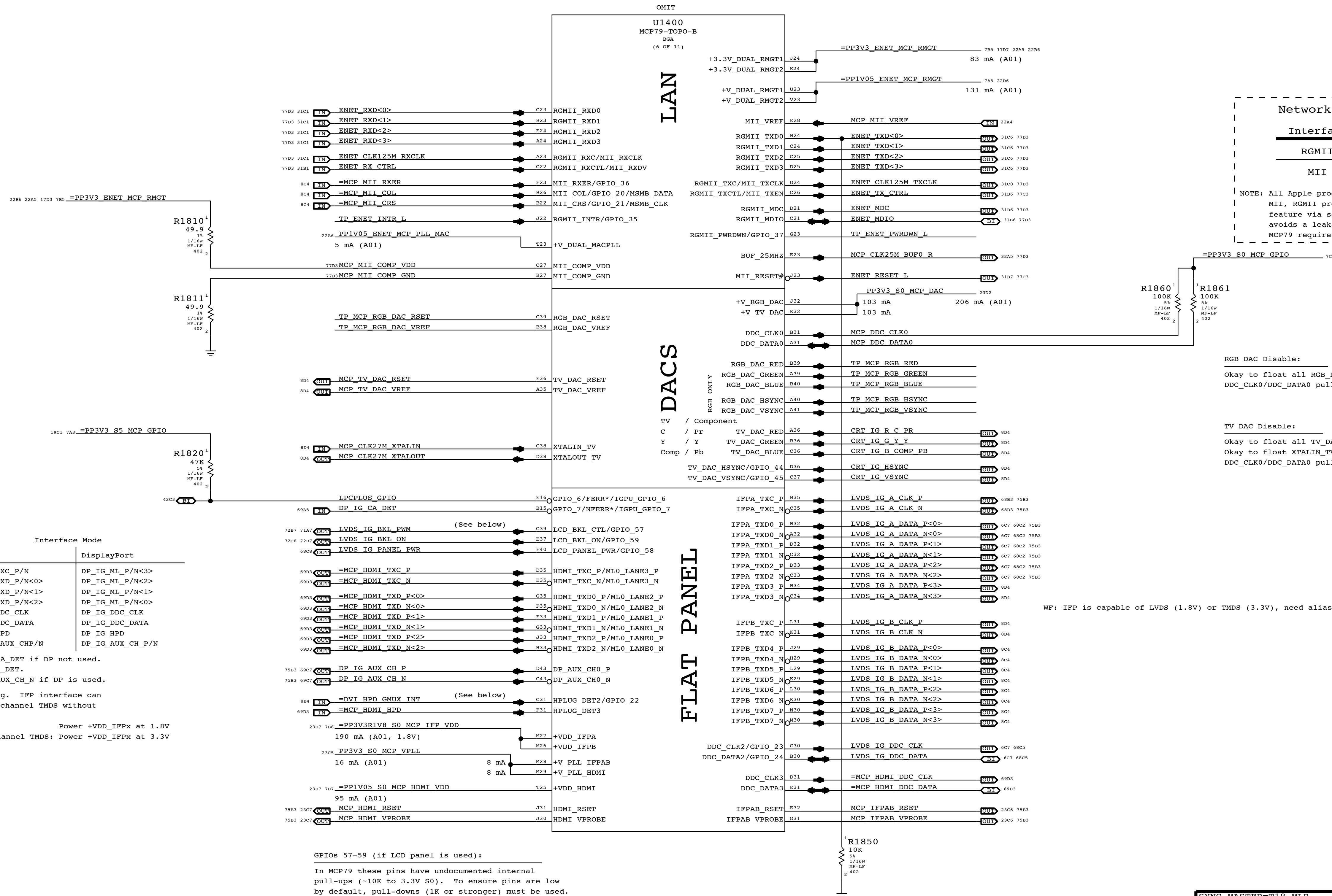
PAGE 17 OF 109

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE
MCP Ethernet & Graphics

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
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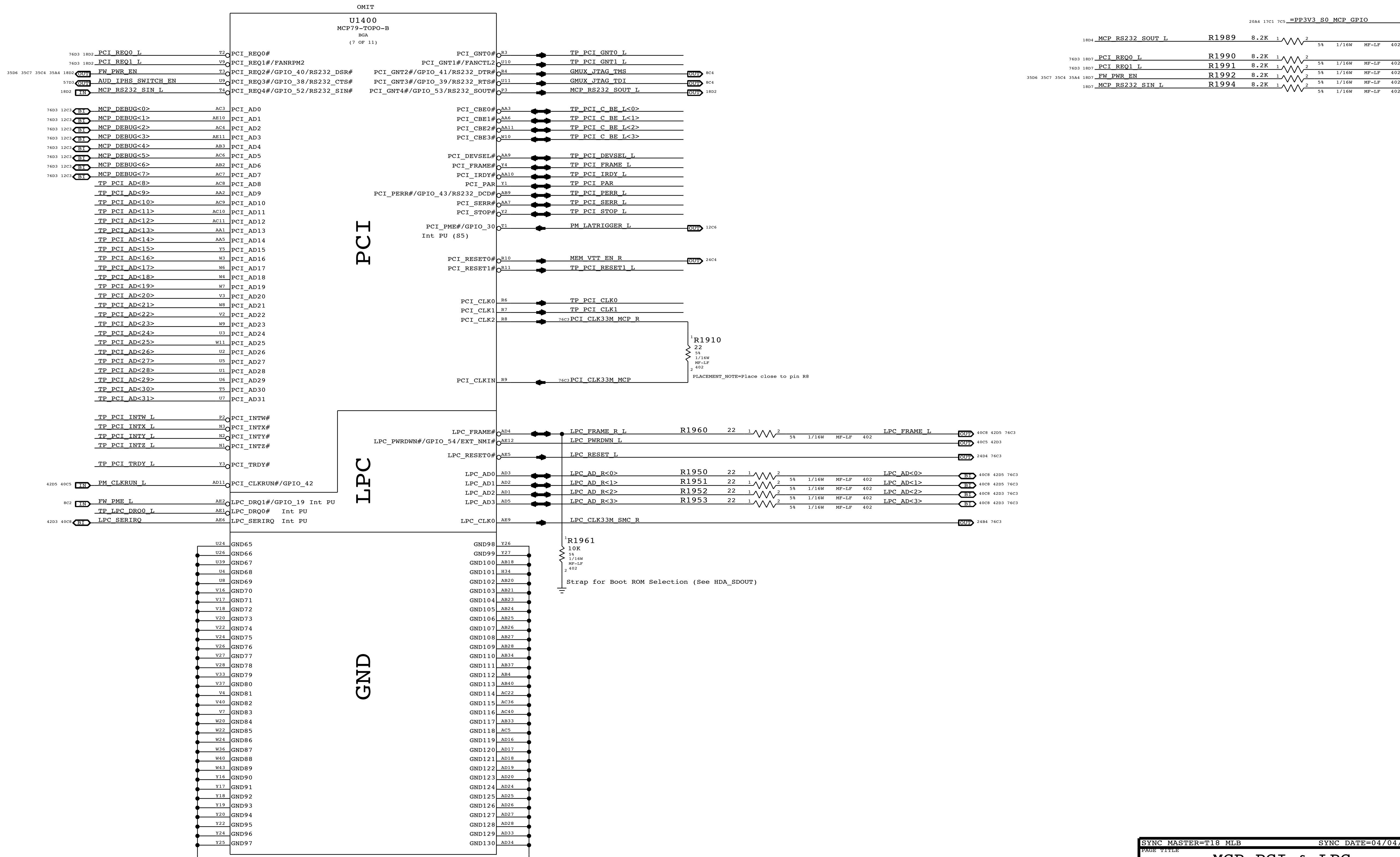
PAGE 18 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=T18_MLB	SYNC_DATE=04/04/2008
PAGE TITLE	MCP PCI & LPC
Apple Inc.	DRAWING NUMBER 051-7898 SIZE D
	REVISION C.0.0
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	PAGE 19 OF 109
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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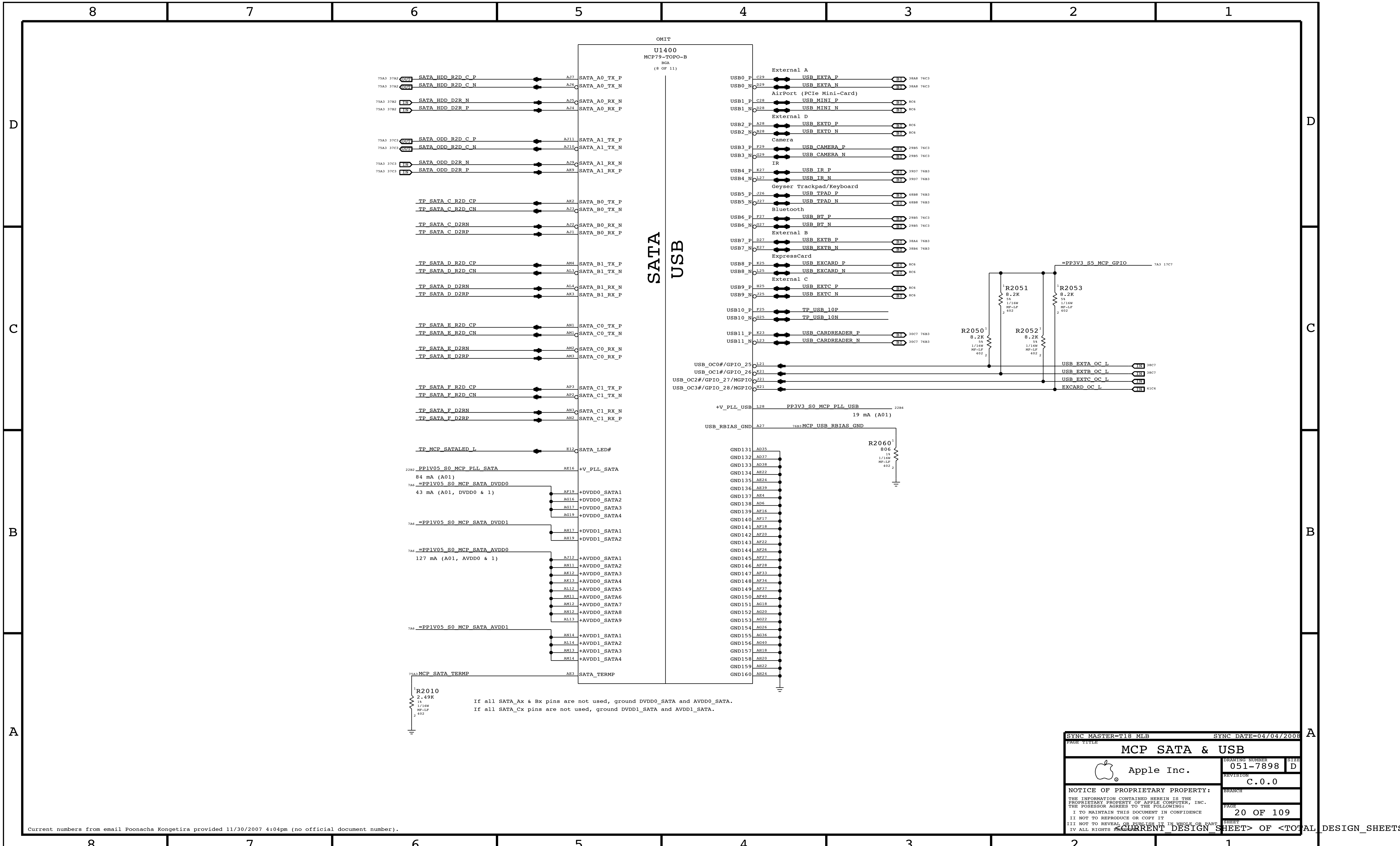

OMIT
U1400
MCP79-TOPO-B
BGA
(8 OF 11)
SATA
USB
SATA_HDD_R2D_C_P
SATA_HDD_R2D_C_N
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_ODD_R2D_C_P
SATA_ODD_R2D_C_N
SATA_ODD_D2R_N
SATA_ODD_D2R_P
TP_SATA_C_R2D_CP
TP_SATA_C_R2D_CN
TP_SATA_C_D2RN
TP_SATA_C_D2RP
TP_SATA_D_R2D_CP
TP_SATA_D_R2D_CN
TP_SATA_D_D2RN
TP_SATA_D_D2RP
TP_SATA_E_R2D_CP
TP_SATA_E_R2D_CN
TP_SATA_E_D2RN
TP_SATA_E_D2RP
TP_SATA_F_R2D_CP
TP_SATA_F_R2D_CN
TP_SATA_F_D2RN
TP_SATA_F_D2RP
TP_MCP_SATALED_L
PP1V05_S0_MCP_PLL_SATA
84 mA (A01)
=PP1V05_S0_MCP_SATA_DVDD0
43 mA (A01, DVDD0 & 1)
=PP1V05_S0_MCP_SATA_DVDD1
=PP1V05_S0_MCP_SATA_AVDD0
127 mA (A01, AVDD0 & 1)
=PP1V05_S0_MCP_SATA_AVDD1
MCP_SATA_TERMP
R2010
2.49K
1%
1/16W
MF-LF
402
SATA_A0_TX_P
SATA_A0_TX_N
SATA_A0_RX_N
SATA_A0_RX_P
SATA_A1_TX_P
SATA_A1_TX_N
SATA_A1_RX_N
SATA_A1_RX_P
SATA_B0_TX_P
SATA_B0_TX_N
SATA_B0_RX_N
SATA_B0_RX_P
SATA_B1_TX_P
SATA_B1_TX_N
SATA_B1_RX_N
SATA_B1_RX_P
SATA_C0_TX_P
SATA_C0_TX_N
SATA_C0_RX_N
SATA_C0_RX_P
SATA_C1_TX_P
SATA_C1_TX_N
SATA_C1_RX_N
SATA_C1_RX_P
SATA_LED#
+V_PLL_SATA
+DVDD0_SATA1
+DVDD0_SATA2
+DVDD0_SATA3
+DVDD0_SATA4
+DVDD1_SATA1
+DVDD1_SATA2
+AVDD0_SATA1
+AVDD0_SATA2
+AVDD0_SATA3
+AVDD0_SATA4
+AVDD0_SATA5
+AVDD0_SATA6
+AVDD0_SATA7
+AVDD0_SATA8
+AVDD0_SATA9
+AVDD1_SATA1
+AVDD1_SATA2
+AVDD1_SATA3
+AVDD1_SATA4
SATA_TERMP
External A
USB0_P
USB0_N
USB_EXTA_P
USB_EXTA_N
AirPort (PCIe Mini-Card)
USB1_P
USB1_N
USB_MINI_P
USB_MINI_N
External D
USB2_P
USB2_N
USB_EXTD_P
USB_EXTD_N
Camera
USB3_P
USB3_N
USB_CAMERA_P
USB_CAMERA_N
IR
USB4_P
USB4_N
USB_IR_P
USB_IR_N
Geyser Trackpad/Keyboard
USB5_P
USB5_N
USB_TPAD_P
USB_TPAD_N
Bluetooth
USB6_P
USB6_N
USB_BT_P
USB_BT_N
External B
USB7_P
USB7_N
USB_EXTB_P
USB_EXTB_N
ExpressCard
USB8_P
USB8_N
USB_EXCARD_P
USB_EXCARD_N
External C
USB9_P
USB9_N
USB_EXTC_P
USB_EXTC_N
USB10_P
USB10_N
TP_USB_10P
TP_USB_10N
USB11_P
USB11_N
USB_CARDREADER_P
USB_CARDREADER_N
USB_OC0#/GPIO_25
USB_OC1#/GPIO_26
USB_OC2#/GPIO_27/MGPIO
USB_OC3#/GPIO_28/MGPIO
USB_EXTA_OC_L
USB_EXTB_OC_L
USB_EXTC_OC_L
EXCARD_OC_L
=PP3V3_S5_MCP_GPIO
R2050
R2051
R2052
R2053
8.2K
5%
1/16W
MF-LF
402
+V_PLL_USB
PP3V3_S0_MCP_PLL_USB
19 mA (A01)
USB_RBIAS_GND
MCP_USB_RBIAS_GND
R2060
806
1%
1/16W
MF-LF
402
GND131
GND132
GND133
GND134
GND135
GND136
GND137
GND138
GND139
GND140
GND141
GND142
GND143
GND144
GND145
GND146
GND147
GND148
GND149
GND150
GND151
GND152
GND153
GND154
GND155
GND156
GND157
GND158
GND159
GND160
If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.
SYNC_MASTER=T18_MLB
SYNC_DATE=04/04/2008
PAGE TITLE
MCP SATA & USB
Apple Inc.
DRAWING NUMBER
051-7898
SIZE
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REVISION
C.0.0
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20 OF 109
SHEET
<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>
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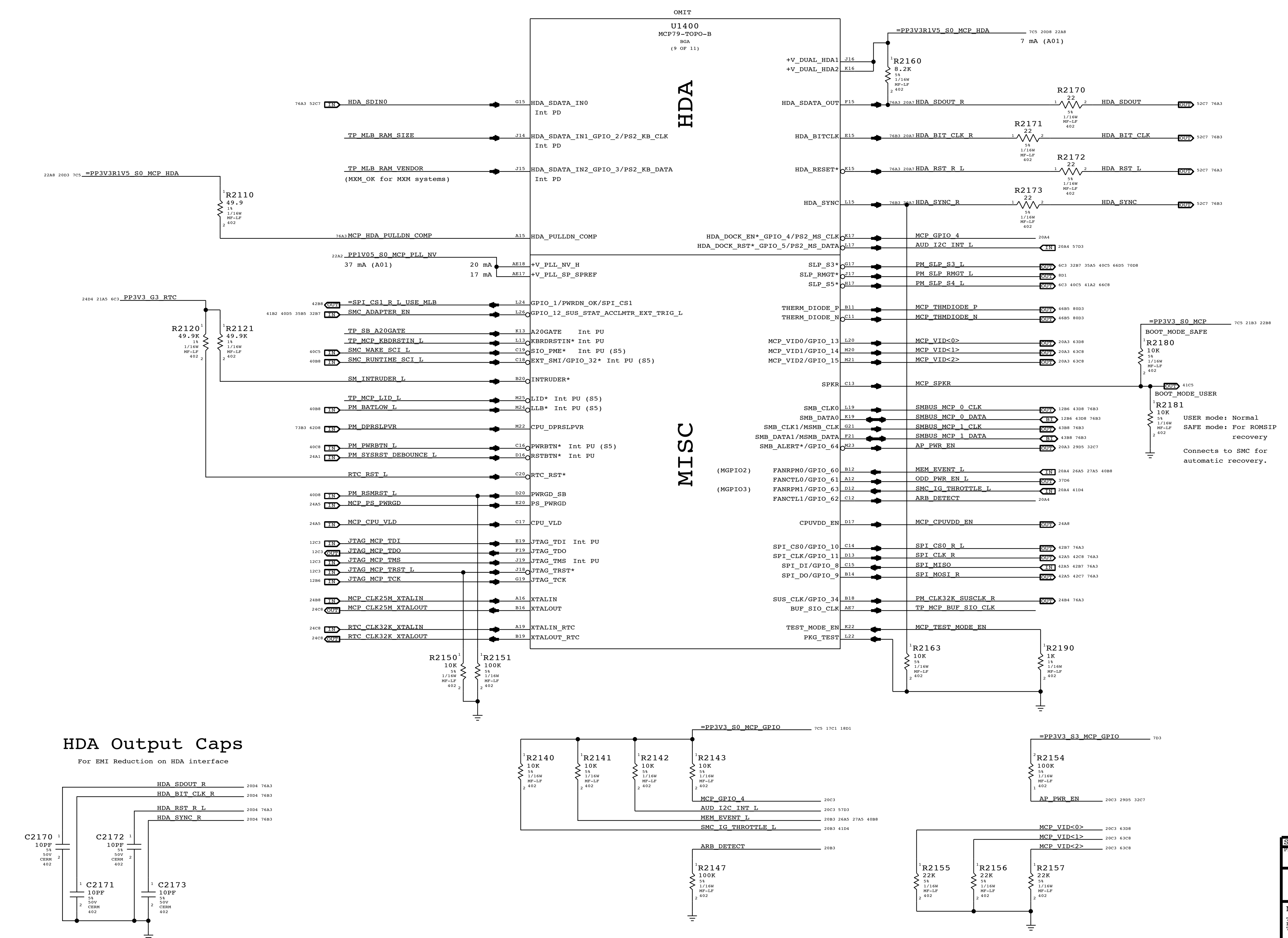

BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

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SYNC_MASTER=T18_MLB SYNC_DATE=06/26/2008

PAGE TITLE

MCP HDA & MISC

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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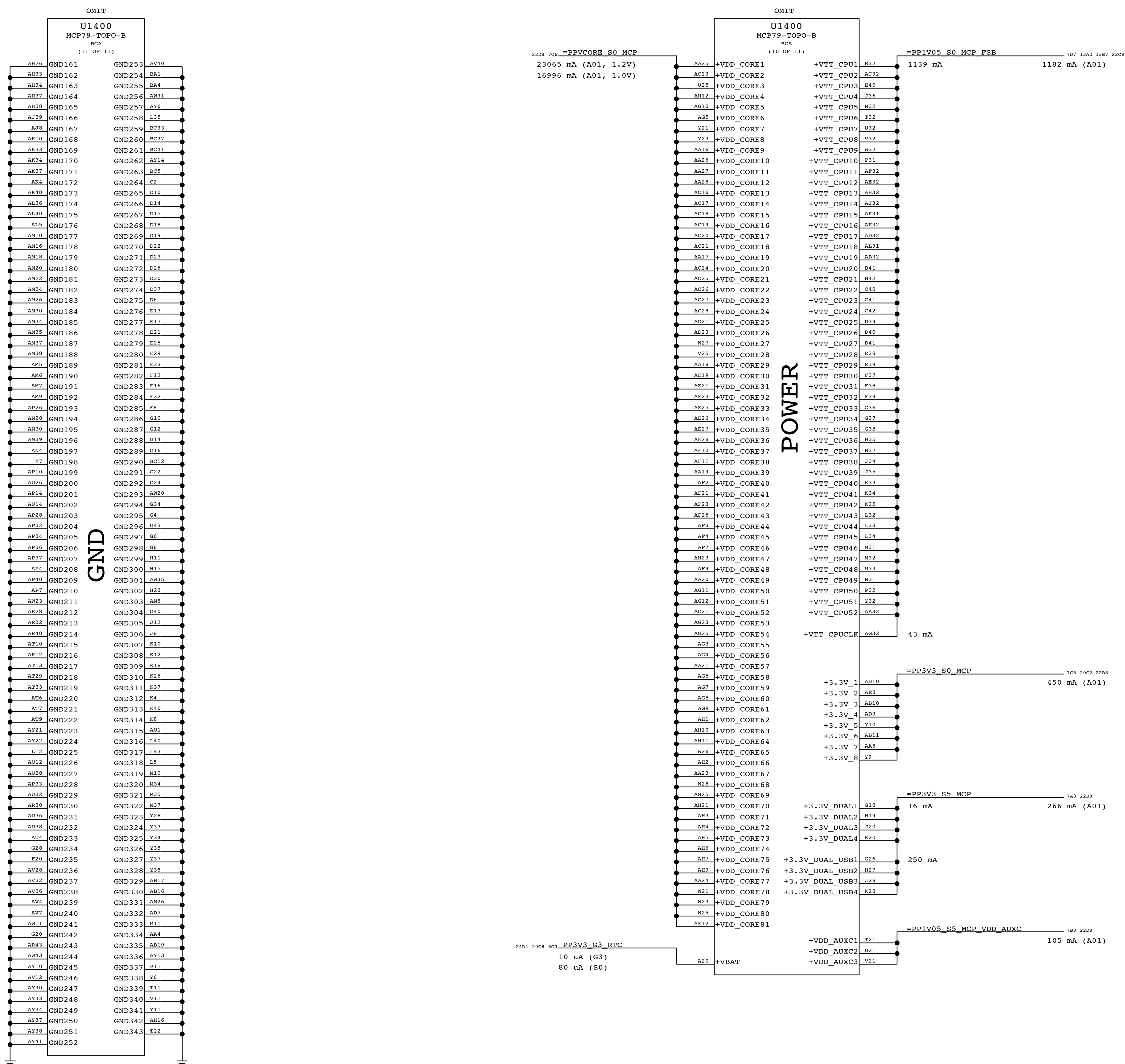

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SYNC MASTER=T18 MLB SYNC DATE=04/04/2008

PAGE TITLE

MCP Power & Ground

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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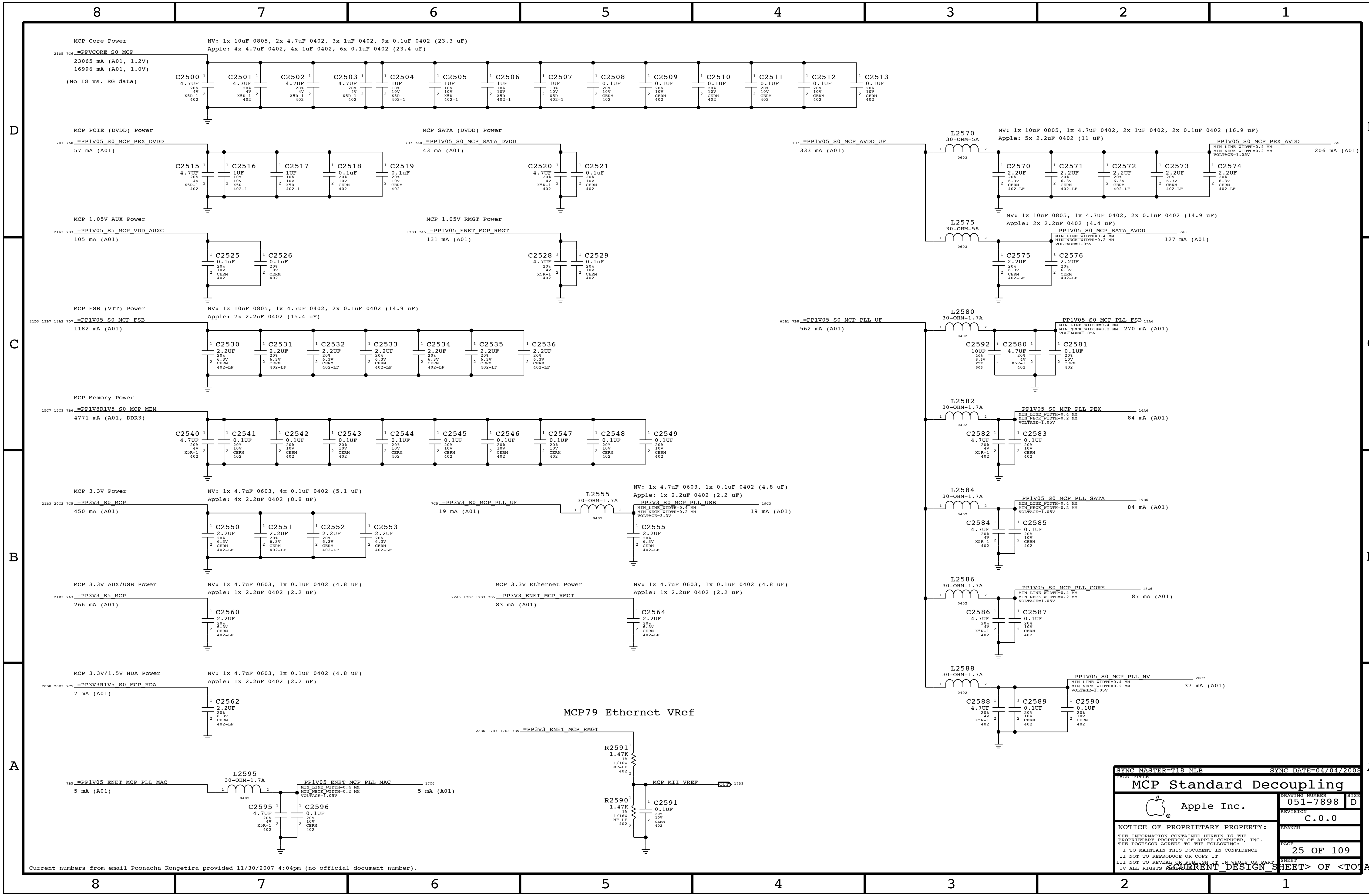
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



MCP Core Power
NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)
=PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)
C2500 4.7UF
C2501 4.7UF
C2502 4.7UF
C2503 4.7UF
C2504 1UF
C2505 1UF
C2506 1UF
C2507 1UF
C2508 0.1UF
C2509 0.1UF
C2510 0.1UF
C2511 0.1UF
C2512 0.1UF
C2513 0.1UF
MCP PCIE (DVDD) Power
=PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)
C2515 4.7UF
C2516 1UF
C2517 1UF
C2518 0.1UF
C2519 0.1UF
MCP SATA (DVDD) Power
=PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)
C2520 4.7UF
C2521 0.1UF
MCP 1.05V AUX Power
=PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)
C2525 0.1UF
C2526 0.1UF
MCP 1.05V RMGT Power
=PP1V05_ENET_MCP_RMGT
131 mA (A01)
C2528 4.7UF
C2529 0.1UF
MCP FSB (VTT) Power
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)
=PP1V05_S0_MCP_FSB
1182 mA (A01)
C2530 2.2UF
C2531 2.2UF
C2532 2.2UF
C2533 2.2UF
C2534 2.2UF
C2535 2.2UF
C2536 2.2UF
MCP Memory Power
=PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)
C2540 4.7UF
C2541 0.1UF
C2542 0.1UF
C2543 0.1UF
C2544 0.1UF
C2545 0.1UF
C2546 0.1UF
C2547 0.1UF
C2548 0.1UF
C2549 0.1UF
MCP 3.3V Power
NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)
=PP3V3_S0_MCP
450 mA (A01)
C2550 2.2UF
C2551 2.2UF
C2552 2.2UF
C2553 2.2UF
=PP3V3_S0_MCP_PLL_UF
19 mA (A01)
L2555 30-OHM-1.7A
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
PP3V3_S0_MCP_PLL_USB
19 mA (A01)
C2555 2.2UF
MCP 3.3V AUX/USB Power
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
=PP3V3_S5_MCP
266 mA (A01)
C2560 2.2UF
MCP 3.3V Ethernet Power
=PP3V3_ENET_MCP_RMGT
83 mA (A01)
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2564 2.2UF
MCP 3.3V/1.5V HDA Power
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
=PP3V3R1V5_S0_MCP_HDA
7 mA (A01)
C2562 2.2UF
MCP79 Ethernet VRef
=PP3V3_ENET_MCP_RMGT
R2591 1.47K
R2590 1.47K
MCP_MII_VREF
C2591 0.1UF
=PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)
L2595 30-OHM-1.7A
PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)
C2595 4.7UF
C2596 0.1UF
=PP1V05_S0_MCP_AVDD_UF
333 mA (A01)
L2570 30-OHM-5A
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)
PP1V05_S0_MCP_PEX_AVDD
206 mA (A01)
C2570 2.2UF
C2571 2.2UF
C2572 2.2UF
C2573 2.2UF
C2574 2.2UF
L2575 30-OHM-5A
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)
PP1V05_S0_MCP_SATA_AVDD
127 mA (A01)
C2575 2.2UF
C2576 2.2UF
=PP1V05_S0_MCP_PLL_UF
562 mA (A01)
L2580 30-OHM-1.7A
PP1V05_S0_MCP_PLL_FSB
270 mA (A01)
C2592 10UF
C2580 4.7UF
C2581 0.1UF
L2582 30-OHM-1.7A
PP1V05_S0_MCP_PLL_PEX
84 mA (A01)
C2582 4.7UF
C2583 0.1UF
L2584 30-OHM-1.7A
PP1V05_S0_MCP_PLL_SATA
84 mA (A01)
C2584 4.7UF
C2585 0.1UF
L2586 30-OHM-1.7A
PP1V05_S0_MCP_PLL_CORE
87 mA (A01)
C2586 4.7UF
C2587 0.1UF
L2588 30-OHM-1.7A
PP1V05_S0_MCP_PLL_NV
37 mA (A01)
C2588 4.7UF
C2589 0.1UF
C2590 0.1UF
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).
SYNC MASTER=T18_MLB
SYNC DATE=04/04/2008
PAGE TITLE
MCP Standard Decoupling
Apple Inc.
DRAWING NUMBER 051-7898
SIZE D
REVISION C.0.0
BRANCH
PAGE 25 OF 109
SHEET
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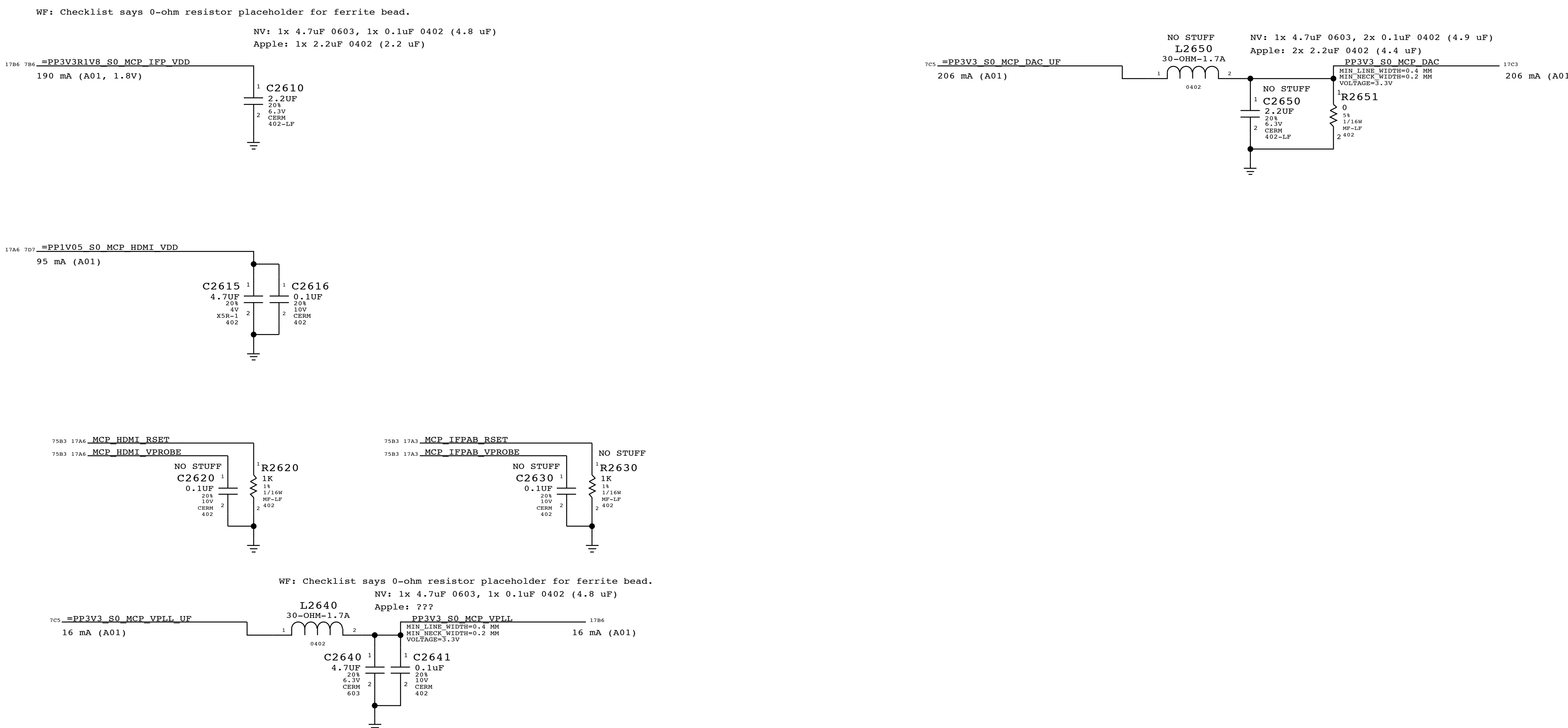

SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC
REMOVE HDCP ROMS

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

PAGE TITLE: MCP Graphics Support

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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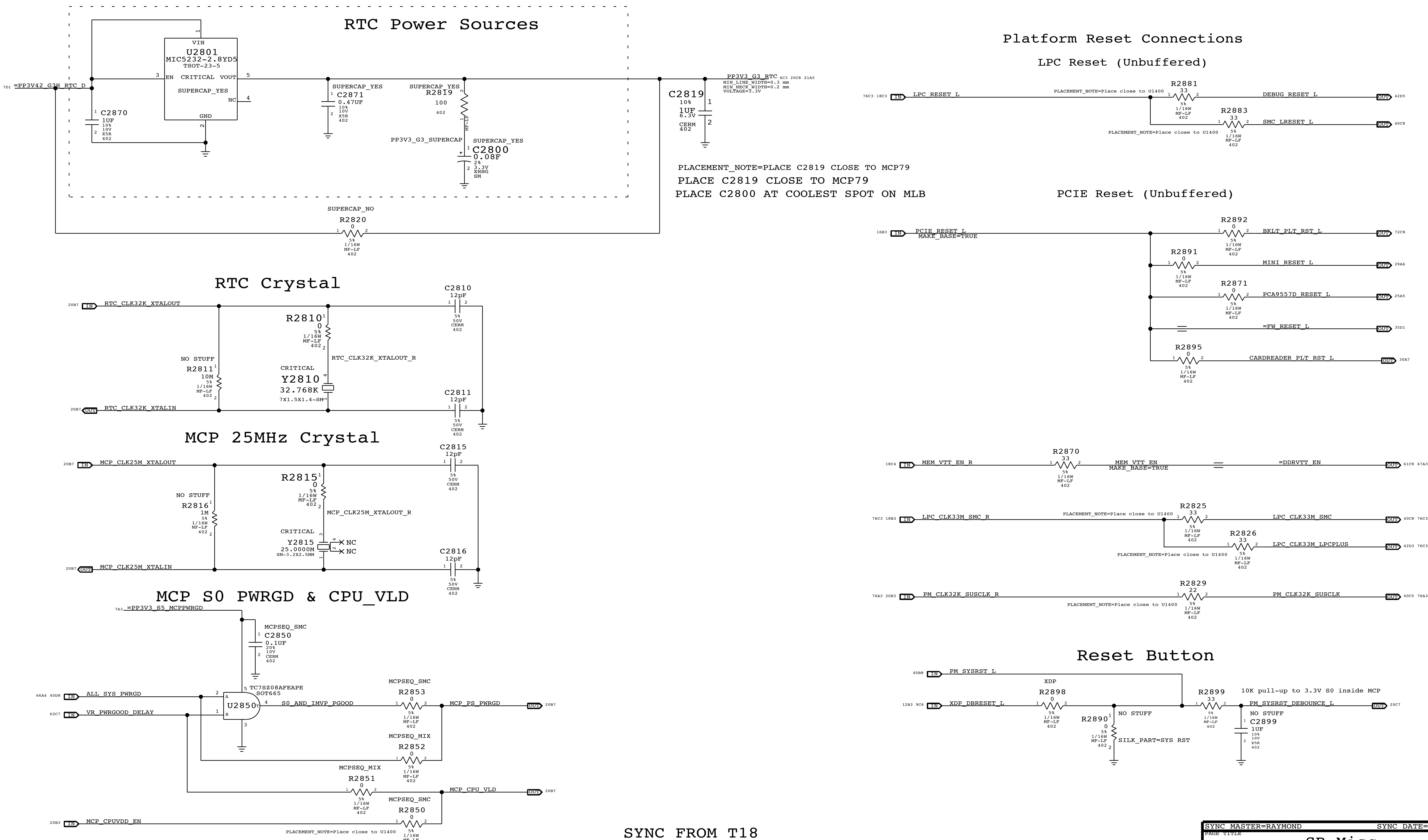
PAGE: 26 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

SYNC FROM T18
CHANGE RESET BUTTOM TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE Y2810 AND U2850 TO SMALLER PARTS

SYNC_MASTER=RAYMOND	SYNC_DATE=04/05/2008
PAGE TITLE: SB Misc	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
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	PAGE: 28 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

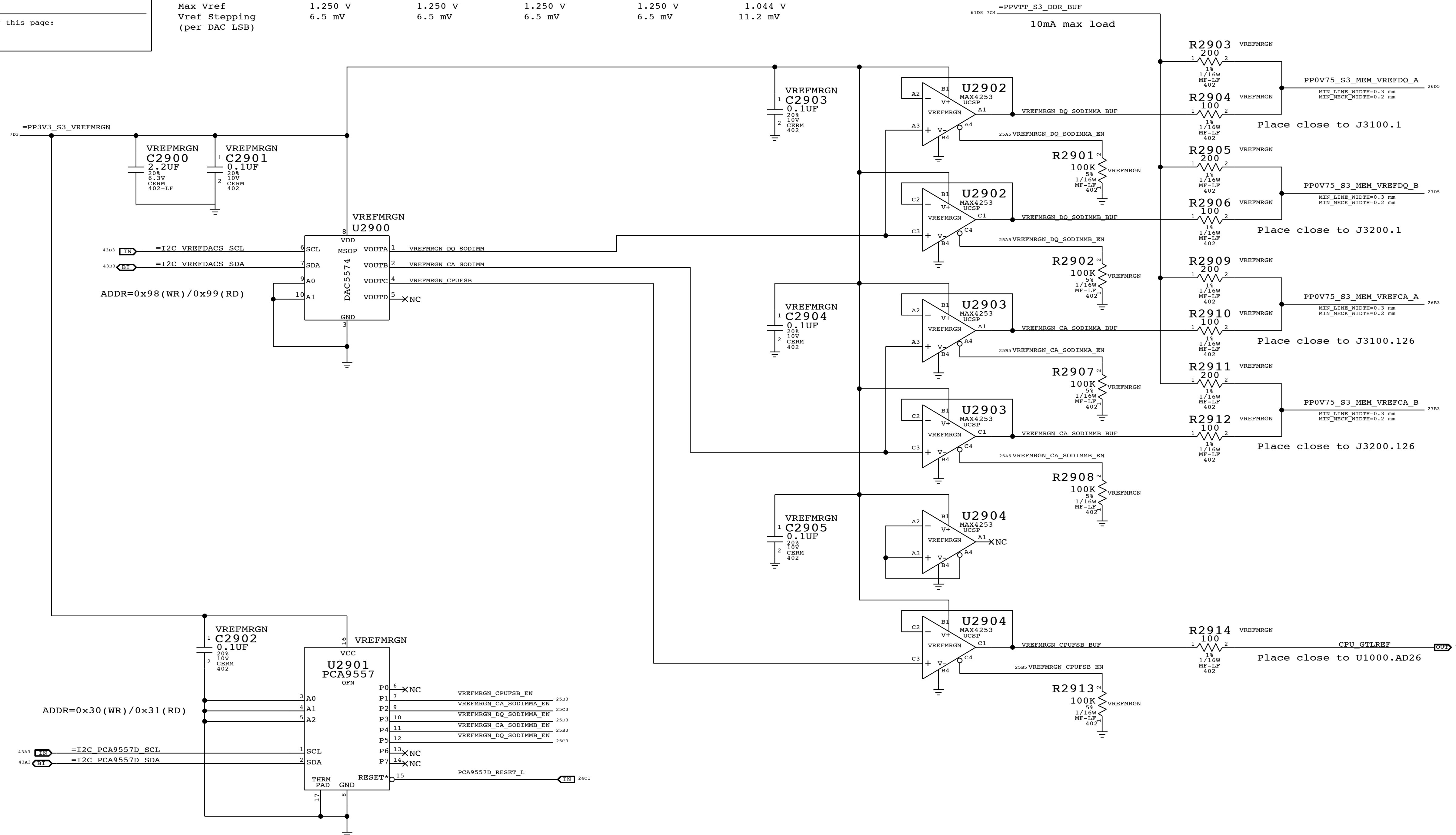
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

SYNC_MASTER=BEN SYNC_DATE=03/31/2008

PAGE TITLE
FSB/DDR3 Vref Margining

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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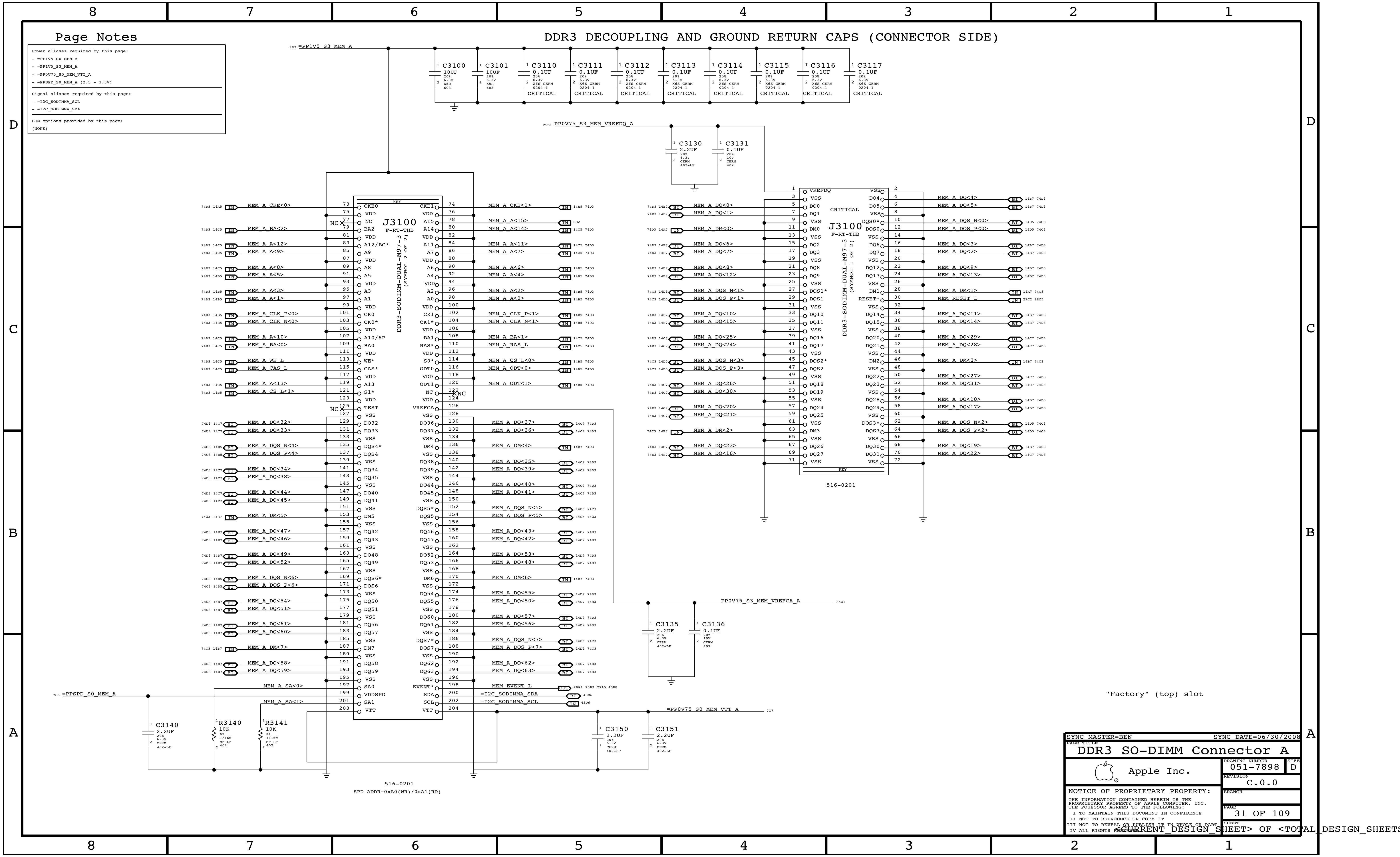

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)
Page Notes
Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)
Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA
BOM options provided by this page:
(NONE)
=PP1V5_S3_MEM_A
PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFCA_A
=PP0V75_S0_MEM_VTT_A
=PPSPD_S0_MEM_A
J3100
F-RT-THB
DDR3-SODIMM-DUAL-M97-3
(SYMBOL 1 OF 2)
(SYMBOL 2 OF 2)
CRITICAL
516-0201
SPD ADDR=0xA0(WR)/0xA1(RD)
"Factory" (top) slot
SYNC_MASTER=BEN
SYNC_DATE=06/30/2008
DDR3 SO-DIMM Connector A
Apple Inc.
051-7898
D
C.0.0
31 OF 109
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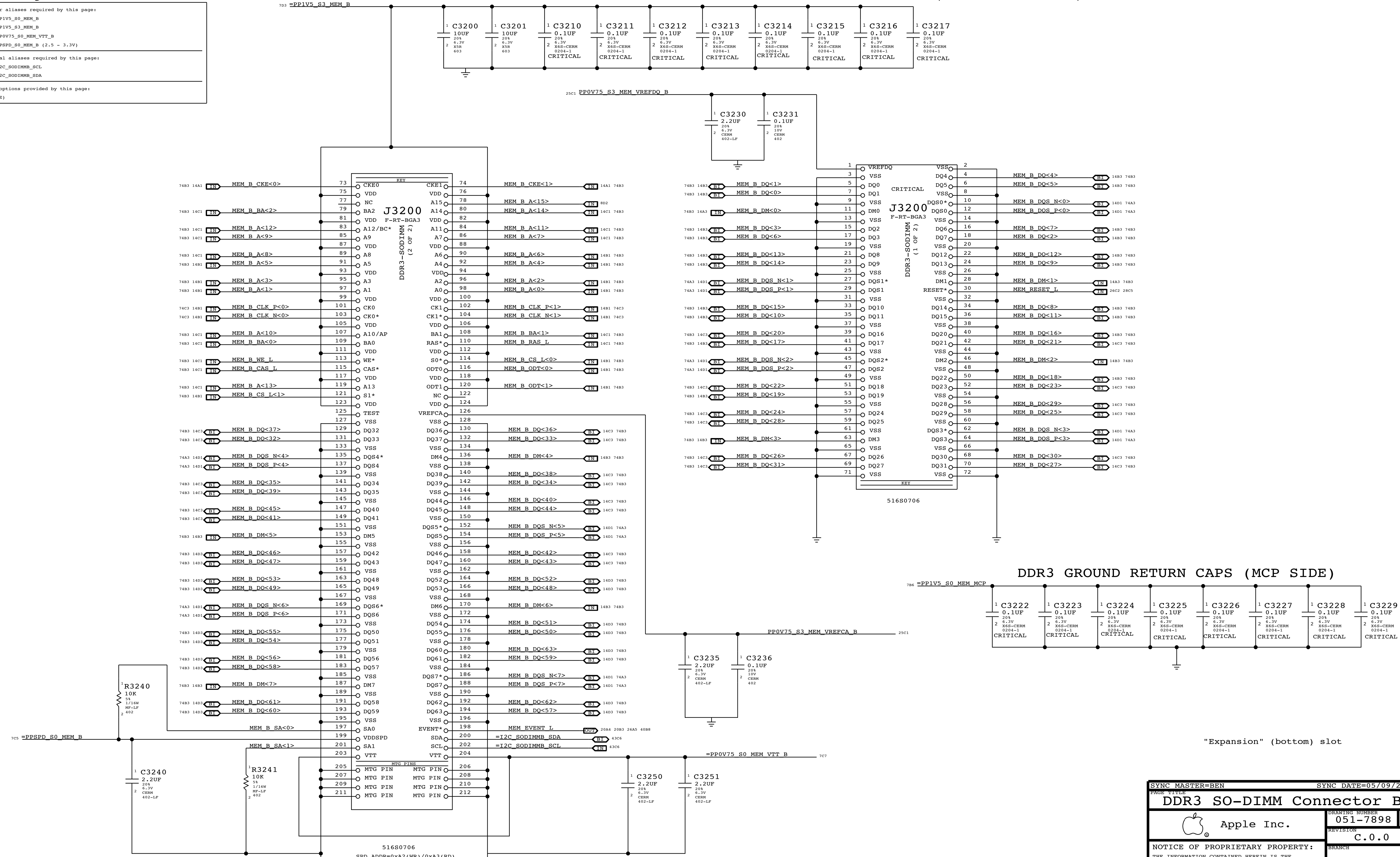
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



"Expansion" (bottom) slot

SYNC MASTER=BEN | SYNC DATE=05/09/2008

PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER: 051-7898 | SIZE: D

REVISION: C.0.0

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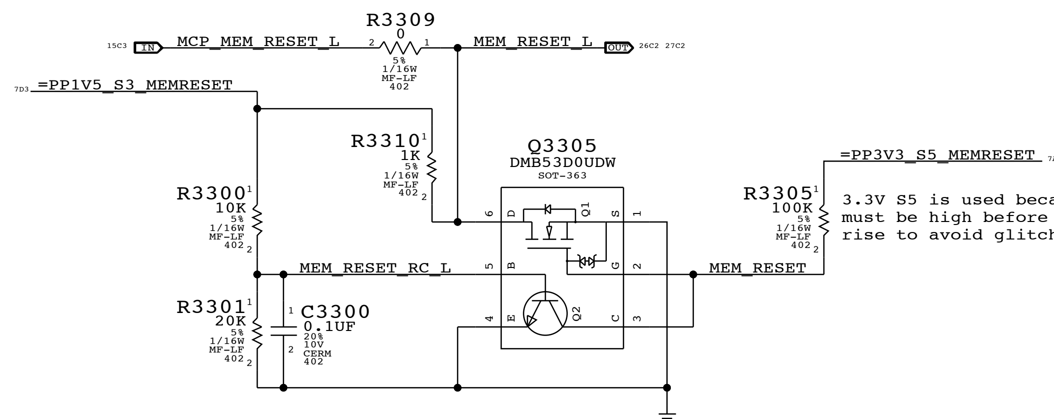
PAGE: 32 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

DDR3 RESET Support

Required becaues MCP79 does not meet DDR3 spec power-up reset timing requirement.



3.3V S5 is used because MEM_RESET must be high before 1.5V starts to rise to avoid glitch on MEM_RESET_L.

SYNC MASTER=T18 MLB | SYNC DATE=04/04/2008

PAGE TITLE

DDR3 Support

Apple Inc.

DRAWING NUMBER 051-7898 | SIZE D

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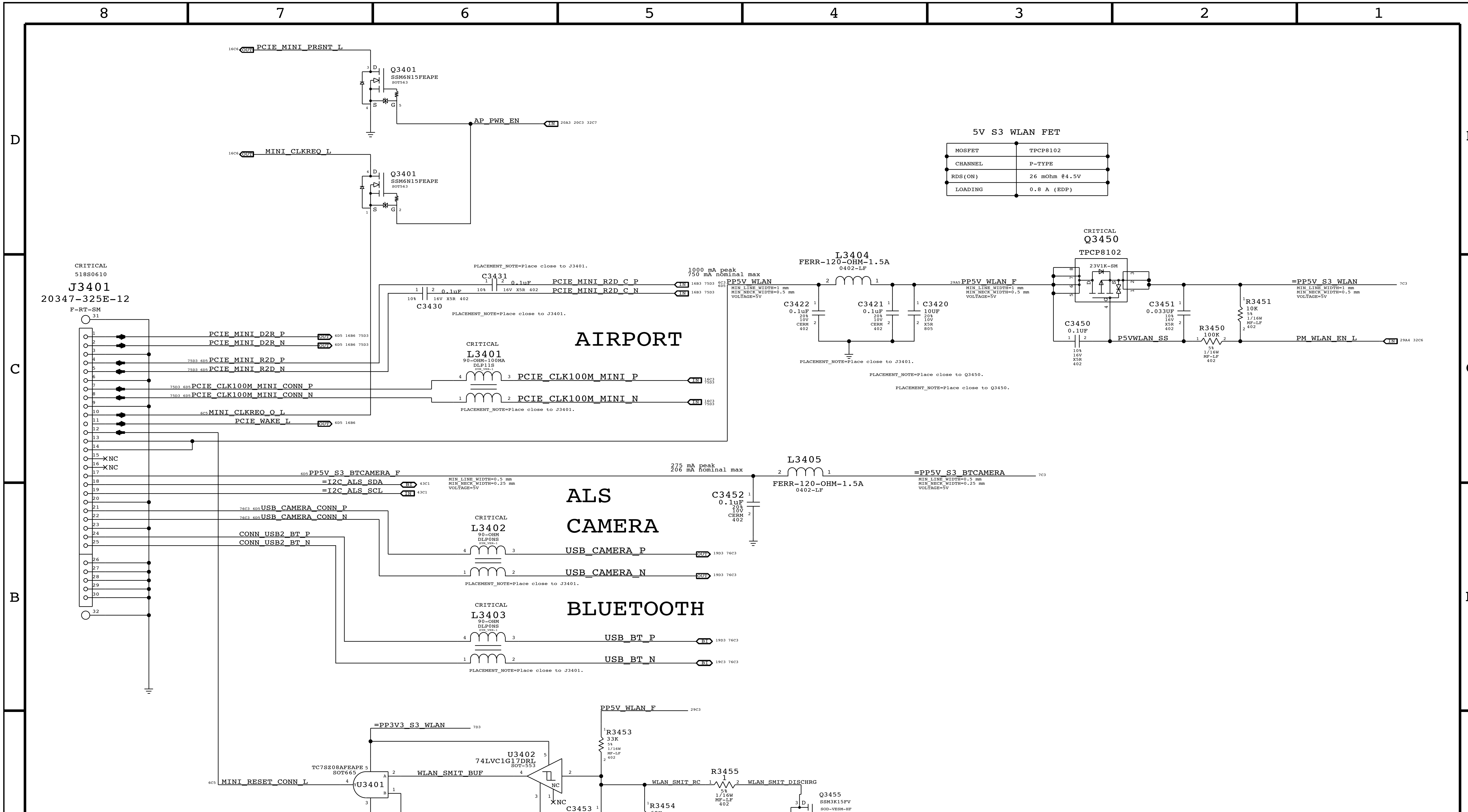
PAGE 33 OF 109

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



5V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

SYNC_MASTER=YITE SYNC_DATE=04/22/2008

PAGE TITLE
Right Clutch Connector

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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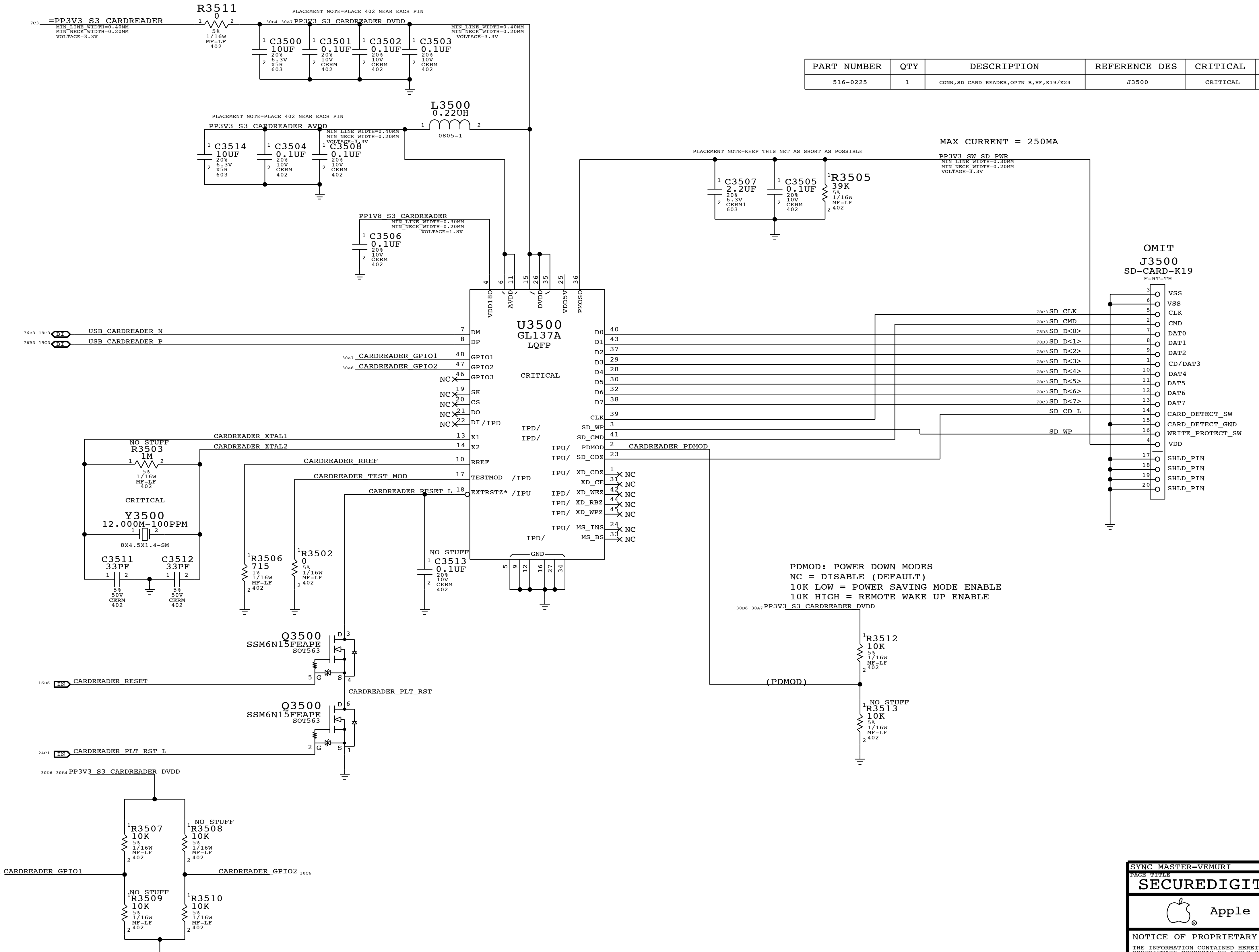
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
516-0225	1	CONN,SD CARD READER,OPTN B,HF,K19/K24	J3500	CRITICAL	



SYNC MASTER=VEMURI SYNC DATE=01/30/2009

PAGE TITLE

SECUREDIGITAL CARD READER

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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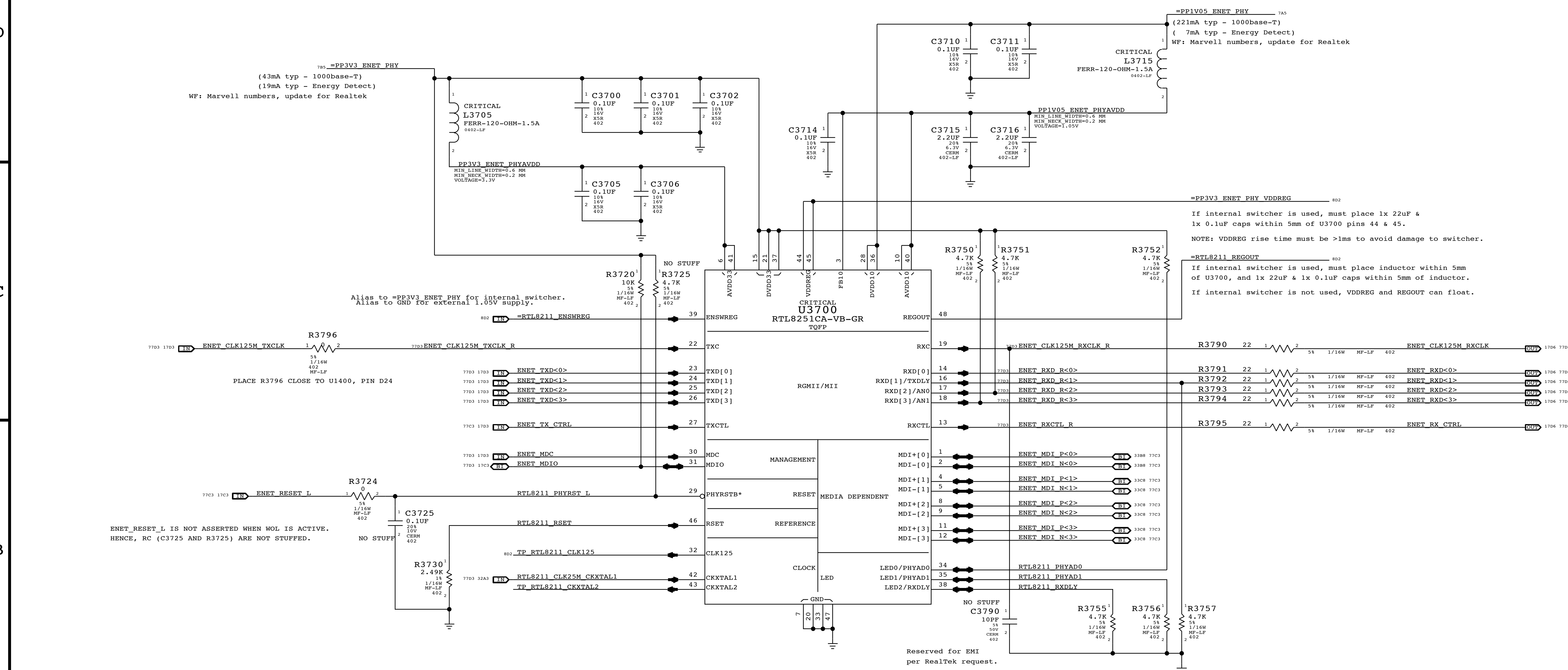
PAGE 35 OF 109

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

SYNC_MASTER=SUMA SYNC_DATE=05/23/2008

PAGE TITLE

Ethernet PHY (RTL8211CL)

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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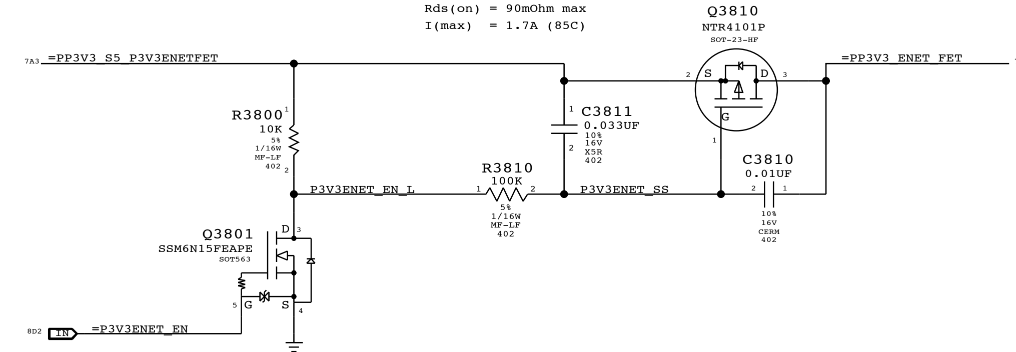
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)



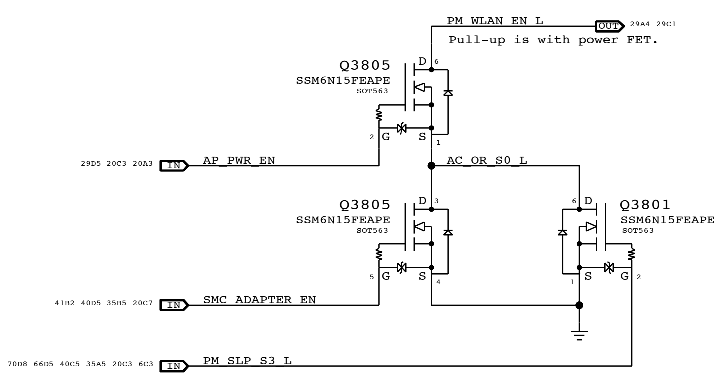
MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

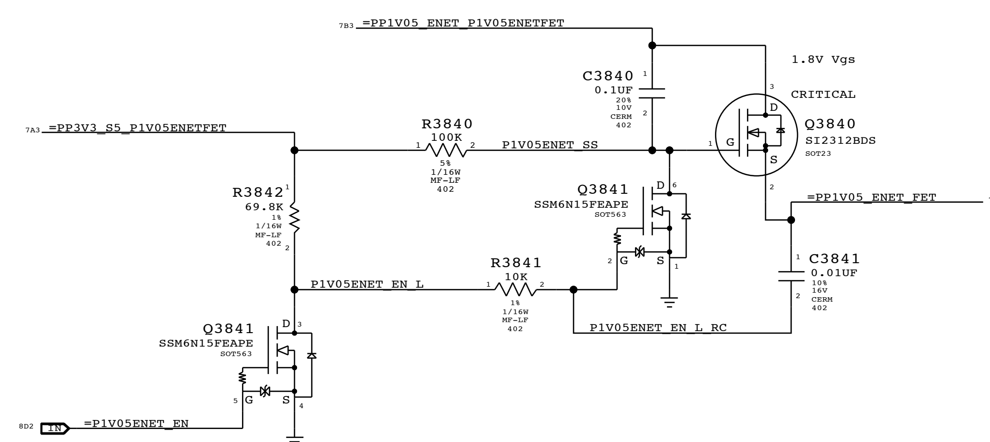
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



1.05V ENET FET

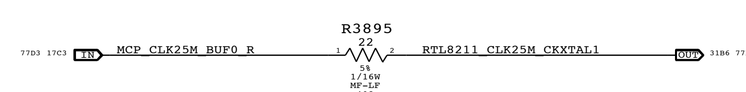


Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



SYNC_MASTER=SUMA SYNC_DATE=07/01/2008

PAGE TITLE: Ethernet & AirPort Support

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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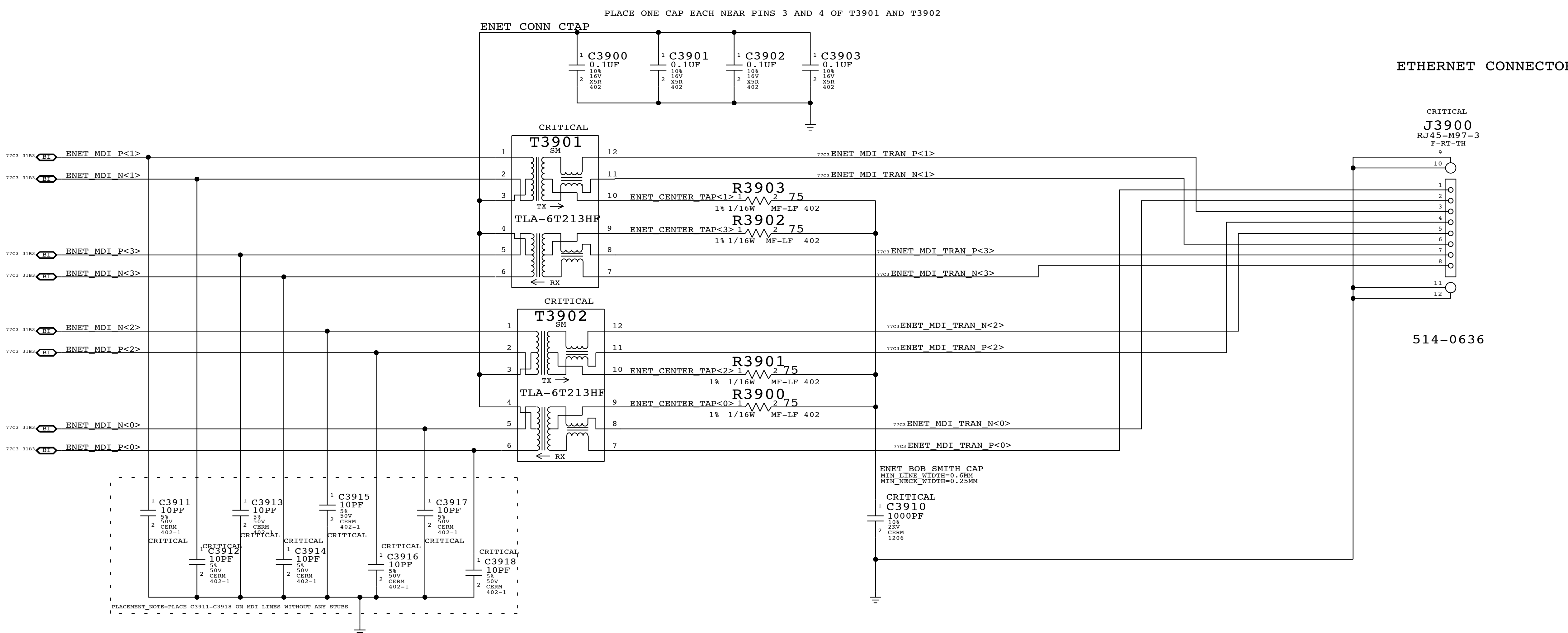
PAGE: 38 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

- COPY THIS PAGE FROM K36 CSA.39



SYNC_MASTER=SUMA SYNC_DATE=04/04/2008

PAGE TITLE

ETHERNET CONNECTOR

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

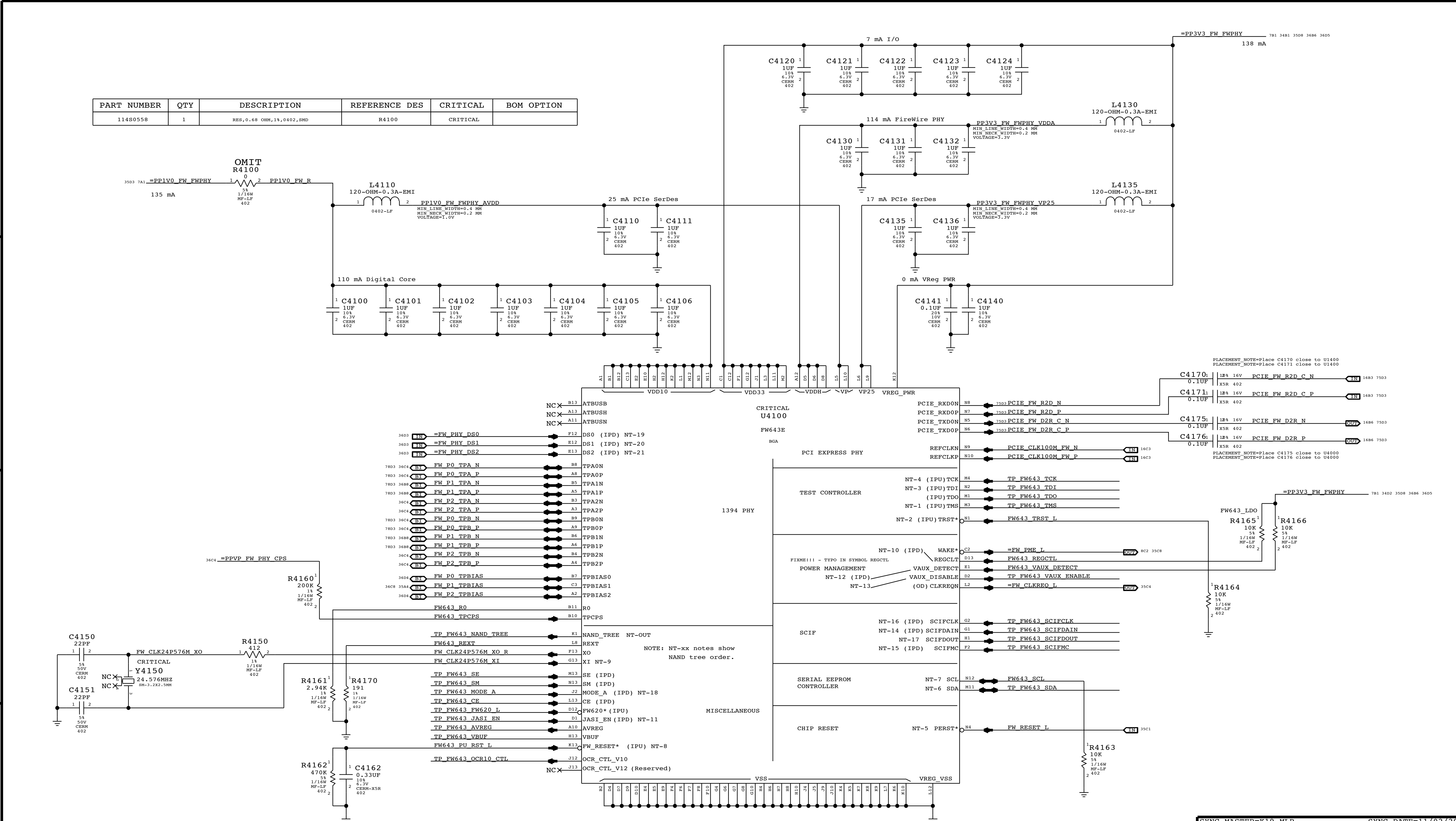
REVISION C.0.0

BRANCH

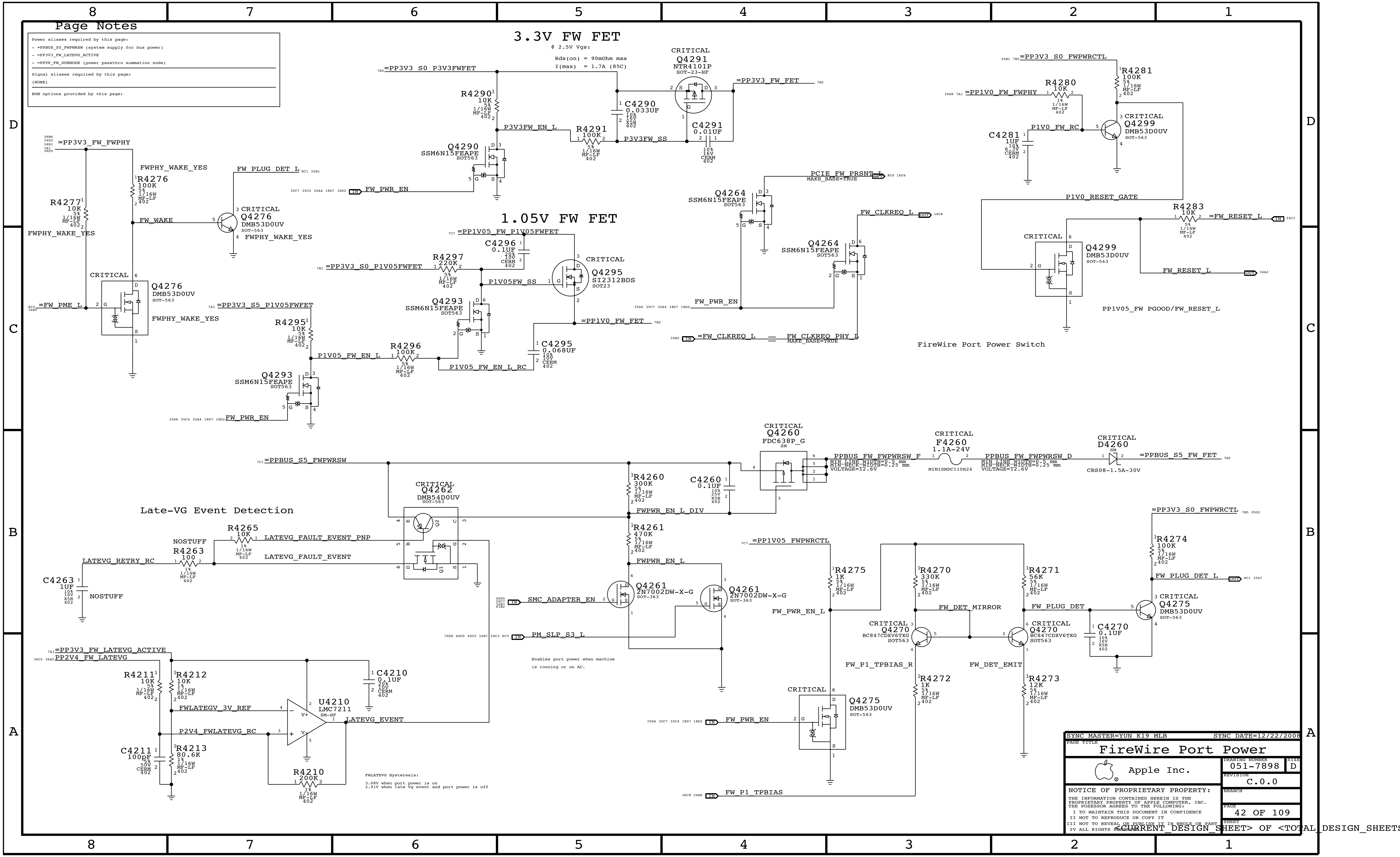
PAGE 39 OF 109

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0558	1	RES,0.68 OHM,1%,0402,SMD	R4100	CRITICAL	



SYNC_MASTER=K19_MLB	SYNC_DATE=11/02/2008
PAGE TITLE	FireWire LLC/PHY (FW643)
	Apple Inc.
DRAWING NUMBER	051-7898
SIZE	D
REVISION	C.0.0
BRANCH	
PAGE	41 OF 109
SHEET	<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



Page Notes
Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
3.3V FW FET
@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)
=PP3V3_S0_P3V3FWFET
CRITICAL
Q4291
NTR4101P
SOT-23-HF
=PP3V3_FW_FET
R4290
C4290
0.033UF
R4291
100K
P3V3FW_EN_L
P3V3FW_SS
C4291
0.01UF
Q4290
SSM6N15FEAPE
FW_PWR_EN
=PP3V3_FW_FWPHY
FWPHY_WAKE_YES
FW_PLUG_DET_L
R4276
100K
R4277
10K
FW_WAKE
CRITICAL
Q4276
DMB53D0UV
FWPHY_WAKE_YES
=FW_PME_L
1.05V FW FET
=PP1V05_FW_P1V05FWFET
C4296
0.1UF
R4297
220K
=PP3V3_S0_P1V05FWFET
P1V05FW_SS
Q4295
SI2312BDS
Q4293
SSM6N15FEAPE
=PP3V3_S5_P1V05FWFET
R4295
10K
=PP1V0_FW_FET
C4295
0.068UF
R4296
100K
P1V05_FW_EN_L
P1V05_FW_EN_L_RC
PCIE_FW_PRSNT_L
MAKE_BASE=TRUE
Q4264
SSM6N15FEAPE
FW_CLKREQ_L
=FW_CLKREQ_L
FW_CLKREQ_PHY_L
FireWire Port Power Switch
=PP3V3_S0_FWPWRCTL
R4281
100K
R4280
10K
=PP1V0_FW_FWPHY
CRITICAL
Q4299
DMB53D0UV
C4281
1UF
P1V0_FW_RC
P1V0_RESET_GATE
R4283
10K
=FW_RESET_L
FW_RESET_L
PP1V05_FW PGOOD/FW_RESET_L
CRITICAL
Q4260
FDC638P_G
=PPBUS_S5_FWPWRSW
PPBUS_FW_FWPWRSW_F
CRITICAL
F4260
1.1A-24V
MINISMDC110H24
PPBUS_FW_FWPWRSW_D
CRITICAL
D4260
CRS08-1.5A-30V
=PPBUS_S5_FW_FET
R4260
300K
C4260
0.1UF
FWPWR_EN_L_DIV
R4261
470K
FWPWR_EN_L
CRITICAL
Q4262
DMB54D0UV
Late-VG Event Detection
R4265
10K
LATEVG_FAULT_EVENT_PNP
NOSTUFF
R4263
100
LATEVG_FAULT_EVENT
LATEVG_RETRY_RC
C4263
1UF
NOSTUFF
Q4261
2N7002DW-X-G
SMC_ADAPTER_EN
PM_SLP_S3_L
Enables port power when machine is running or on AC.
=PP1V05_FWPWRCTL
R4275
1K
FW_PWR_EN_L
R4270
330K
R4271
56K
FW_DET_MIRROR
FW_PLUG_DET
CRITICAL
Q4270
BC847CDXV6TXG
FW_P1_TPBIAS_R
FW_DET_EMIT
R4272
1K
R4273
12K
C4270
0.1UF
=PP3V3_S0_FWPWRCTL
R4274
100K
FW_PLUG_DET_L
CRITICAL
Q4275
DMB53D0UV
CRITICAL
Q4275
DMB53D0UV
FW_PWR_EN
FW_P1_TPBIAS
=PP3V3_FW_LATEVG_ACTIVE
PP2V4_FW_LATEVG
R4211
10K
R4212
10K
C4210
0.1UF
FWLATEGV_3V_REF
U4210
LMC7211
P2V4_FWLATEVG_RC
LATEVG_EVENT
C4211
100PF
R4213
80.6K
R4210
200K
FWLATEVG Hysteresis:
3.08V when port power is on
2.91V when late Vg event and port power is off
SYNC_MASTER=YUN_K19_MLB
SYNC_DATE=12/22/2008
PAGE TITLE
FireWire Port Power
Apple Inc.
DRAWING NUMBER
051-7898
SIZE
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REVISION
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<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>
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Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

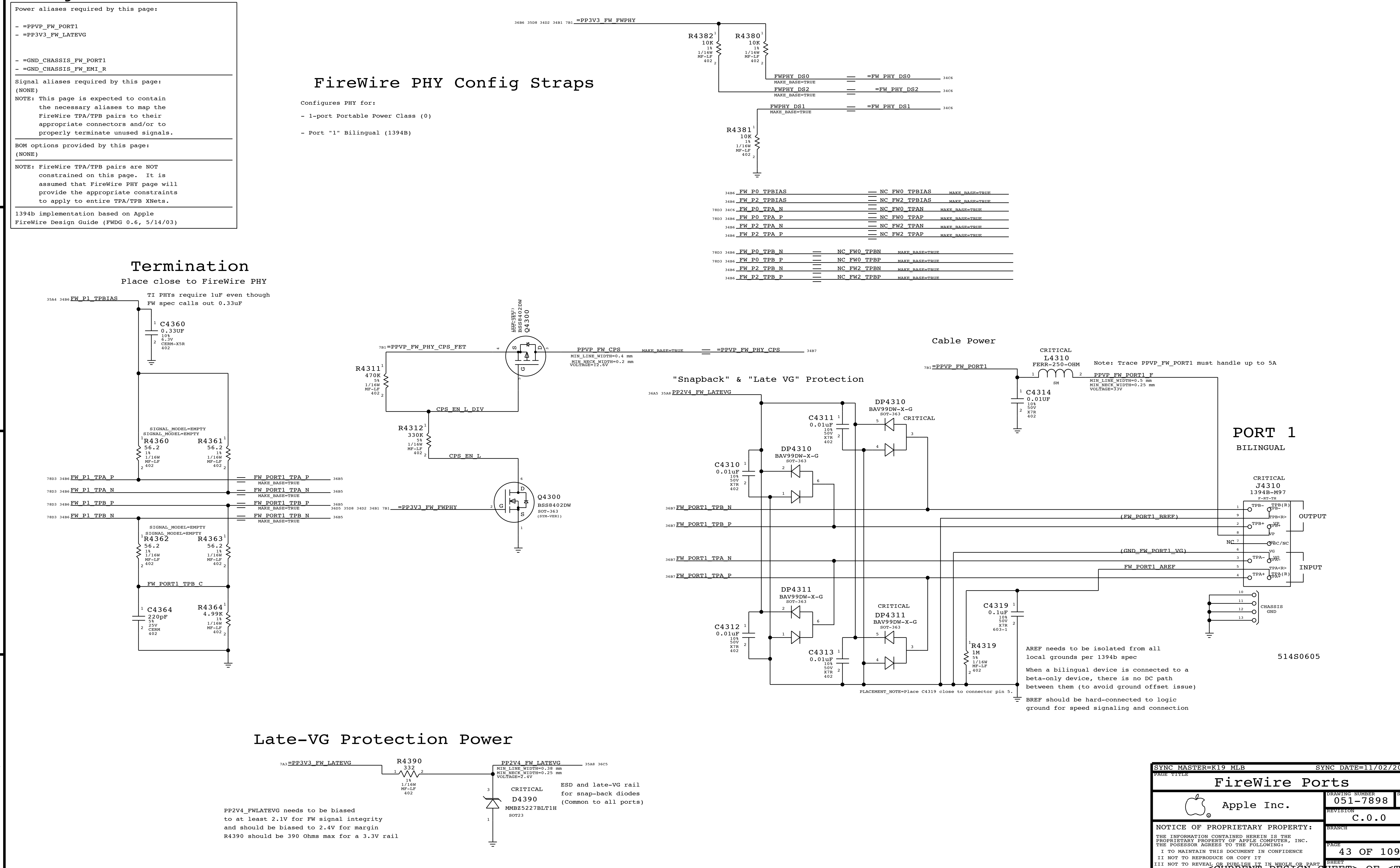
Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)



SYNC_MASTER=K19_MLB SYNC_DATE=11/02/2008

PAGE TITLE: FireWire Ports

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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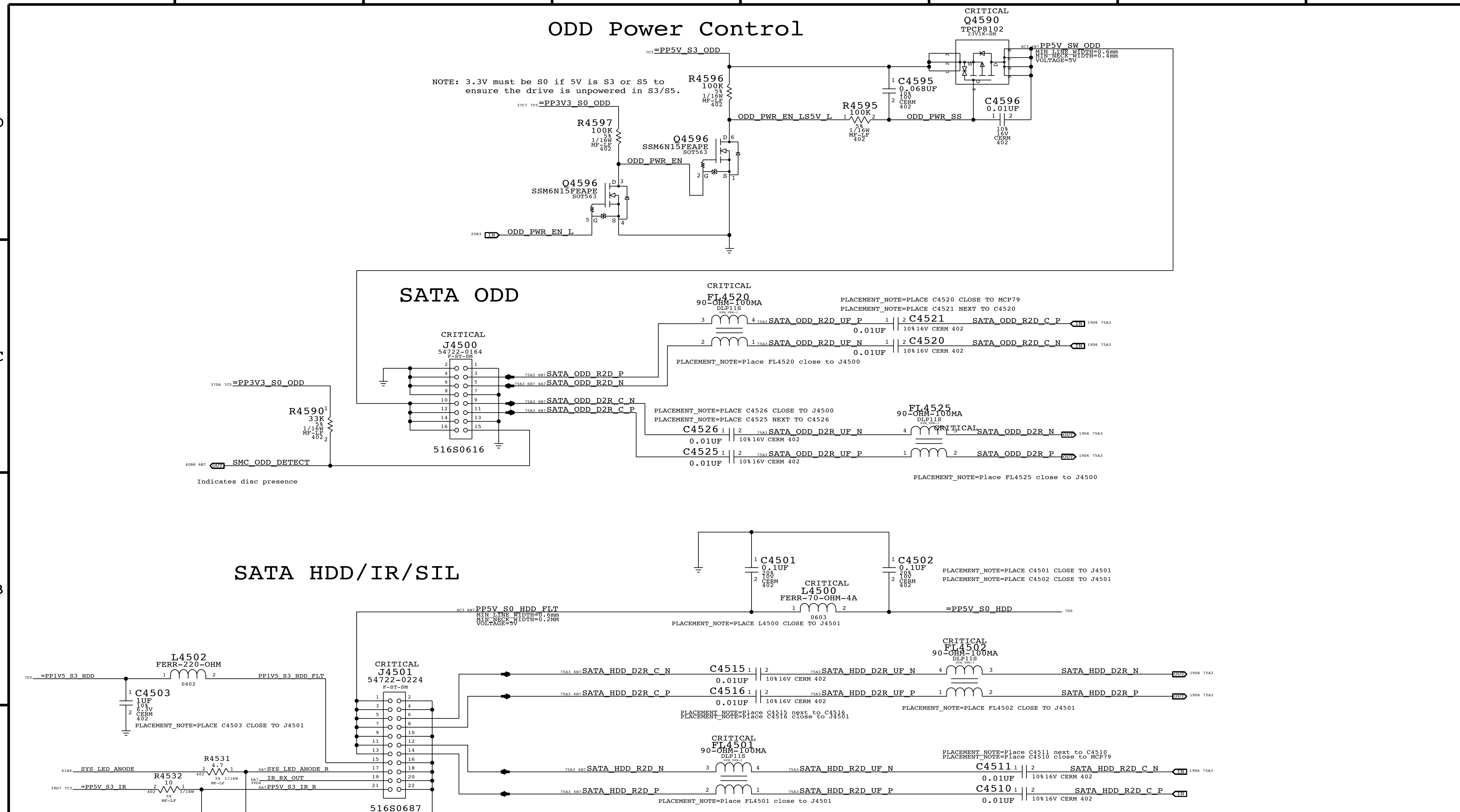
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K19_MLB SYNC_DATE=12/04/2008

PAGE TITLE
SATA Connectors

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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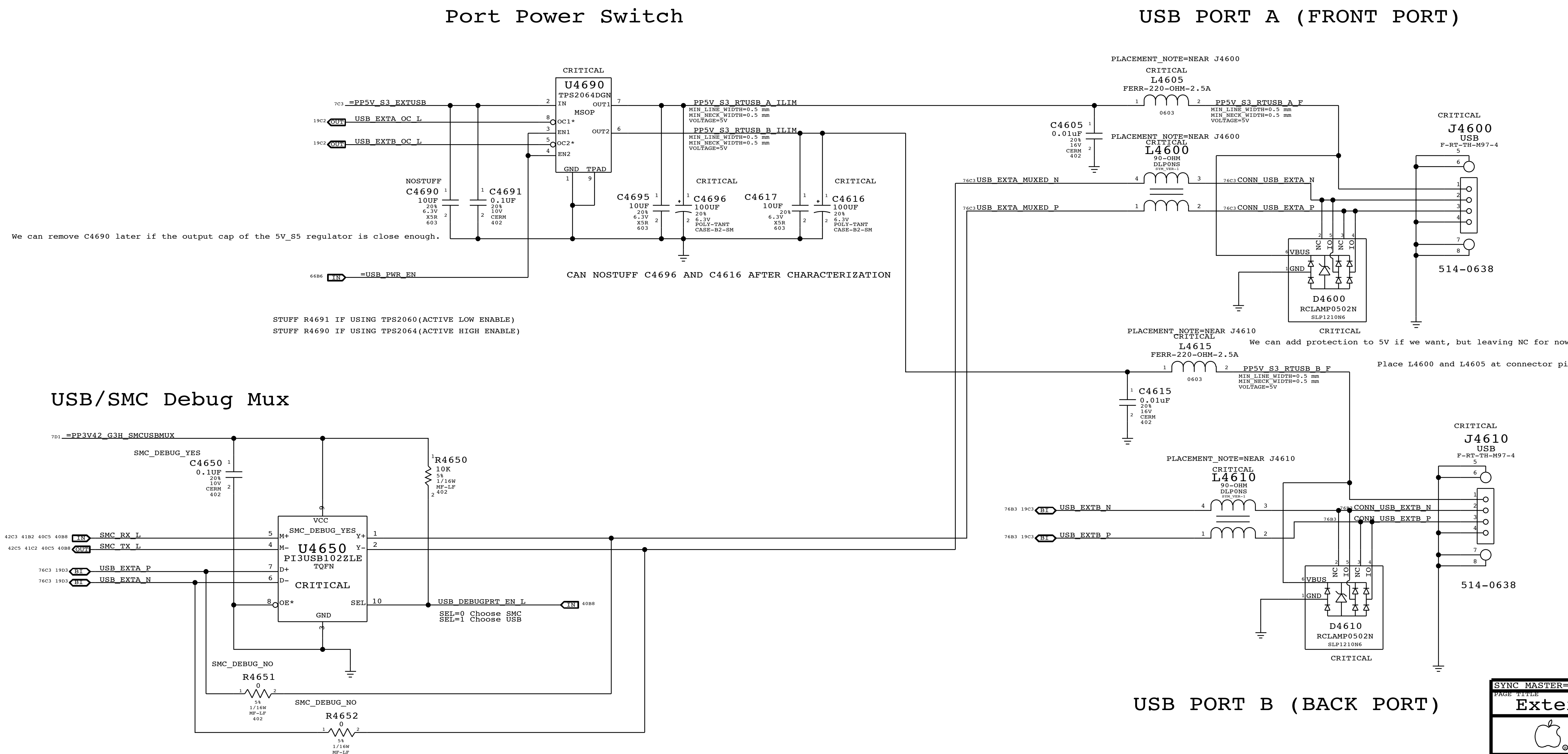
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=YUAN.MA SYNC_DATE=01/18/2008

PAGE TITLE

External USB Connectors

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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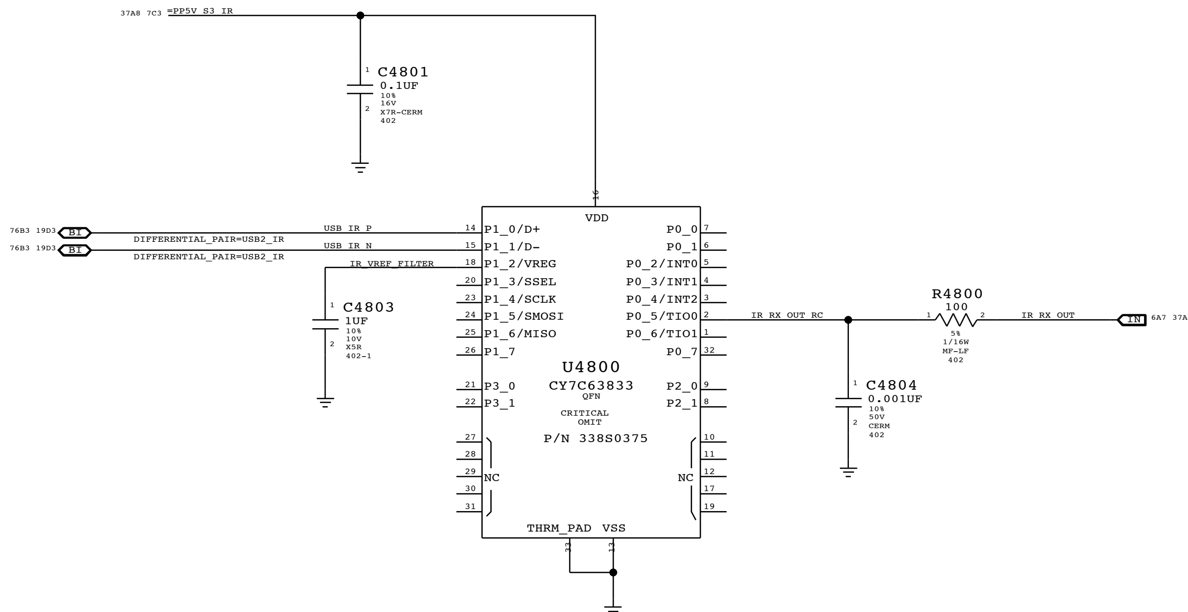

CYPRESS 'ENCORE II' USB CONTROLLER

SYNC MASTER=YUAN.MA SYNC DATE=05/28/2008

PAGE TITLE

Front Flex Support

Apple Inc.

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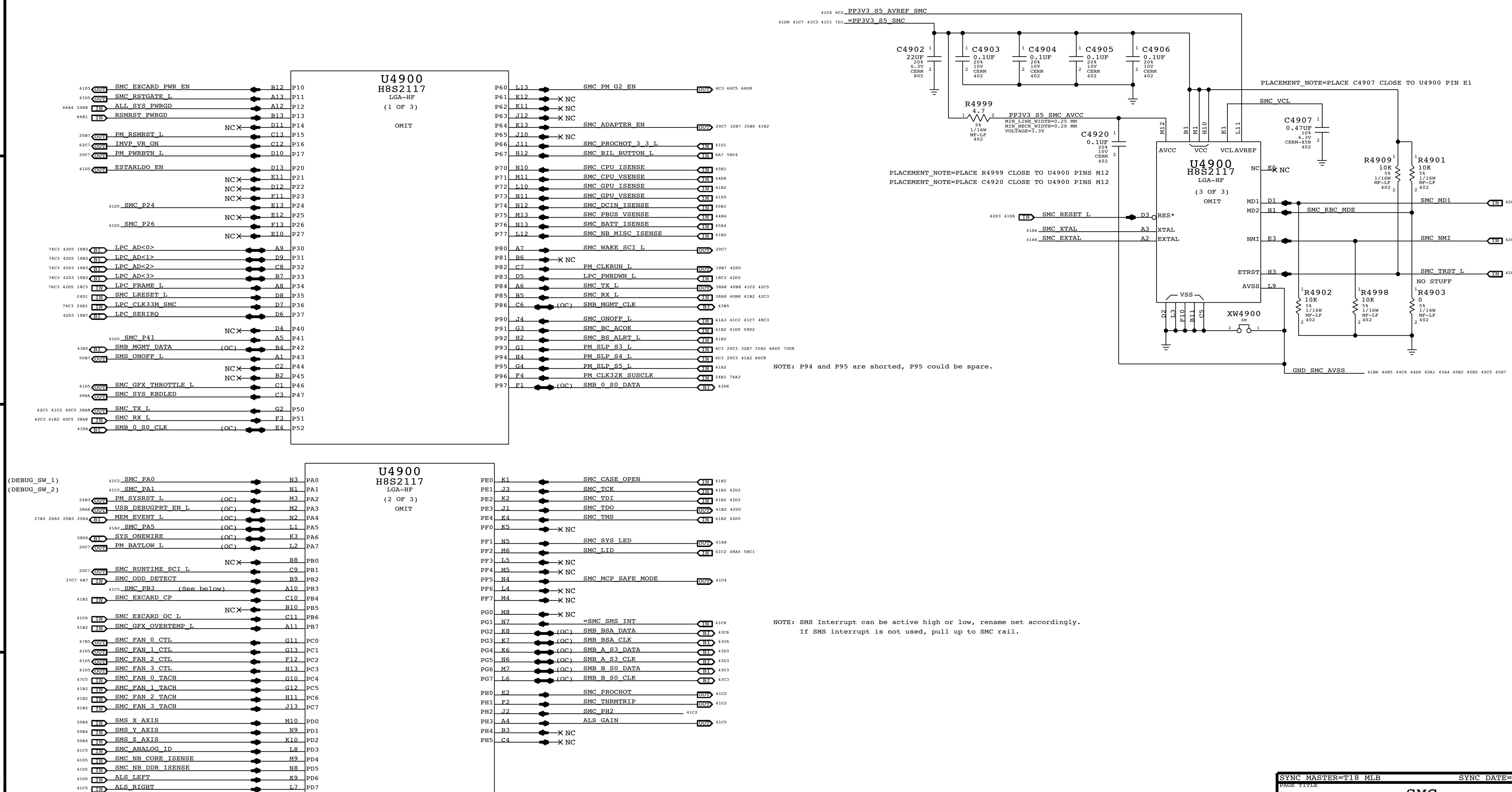
NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SYNC_MASTER=T18_MLB SYNC_DATE=06/26/2008

PAGE TITLE
SMC

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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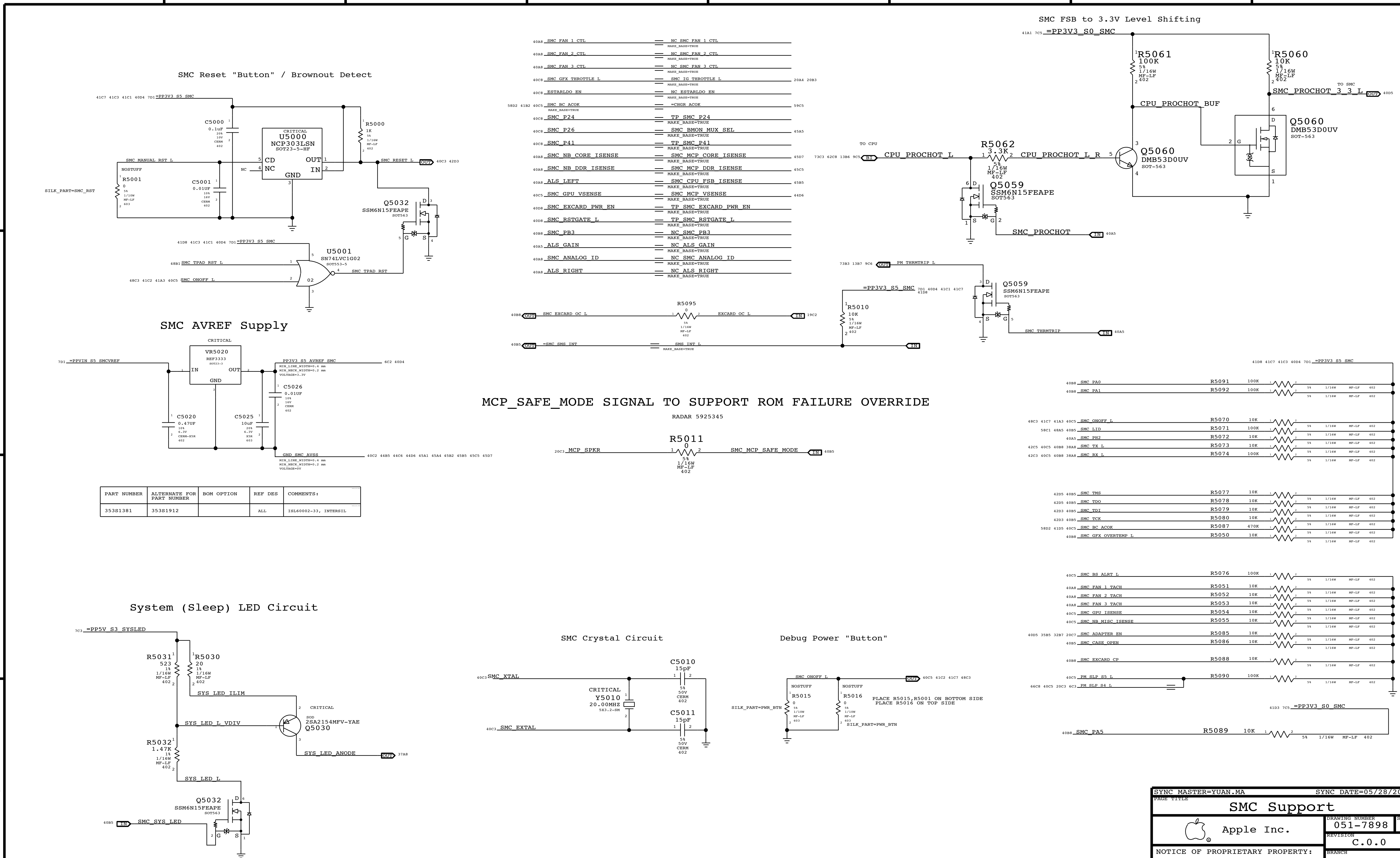
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	ISL60002-33, INTERSIL

SYNC_MASTER=YUAN_MA SYNC_DATE=05/28/2008

PAGE TITLE

SMC Support

Apple Inc.

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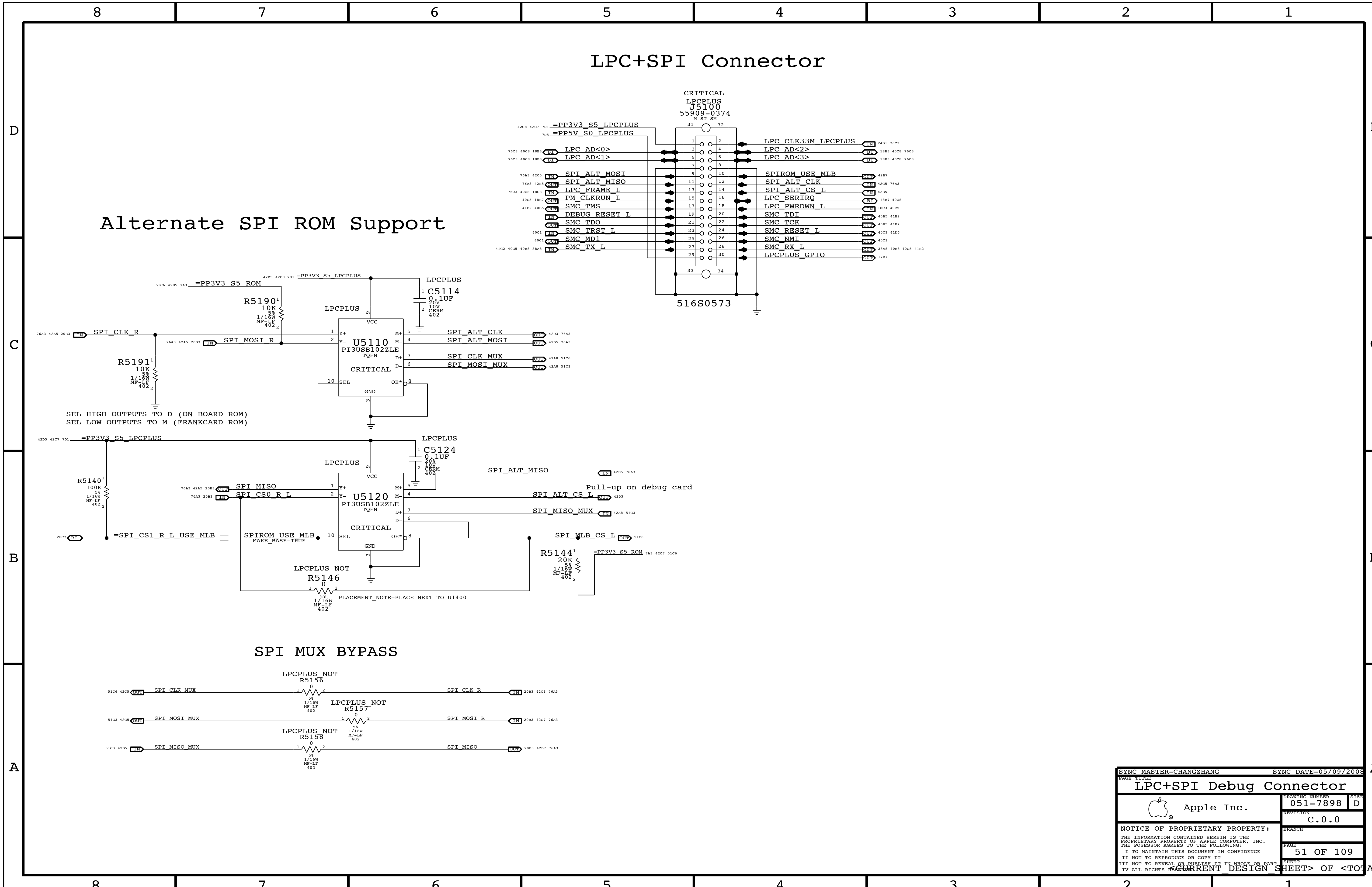
LPC+SPI Connector
CRITICAL
LPCPLUS
J5100
55909-0374
M-ST-SM
=PP3V3_S5_LPCPLUS
=PP5V_S0_LPCPLUS
LPC_AD<0>
LPC_AD<1>
SPI_ALT_MOSI
SPI_ALT_MISO
LPC_FRAME_L
PM_CLKRUN_L
SMC_TMS
DEBUG_RESET_L
SMC_TDO
SMC_TRST_L
SMC_MD1
SMC_TX_L
LPC_CLK33M_LPCPLUS
LPC_AD<2>
LPC_AD<3>
SPIROM_USE_MLB
SPI_ALT_CLK
SPI_ALT_CS_L
LPC_SERIRQ
LPC_PWRDWN_L
SMC_TDI
SMC_TCK
SMC_RESET_L
SMC_NMI
SMC_RX_L
LPCPLUS_GPIO
516S0573
Alternate SPI ROM Support
=PP3V3_S5_ROM
R5190
10K
5%
1/16W
MF-LF
402
SPI_CLK_R
SPI_MOSI_R
R5191
10K
LPCPLUS
U5110
PI3USB102ZLE
TQFN
CRITICAL
C5114
0.1UF
20%
10V
CERM
402
SPI_ALT_CLK
SPI_ALT_MOSI
SPI_CLK_MUX
SPI_MOSI_MUX
SEL HIGH OUTPUTS TO D (ON BOARD ROM)
SEL LOW OUTPUTS TO M (FRANKCARD ROM)
=PP3V3_S5_LPCPLUS
R5140
100K
C5124
0.1UF
U5120
PI3USB102ZLE
TQFN
CRITICAL
SPI_MISO
SPI_CS0_R_L
SPI_ALT_MISO
Pull-up on debug card
SPI_ALT_CS_L
SPI_MISO_MUX
SPI_MLB_CS_L
=SPI_CS1_R_L_USE_MLB
SPIROM_USE_MLB
MAKE_BASE=TRUE
R5144
20K
=PP3V3_S5_ROM
LPCPLUS_NOT
R5146
0
PLACEMENT_NOTE=PLACE NEXT TO U1400
SPI MUX BYPASS
LPCPLUS_NOT
R5156
SPI_CLK_MUX
SPI_CLK_R
LPCPLUS_NOT
R5157
SPI_MOSI_MUX
SPI_MOSI_R
LPCPLUS_NOT
R5158
SPI_MISO_MUX
SPI_MISO
SYNC_MASTER=CHANGZHANG
SYNC_DATE=05/09/2008
PAGE TITLE
LPC+SPI Debug Connector
Apple Inc.
DRAWING NUMBER
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<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>
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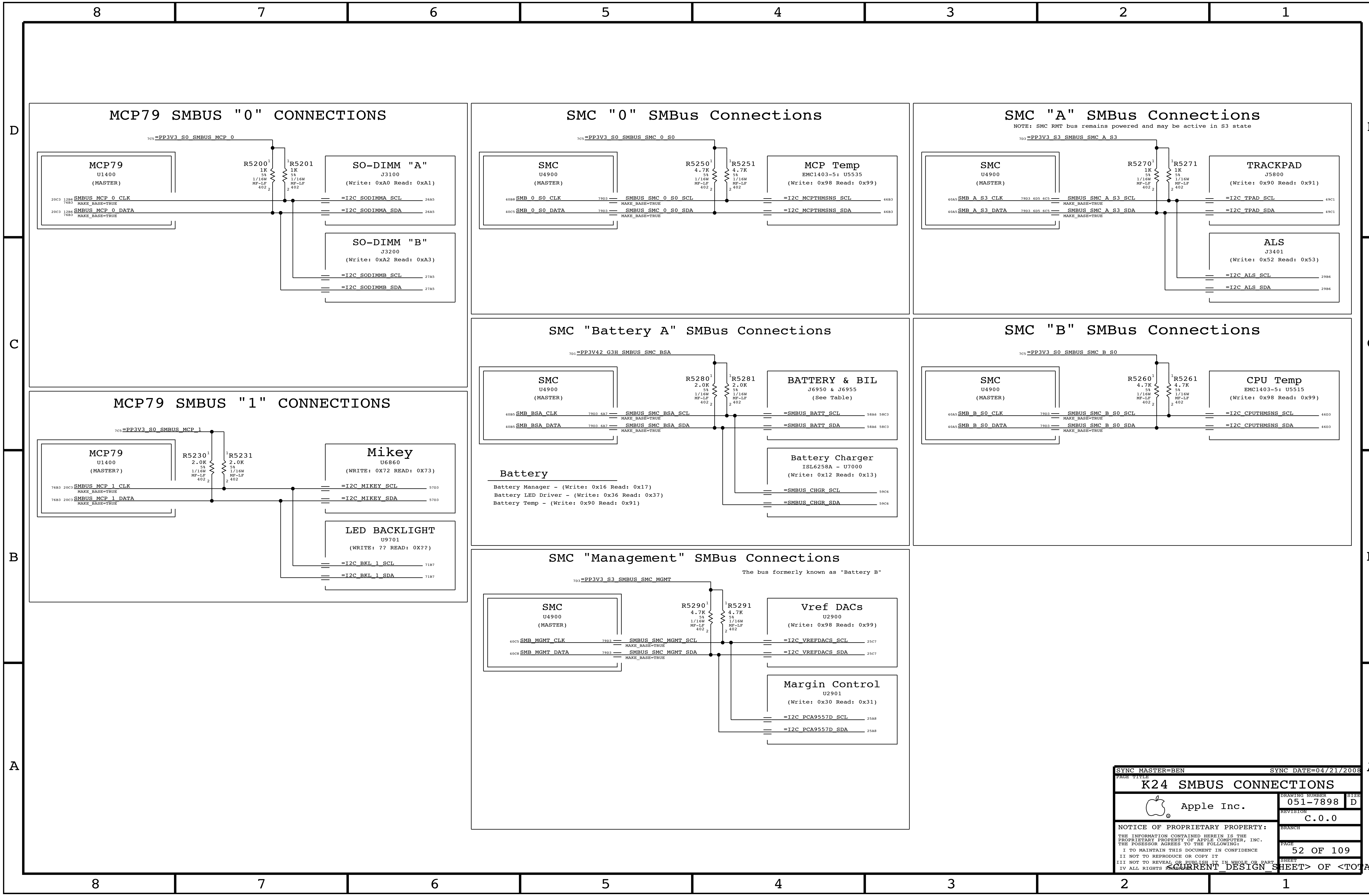
MCP79 SMBUS "0" CONNECTIONS
=PP3V3_S0_SMBUS_MCP_0
MCP79
U1400
(MASTER)
SMBUS_MCP_0_CLK
SMBUS_MCP_0_DATA
MAKE_BASE=TRUE
R5200
1K
R5201
1K
5%
1/16W
MF-LF
402
SO-DIMM "A"
J3100
(Write: 0xA0 Read: 0xA1)
=I2C_SODIMMA_SCL
=I2C_SODIMMA_SDA
SO-DIMM "B"
J3200
(Write: 0xA2 Read: 0xA3)
=I2C_SODIMMB_SCL
=I2C_SODIMMB_SDA
SMC "0" SMBus Connections
=PP3V3_S0_SMBUS_SMC_0_S0
SMC
U4900
(MASTER)
SMB_0_S0_CLK
SMB_0_S0_DATA
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA
R5250
4.7K
R5251
4.7K
MCP Temp
EMC1403-5: U5535
(Write: 0x98 Read: 0x99)
=I2C_MCPTHMSNS_SCL
=I2C_MCPTHMSNS_SDA
SMC "A" SMBus Connections
NOTE: SMC RMT bus remains powered and may be active in S3 state
=PP3V3_S3_SMBUS_SMC_A_S3
SMC
U4900
(MASTER)
SMB_A_S3_CLK
SMB_A_S3_DATA
SMBUS_SMC_A_S3_SCL
SMBUS_SMC_A_S3_SDA
R5270
1K
R5271
1K
TRACKPAD
J5800
(Write: 0x90 Read: 0x91)
=I2C_TPAD_SCL
=I2C_TPAD_SDA
ALS
J3401
(Write: 0x52 Read: 0x53)
=I2C_ALS_SCL
=I2C_ALS_SDA
SMC "Battery A" SMBus Connections
=PP3V42_G3H_SMBUS_SMC_BSA
SMC
U4900
(MASTER)
SMB_BSA_CLK
SMB_BSA_DATA
SMBUS_SMC_BSA_SCL
SMBUS_SMC_BSA_SDA
R5280
2.0K
R5281
2.0K
BATTERY & BIL
J6950 & J6955
(See Table)
=SMBUS_BATT_SCL
=SMBUS_BATT_SDA
Battery Charger
ISL6258A - U7000
(Write: 0x12 Read: 0x13)
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA
Battery
Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)
SMC "B" SMBus Connections
=PP3V3_S0_SMBUS_SMC_B_S0
SMC
U4900
(MASTER)
SMB_B_S0_CLK
SMB_B_S0_DATA
SMBUS_SMC_B_S0_SCL
SMBUS_SMC_B_S0_SDA
R5260
4.7K
R5261
4.7K
CPU Temp
EMC1403-5: U5515
(Write: 0x98 Read: 0x99)
=I2C_CPUTHMSNS_SCL
=I2C_CPUTHMSNS_SDA
MCP79 SMBUS "1" CONNECTIONS
=PP3V3_S0_SMBUS_MCP_1
MCP79
U1400
(MASTER?)
SMBUS_MCP_1_CLK
SMBUS_MCP_1_DATA
R5230
2.0K
R5231
2.0K
Mikey
U6860
(WRITE: 0X72 READ: 0X73)
=I2C_MIKEY_SCL
=I2C_MIKEY_SDA
LED BACKLIGHT
U9701
(WRITE: ?? READ: 0X??)
=I2C_BKL_1_SCL
=I2C_BKL_1_SDA
SMC "Management" SMBus Connections
The bus formerly known as "Battery B"
=PP3V3_S3_SMBUS_SMC_MGMT
SMC
U4900
(MASTER)
SMB_MGMT_CLK
SMB_MGMT_DATA
SMBUS_SMC_MGMT_SCL
SMBUS_SMC_MGMT_SDA
R5290
4.7K
R5291
4.7K
Vref DACs
U2900
(Write: 0x98 Read: 0x99)
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA
Margin Control
U2901
(Write: 0x30 Read: 0x31)
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA
SYNC_MASTER=BEN
SYNC_DATE=04/21/2008
PAGE TITLE
K24 SMBUS CONNECTIONS
Apple Inc.
DRAWING NUMBER
051-7898
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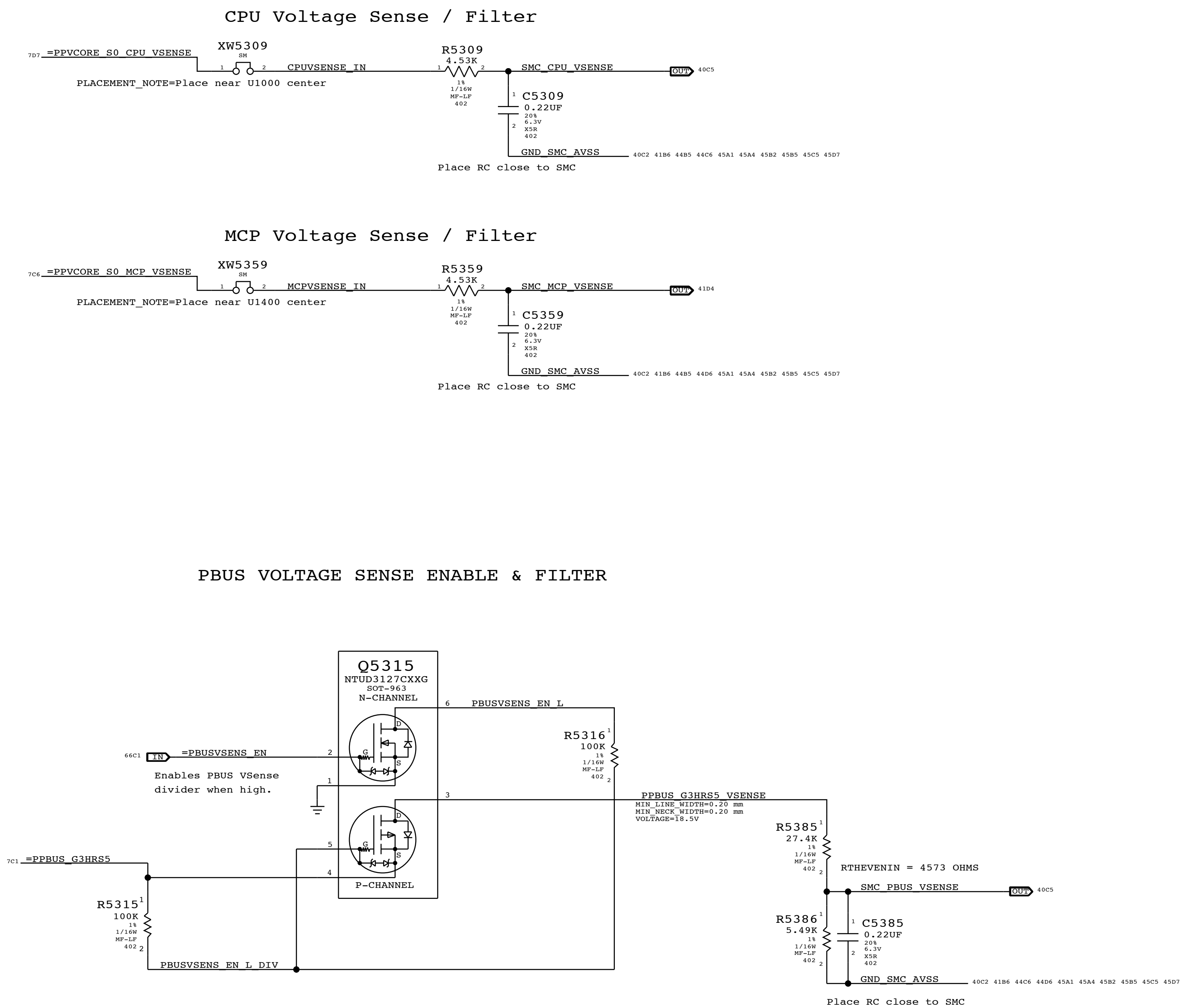

SYNC_MASTER=YUNWU SYNC_DATE=02/04/2008

PAGE TITLE

VOLTAGE SENSING

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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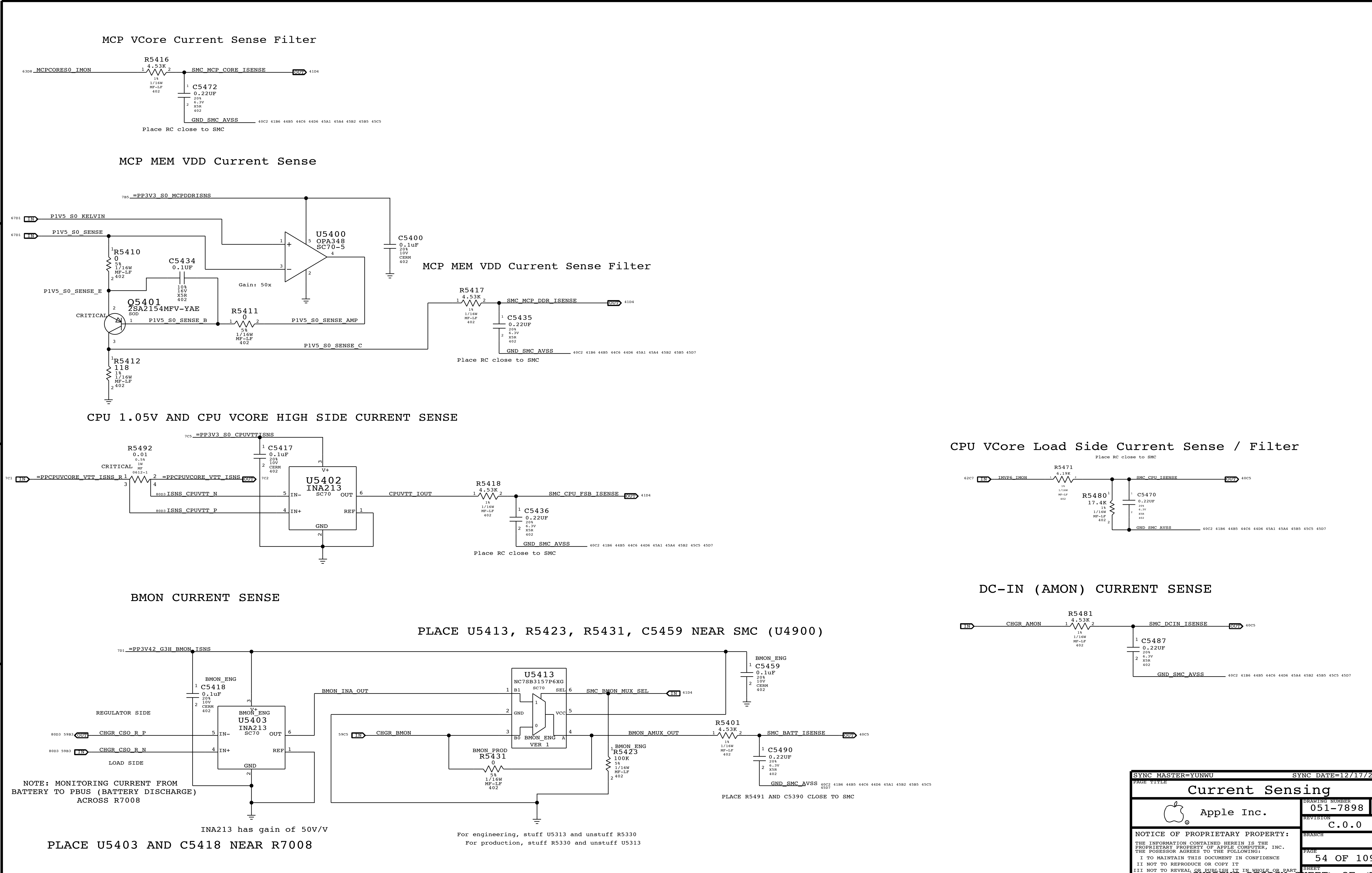

SYNC_MASTER=YUNWU SYNC_DATE=12/17/2008

PAGE TITLE

Current Sensing

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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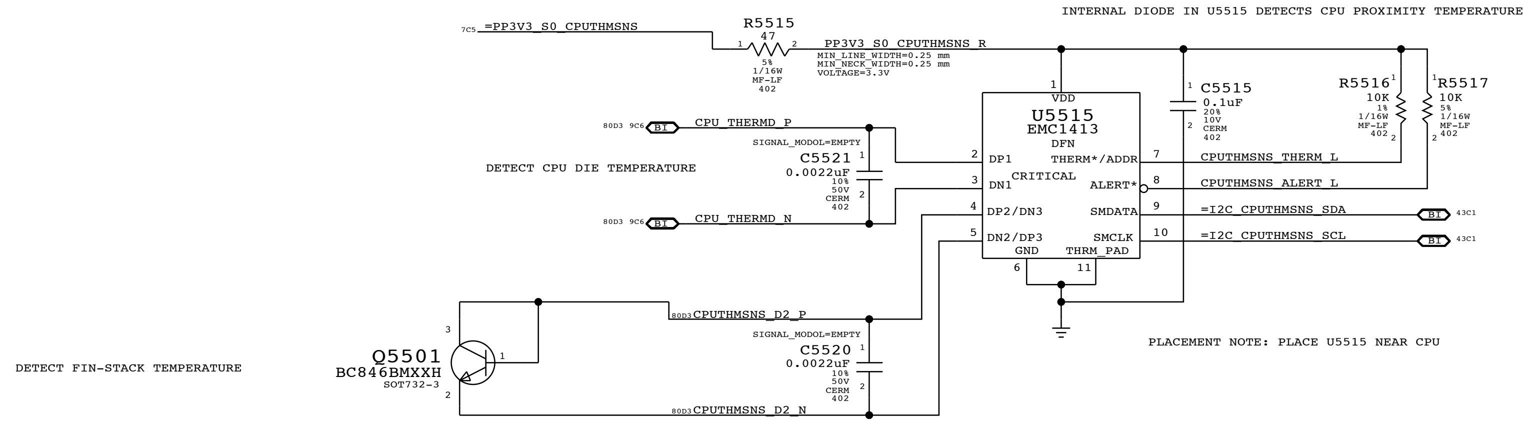
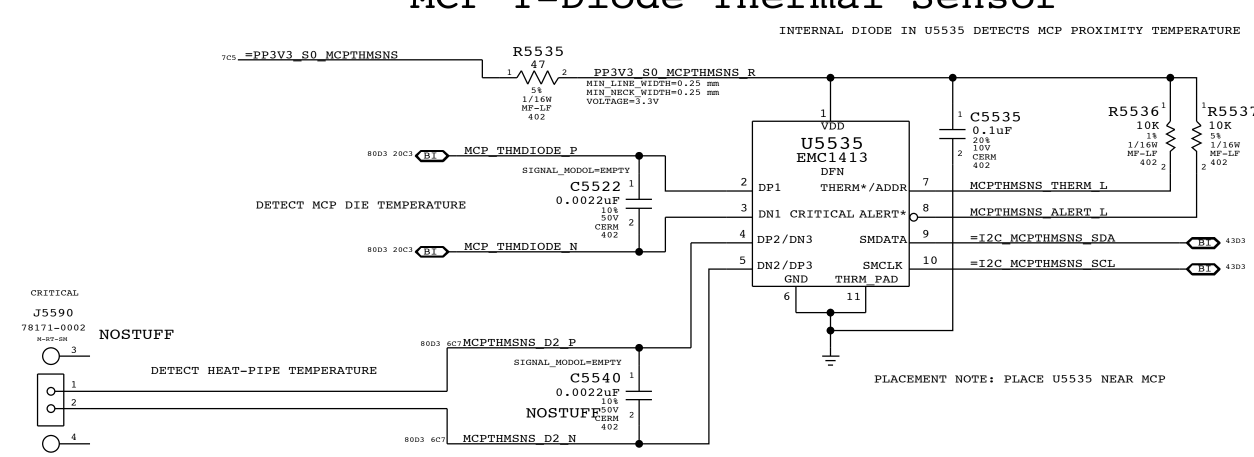
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



REPLACED 518S0521 WITH 518S0519

SYNC_MASTER=YUNWU SYNC_DATE=03/20/2008

PAGE TITLE
Thermal Sensors

Apple Inc.

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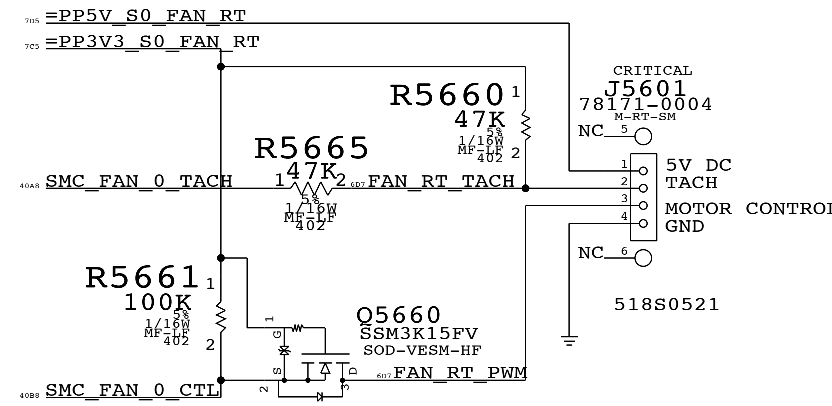

SYNC_MASTER=CHANGZHANG SYNC_DATE=01/18/2008

PAGE TITLE

Fan

Apple Inc.

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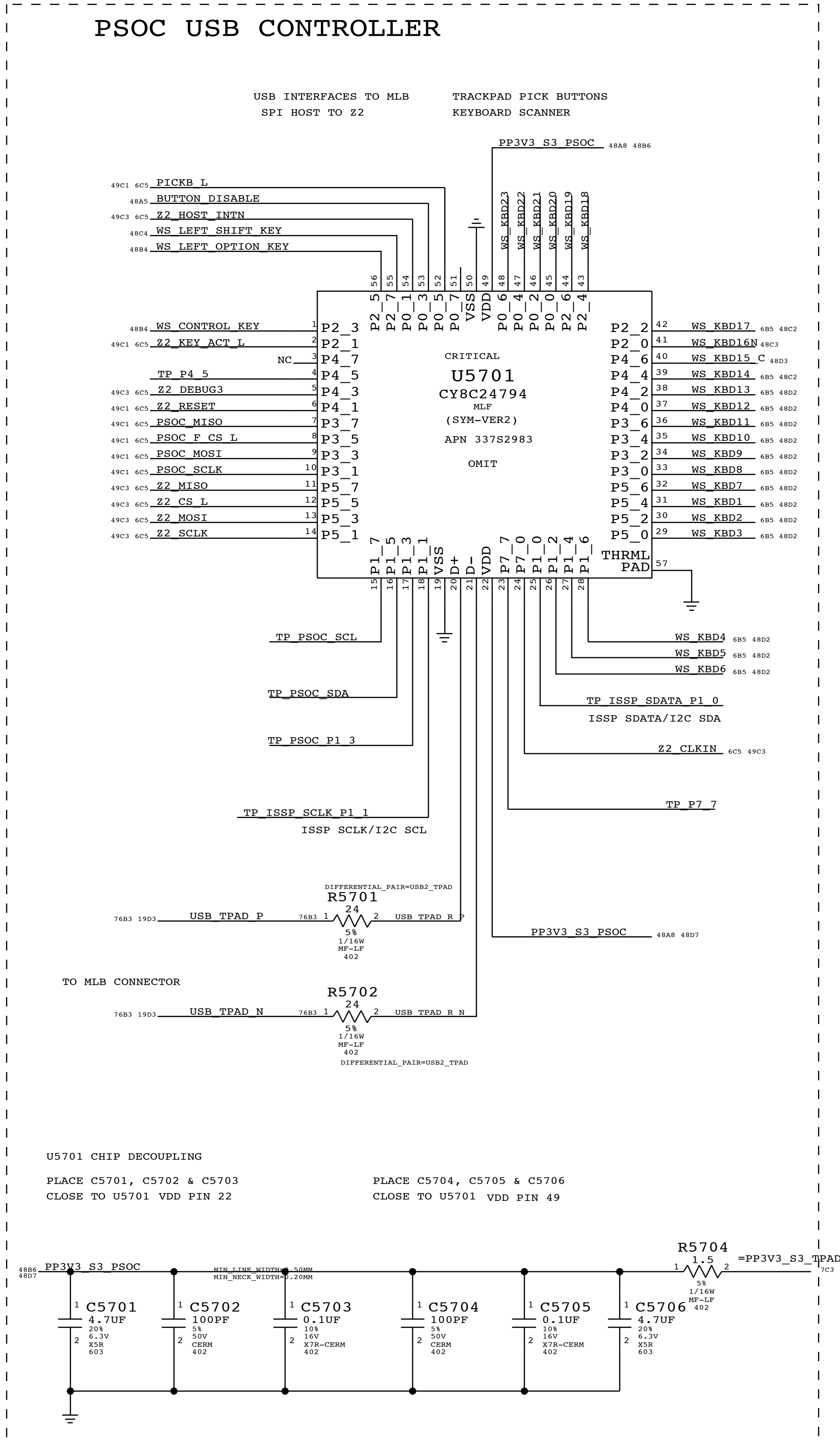
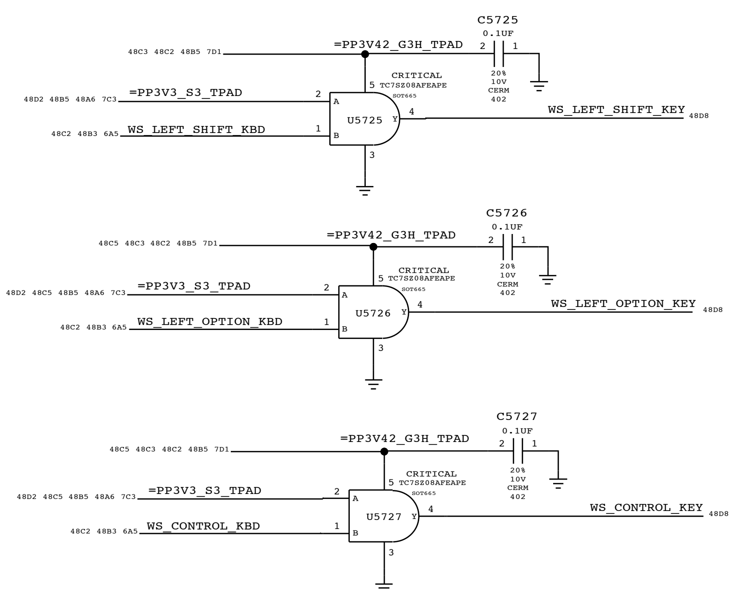
PSOC USB CONTROLLER

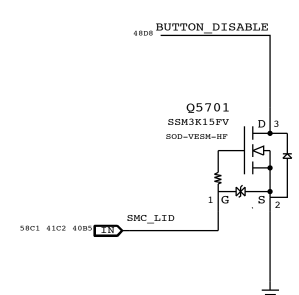


IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

ISOLATION CIRCUIT



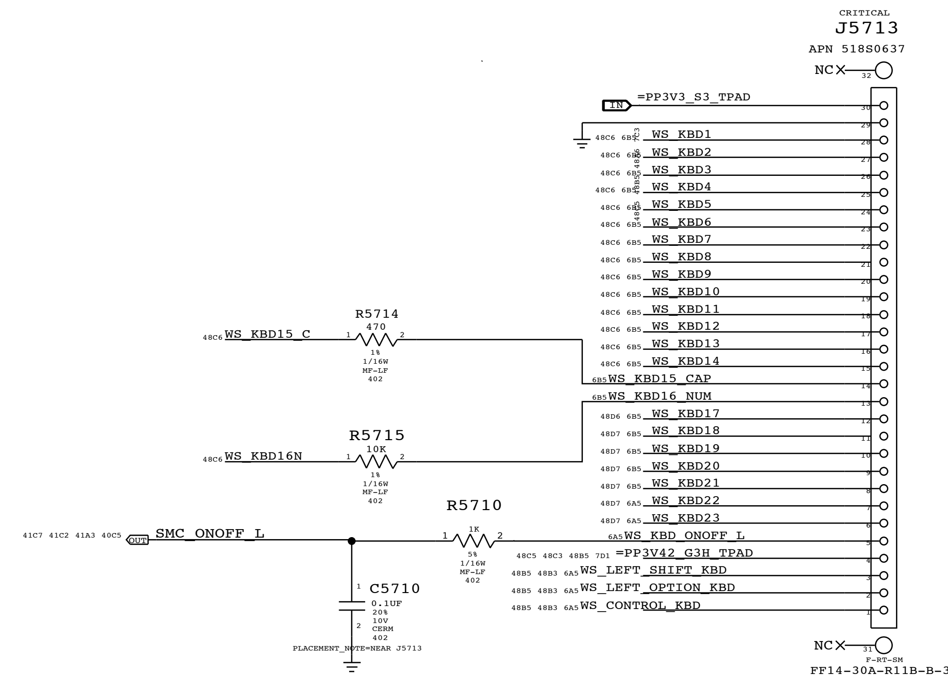
TPAD BUTTONS DISABLE



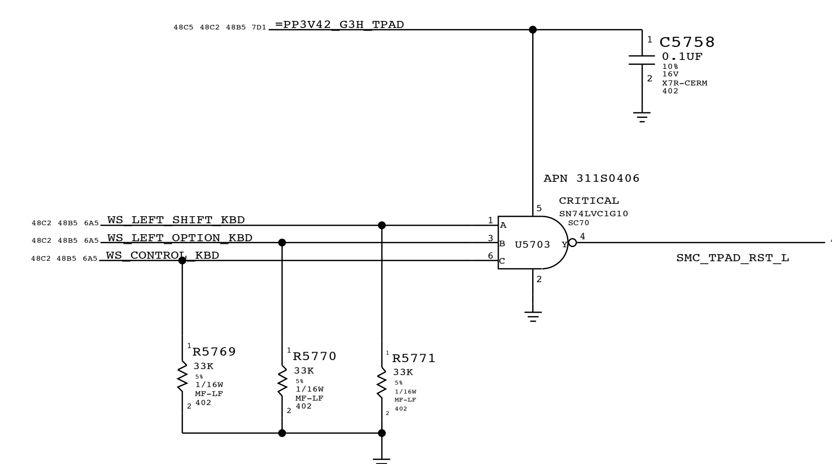
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0406	311S0447		ALL	NXP PART AS ALTERNATE

SYNC_MASTER=YUAN_MA SYNC_DATE=04/22/2008

PAGE TITLE
WELLSPRING 1

Apple Inc.

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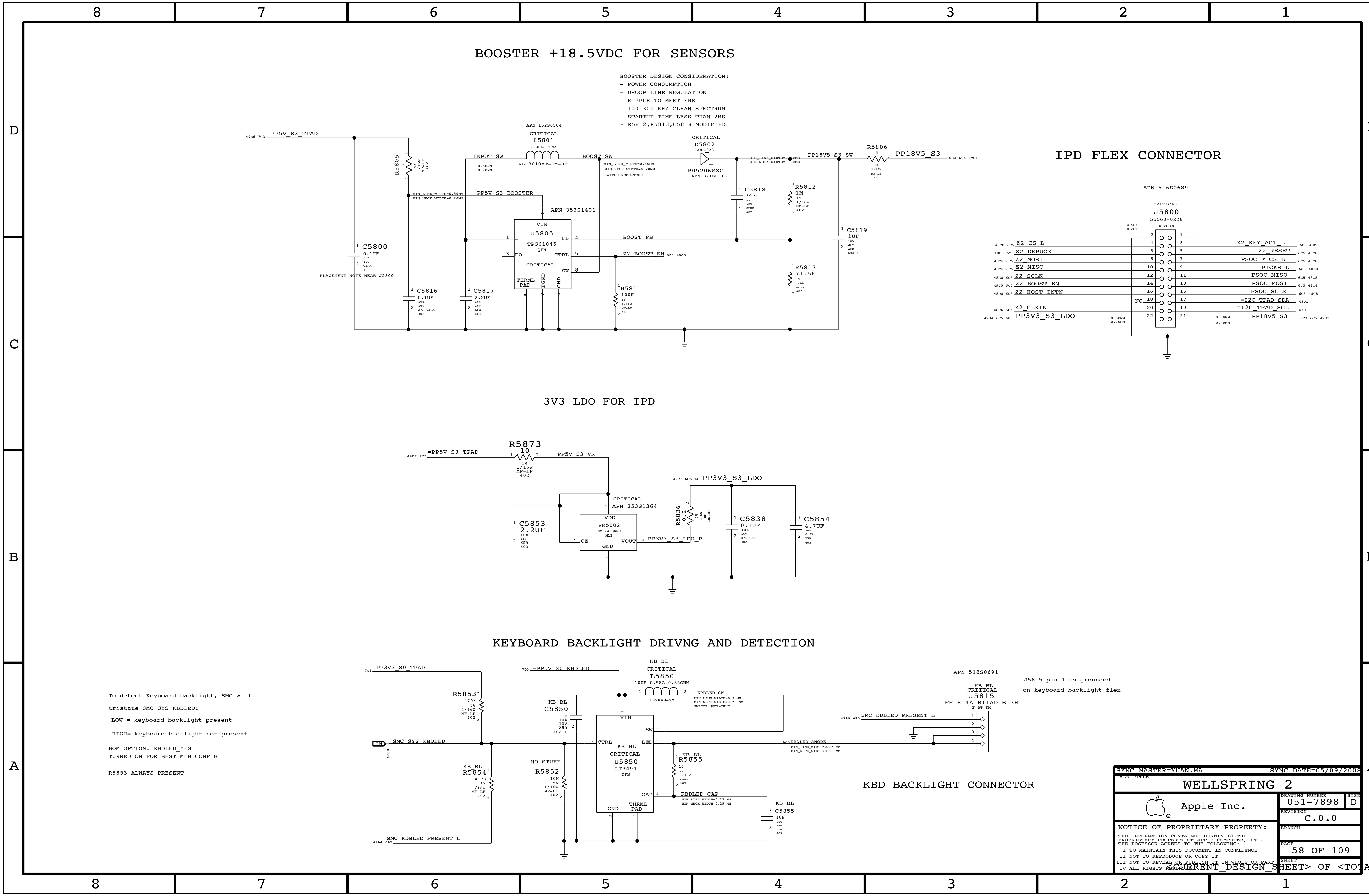

SYNC_MASTER=YUAN.MA SYNC_DATE=05/09/2008

PAGE TITLE: WELLSPRING 2

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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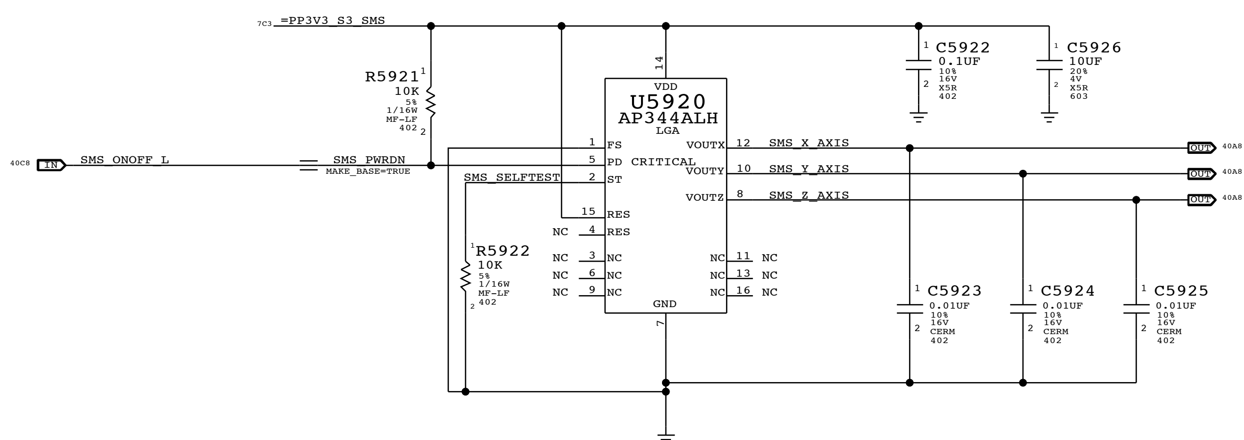
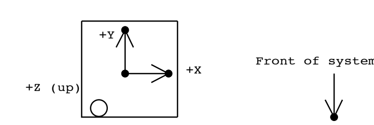
Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

SYNC_MASTER=YUNWU SYNC_DATE=06/26/2008

PAGE TITLE: SMS

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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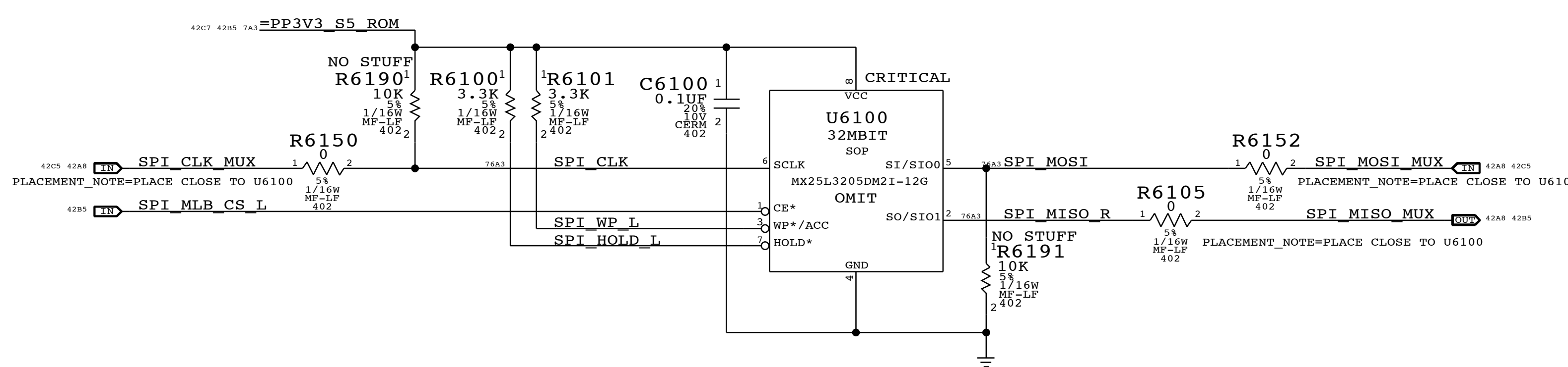
PAGE: 59 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SYNC_MASTER=CHANGZHANG SYNC_DATE=05/02/2008

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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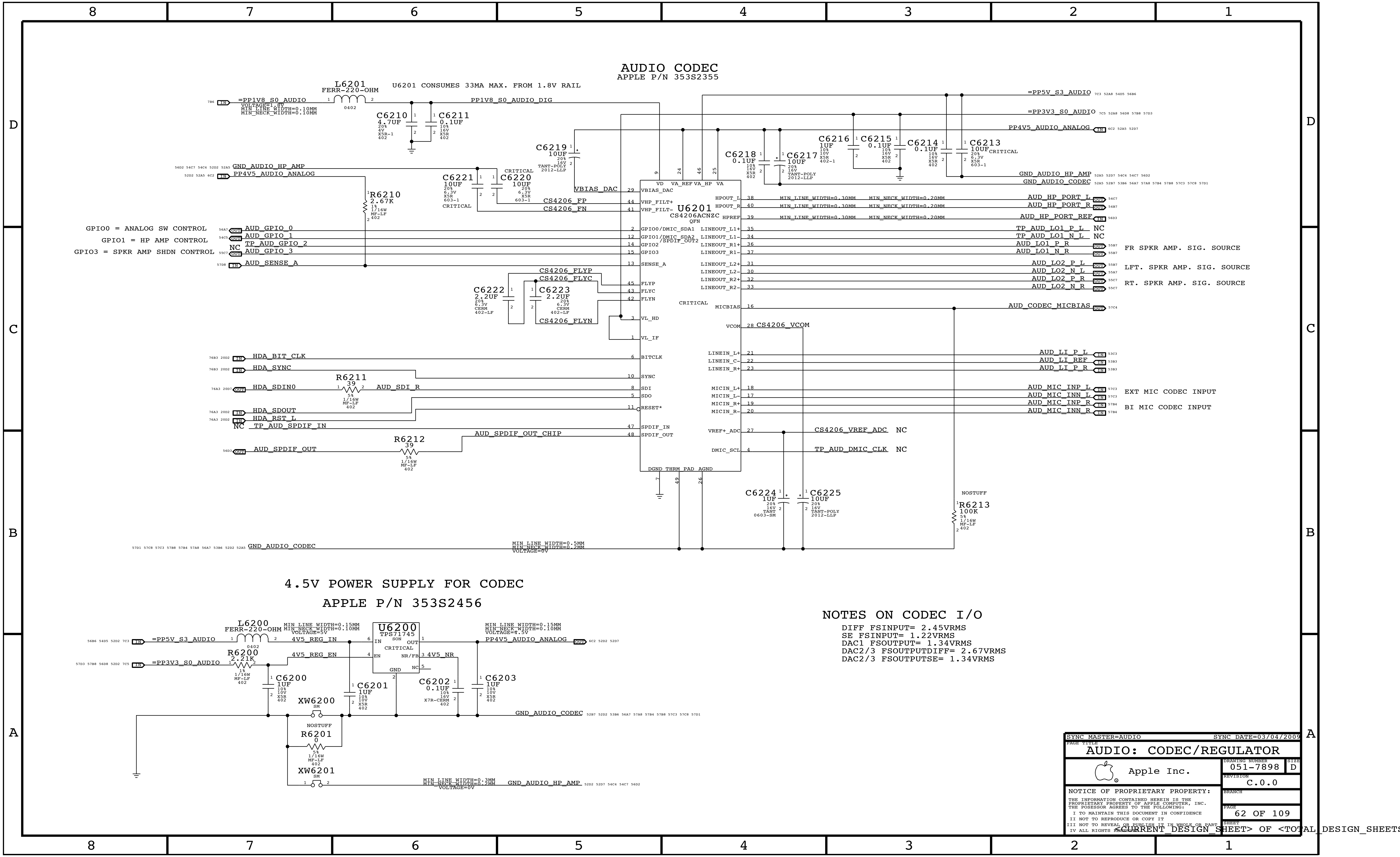
PAGE 61 OF 109

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



AUDIO CODEC
APPLE P/N 353S2355
U6201 CONSUMES 33MA MAX. FROM 1.8V RAIL
L6201
FERR-220-OHM
0402
=PP1V8_S0_AUDIO
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.10MM
MIN_NECK_WIDTH=0.10MM
PP1V8_S0_AUDIO_DIG
C6210
4.7UF
C6211
0.1UF
C6219
10UF
TANT-POLY
2012-LLP
=PP5V_S3_AUDIO
=PP3V3_S0_AUDIO
PP4V5_AUDIO_ANALOG
C6216
1UF
C6215
0.1UF
C6214
0.1UF
C6213
10UF
CRITICAL
C6218
0.1UF
C6217
10UF
GND_AUDIO_HP_AMP
GND_AUDIO_CODEC
GND_AUDIO_HP_AMP
PP4V5_AUDIO_ANALOG
C6221
10UF
CRITICAL
C6220
10UF
CRITICAL
R6210
2.67K
VBIAS_DAC
CS4206_FP
CS4206_FN
U6201
CS4206ACNZC
QFN
GPIO0 = ANALOG SW CONTROL
GPIO1 = HP AMP CONTROL
GPIO3 = SPKR AMP SHDN CONTROL
AUD_GPIO_0
AUD_GPIO_1
TP_AUD_GPIO_2
NC
AUD_GPIO_3
AUD_SENSE_A
CS4206_FLYP
CS4206_FLYC
CS4206_FLYN
C6222
2.2UF
C6223
2.2UF
CRITICAL
HDA_BIT_CLK
HDA_SYNC
R6211
39
HDA_SDIN0
AUD_SDI_R
HDA_SDOUT
HDA_RST_L
TP_AUD_SPDIF_IN
R6212
39
AUD_SPDIF_OUT
AUD_SPDIF_OUT_CHIP
VBIAS_DAC
VHP_FILT+
VHP_FILT-
GPIO0/DMIC_SDA1
GPIO1/DMIC_SDA2 /SPDIF_OUT2
GPIO2
GPIO3
SENSE_A
FLYP
FLYC
FLYN
VL_HD
VL_IF
BITCLK
SYNC
SDI
SDO
RESET*
SPDIF_IN
SPDIF_OUT
VD
VA_REF
VA_HP
VA
DGND
THRM_PAD
AGND
HPOUT_L
HPOUT_R
HPREF
LINEOUT_L1+
LINEOUT_L1-
LINEOUT_R1+
LINEOUT_R1-
LINEOUT_L2+
LINEOUT_L2-
LINEOUT_R2+
LINEOUT_R2-
MICBIAS
VCOM
LINEIN_L+
LINEIN_C-
LINEIN_R+
MICIN_L+
MICIN_L-
MICIN_R+
MICIN_R-
VREF+_ADC
DMIC_SCL
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
AUD_HP_PORT_L
AUD_HP_PORT_R
AUD_HP_PORT_REF
TP_AUD_LO1_P_L
NC
TP_AUD_LO1_N_L
NC
AUD_LO1_P_R
AUD_LO1_N_R
FR SPKR AMP. SIG. SOURCE
AUD_LO2_P_L
AUD_LO2_N_L
LFT. SPKR AMP. SIG. SOURCE
AUD_LO2_P_R
AUD_LO2_N_R
RT. SPKR AMP. SIG. SOURCE
AUD_CODEC_MICBIAS
CS4206_VCOM
AUD_LI_P_L
AUD_LI_REF
AUD_LI_P_R
AUD_MIC_INP_L
AUD_MIC_INN_L
EXT MIC CODEC INPUT
AUD_MIC_INP_R
AUD_MIC_INN_R
BI MIC CODEC INPUT
CS4206_VREF_ADC
NC
TP_AUD_DMIC_CLK
NC
C6224
1UF
TANT
0603-SM
C6225
10UF
TANT-POLY
2012-LLP
NOSTUFF
R6213
100K
GND_AUDIO_CODEC
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2456
L6200
FERR-220-OHM
0402
=PP5V_S3_AUDIO
MIN_LINE_WIDTH=0.15MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=5V
4V5_REG_IN
R6200
2.21K
=PP3V3_S0_AUDIO
4V5_REG_EN
U6200
TPS71745
SON
CRITICAL
IN
EN
OUT
NR/FB
NC
GND
4V5_NR
MIN_LINE_WIDTH=0.15MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=4.5V
PP4V5_AUDIO_ANALOG
C6200
1UF
C6201
1UF
C6202
0.1UF
C6203
1UF
XW6200
SM
NOSTUFF
R6201
0
XW6201
SM
GND_AUDIO_CODEC
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
GND_AUDIO_HP_AMP
NOTES ON CODEC I/O
DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS
SYNC_MASTER=AUDIO
SYNC_DATE=03/04/2009
PAGE TITLE
AUDIO: CODEC/REGULATOR
Apple Inc.
DRAWING NUMBER
051-7898
SIZE
D
REVISION
C.0.0
BRANCH
PAGE
62 OF 109
SHEET
<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>
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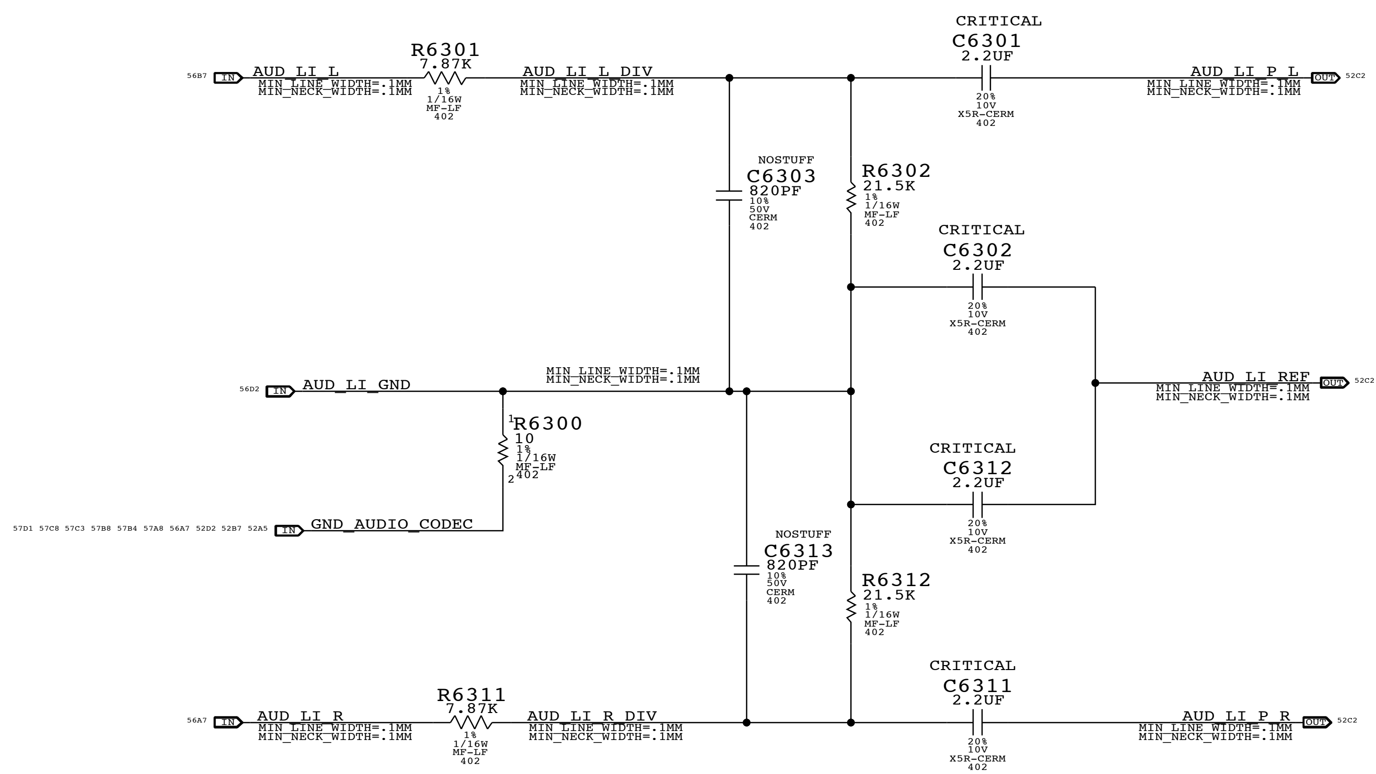
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS

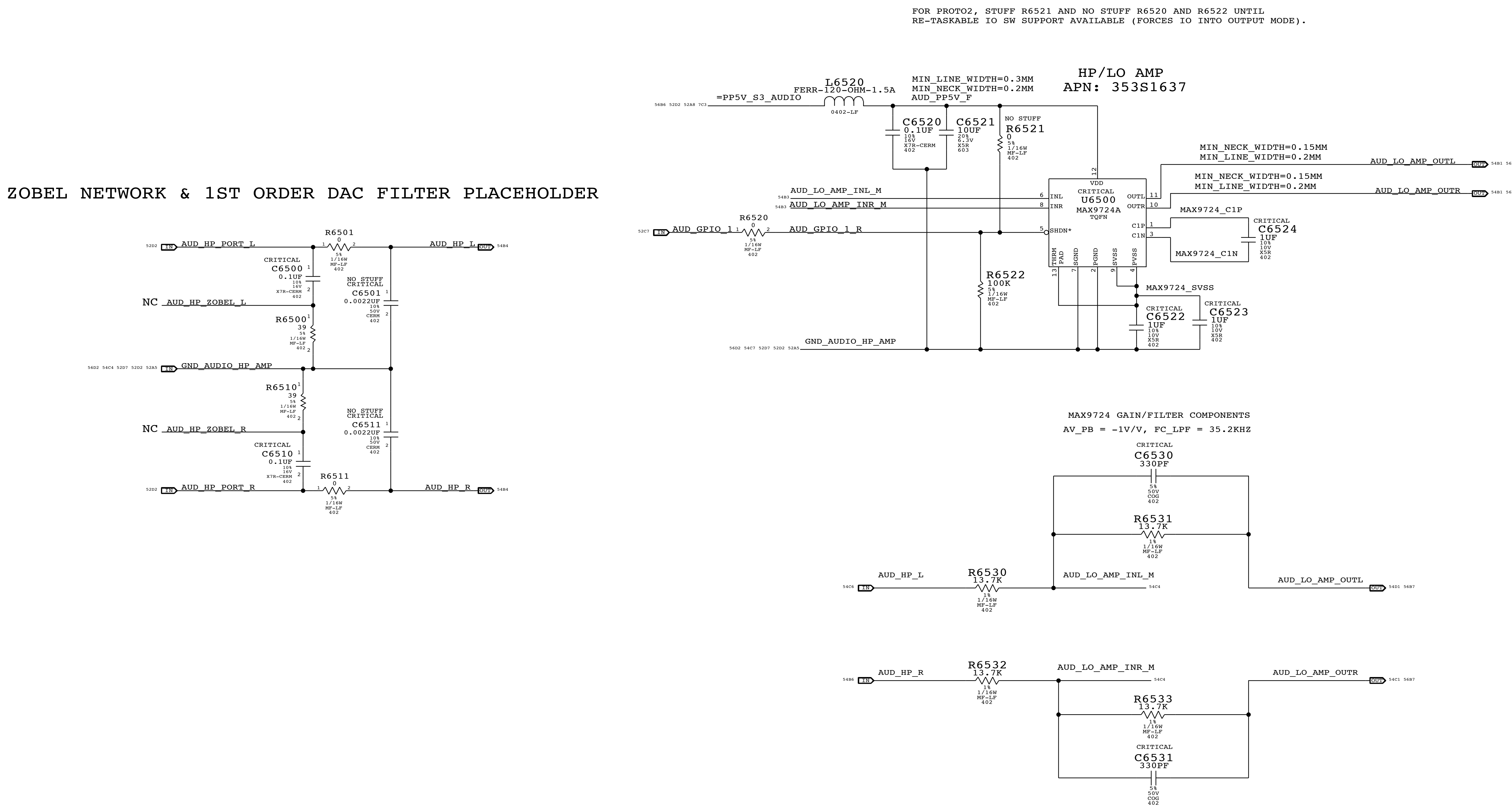


SYNC MASTER=AUDIO SYNC DATE=01/31/2009

PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

DRAWING NUMBER 051-7898 | SIZE D
REVISION C.0.0
BRANCH
PAGE 63 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC MASTER=AUDIO SYNC DATE=02/03/2009

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

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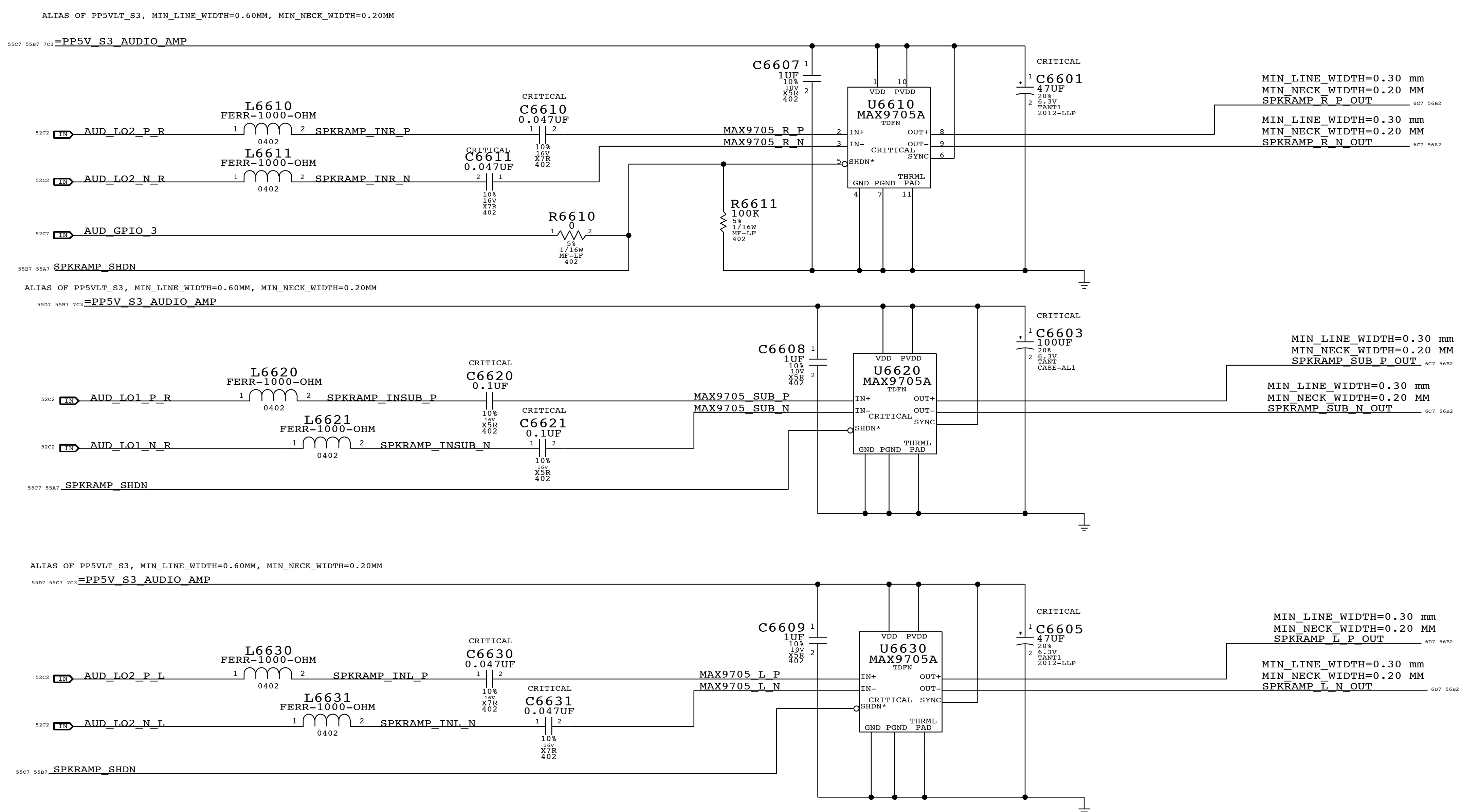
SATELLITE & SUB TWEETER AMPLIFIER

APN:353S2524

SATELLITE	169 HZ < FC < 282 HZ
SUB	80 HZ < FC < 132 HZ
GAIN	6DB



SYNC_MASTER=AUDIO SYNC_DATE=12/18/2008

PAGE TITLE

AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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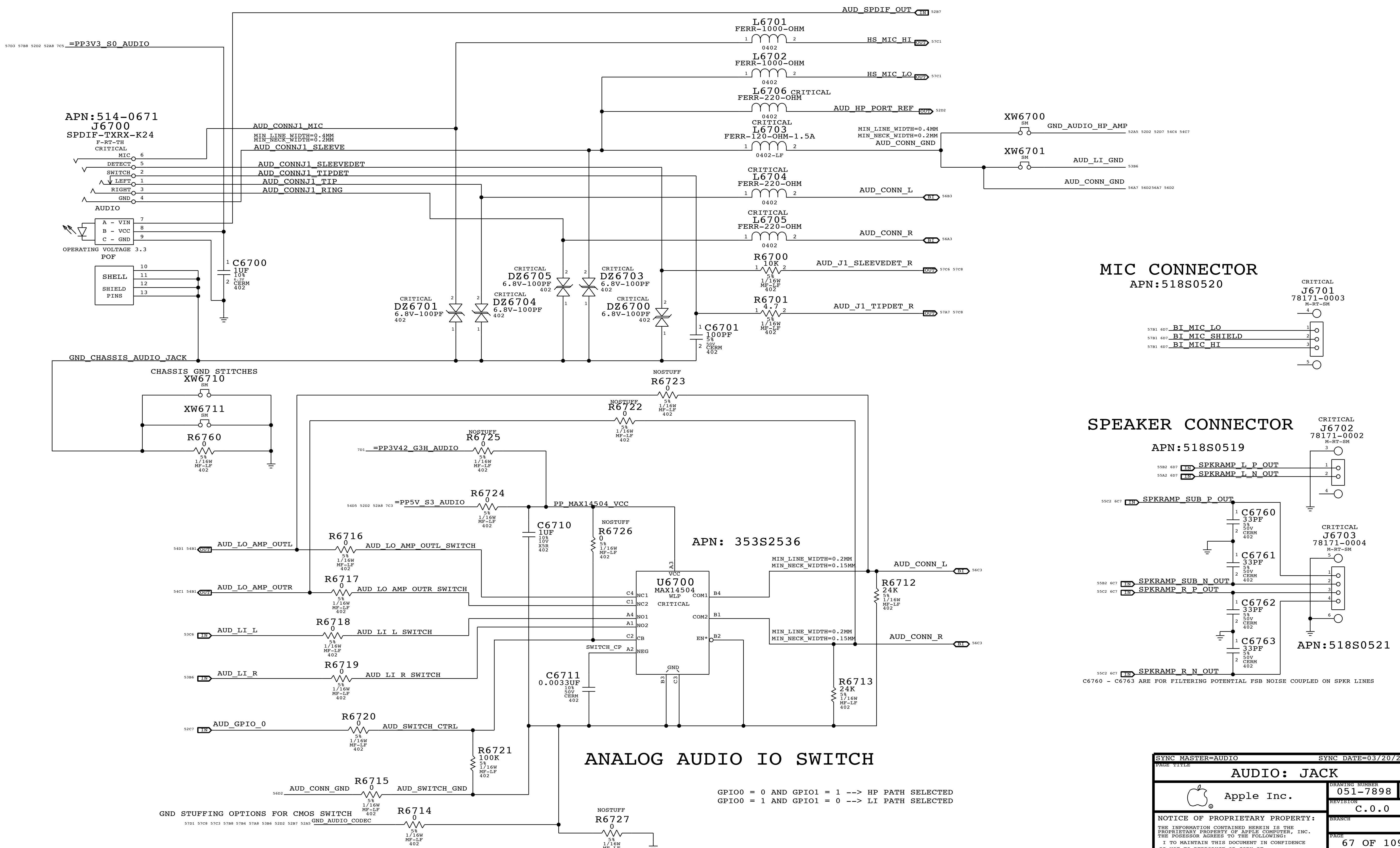
AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



C6760 - C6763 ARE FOR FILTERING POTENTIAL FSB NOISE COUPLED ON SPKR LINES

ANALOG AUDIO IO SWITCH

GPIO0 = 0 AND GPIO1 = 1 --> HP PATH SELECTED
GPIO0 = 1 AND GPIO1 = 0 --> LI PATH SELECTED

SYNC_MASTER=AUDIO SYNC_DATE=03/20/2009

PAGE TITLE: AUDIO: JACK

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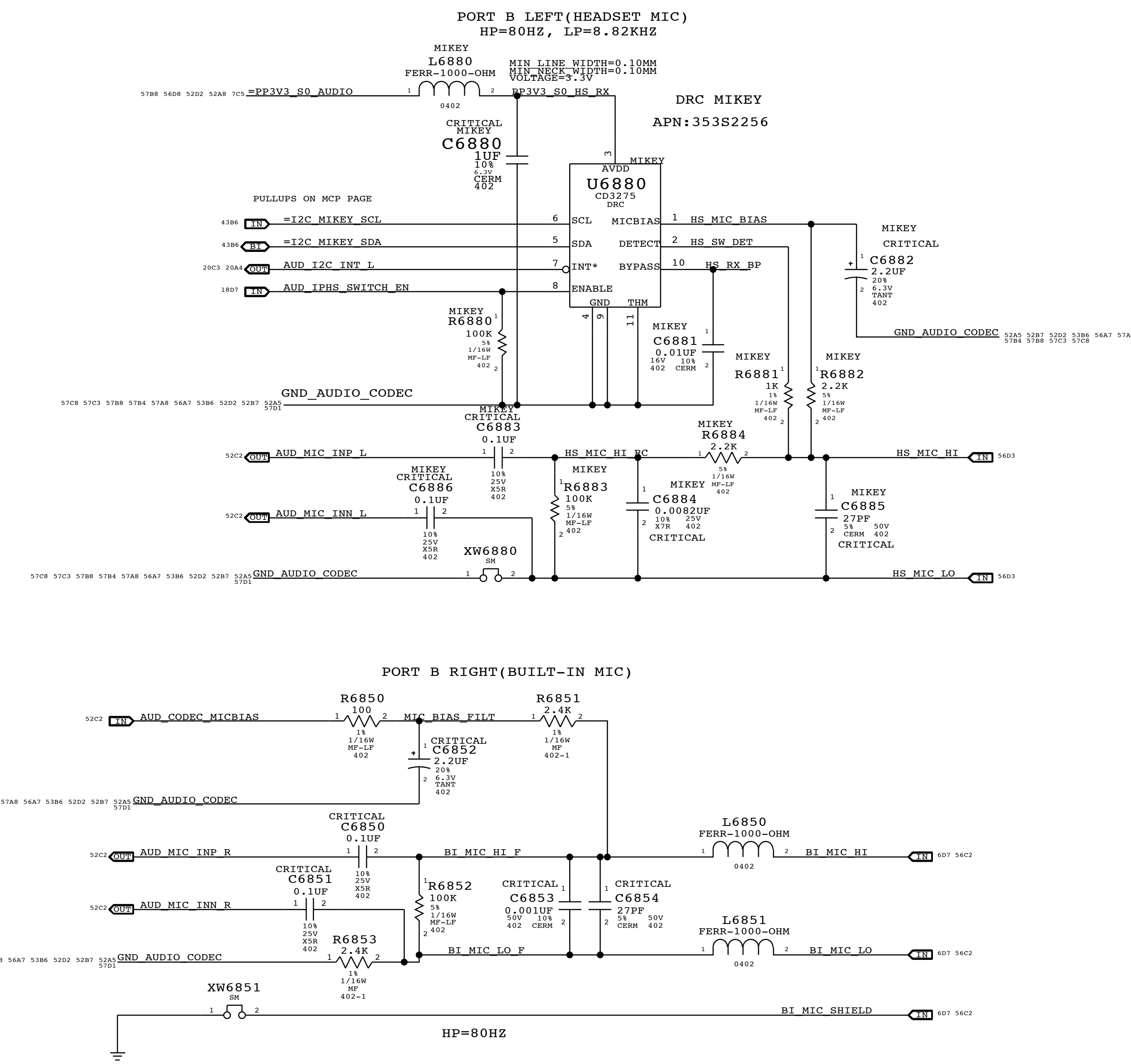
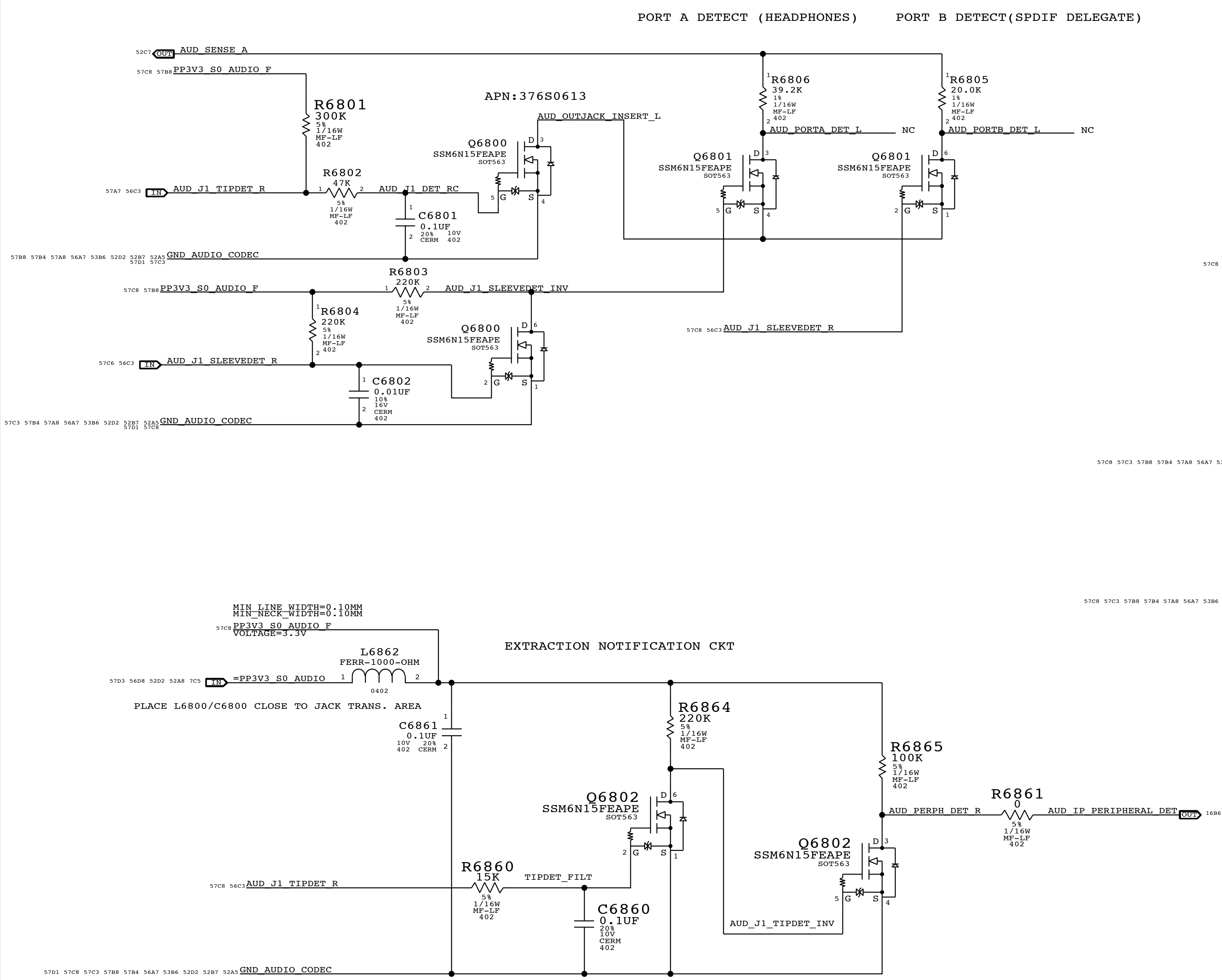
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_0 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_0 AND GPIO_1	0X09 (A)AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY





SYNC MASTER=AUDIO SYNC DATE=03/20/2009

PAGE TITLE

AUDIO: JACK TRANSLATORS

Apple Inc.

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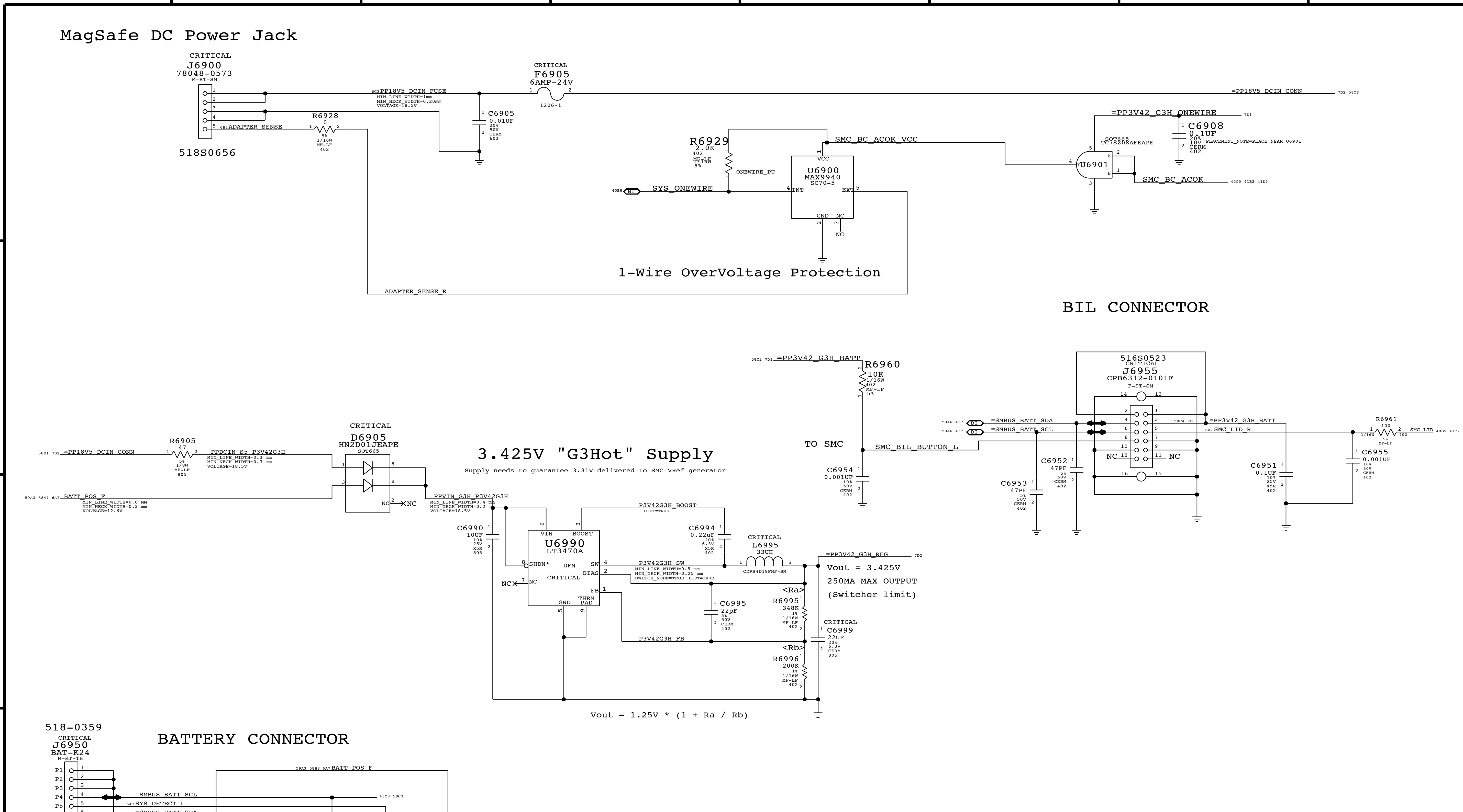

SYNC_MASTER=YUNWU SYNC_DATE=12/11/2008

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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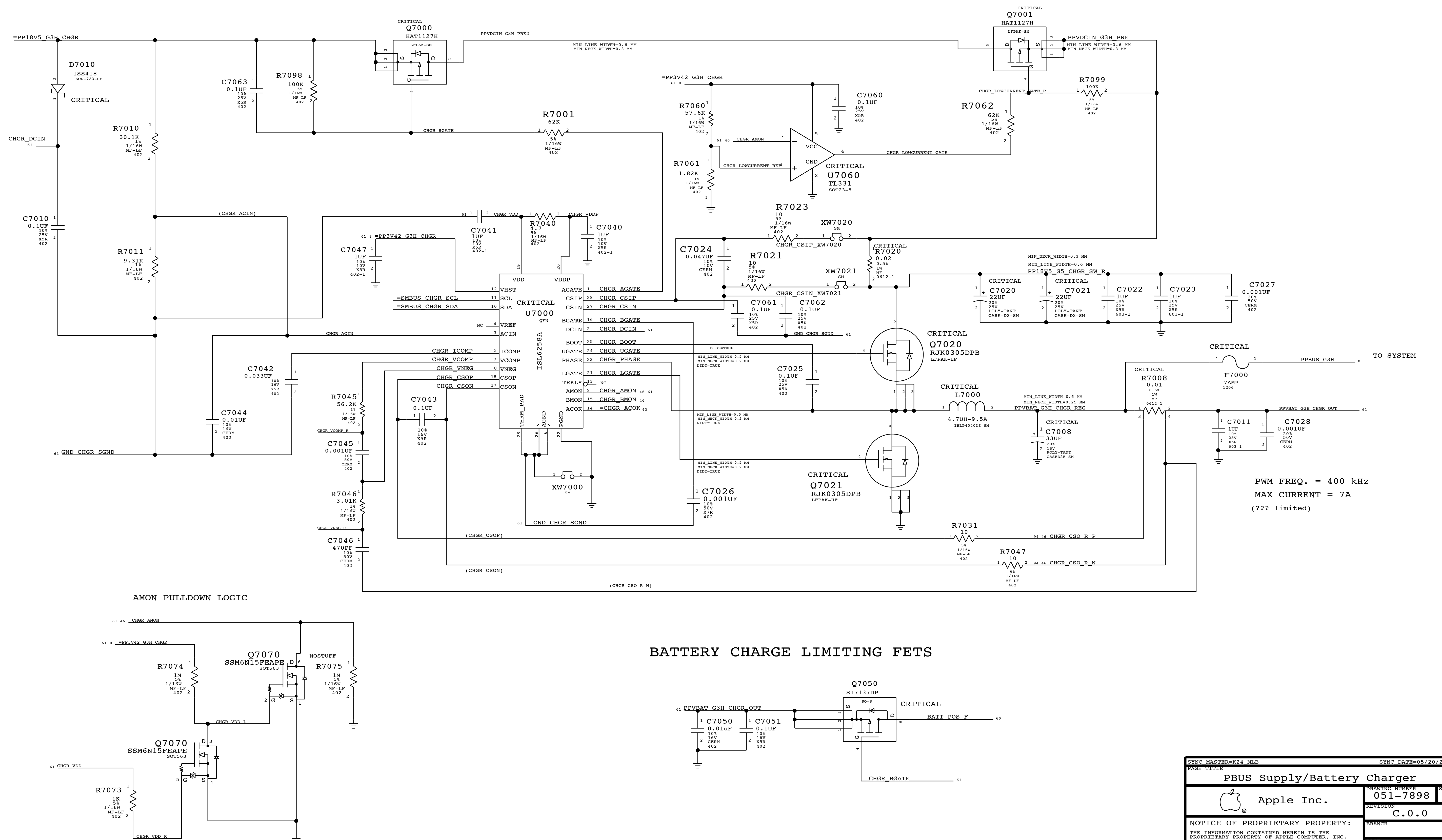
PBUS SUPPLY / BATTERY CHARGER



SYNC_MASTER=K24_MLB SYNC_DATE=05/20/2009

PAGE TITLE: PBUS Supply/Battery Charger

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

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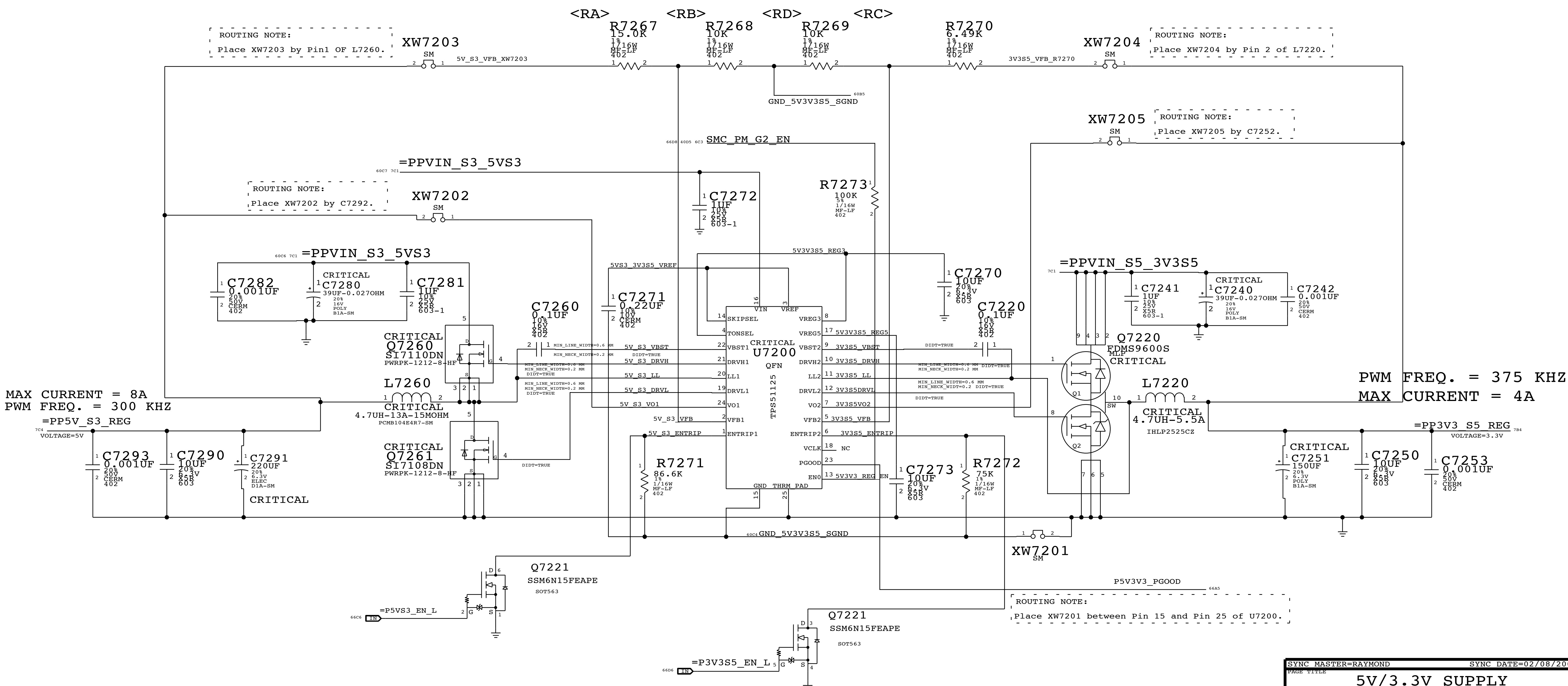
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

5V_S3/3.3V_S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



SEPERATED MASTER PGOOD FOR BOTH 5V AND 3V3.

SYNC_MASTER=RAYMOND SYNC_DATE=02/08/2008

PAGE TITLE: 5V/3.3V SUPPLY

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

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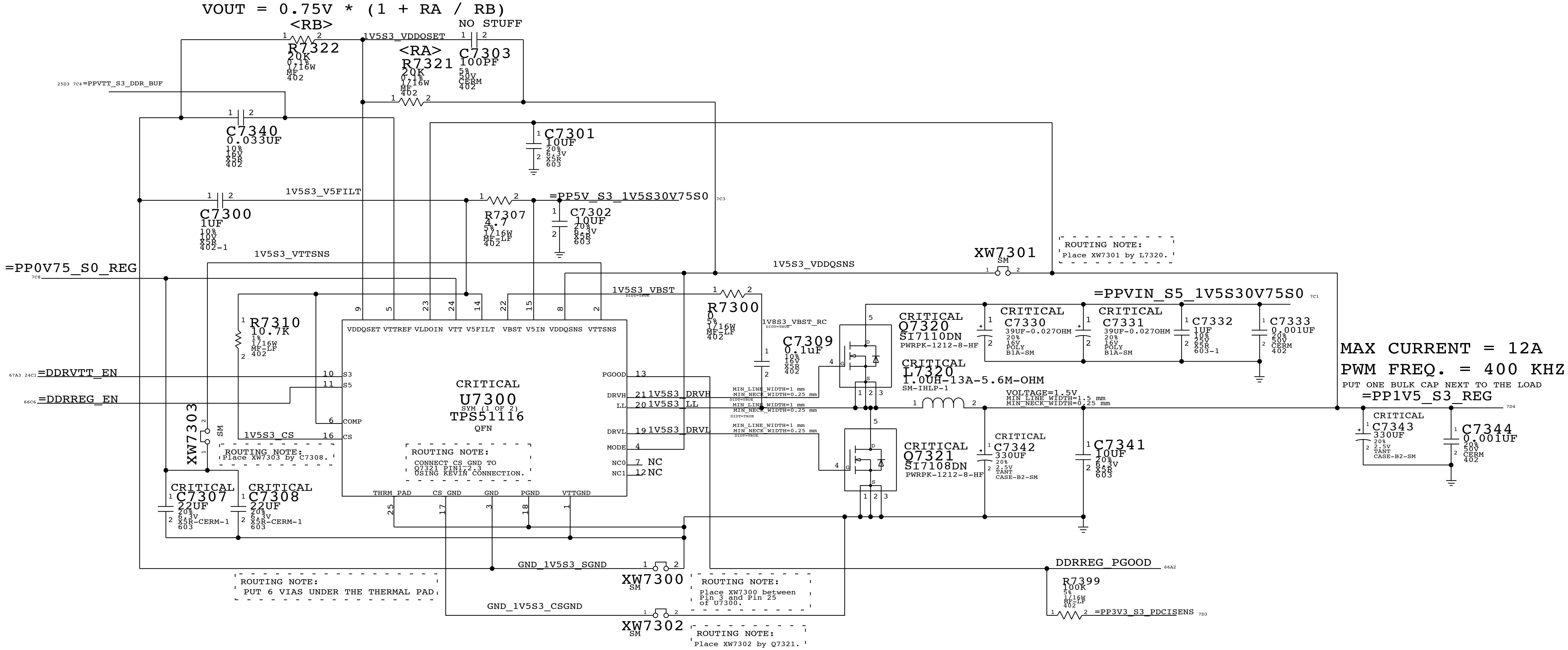
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

1.5V/0.75V(DDR3) POWER SUPPLY



STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

PAGE TITLE
1.5V/0.75V DDR3 SUPPLY

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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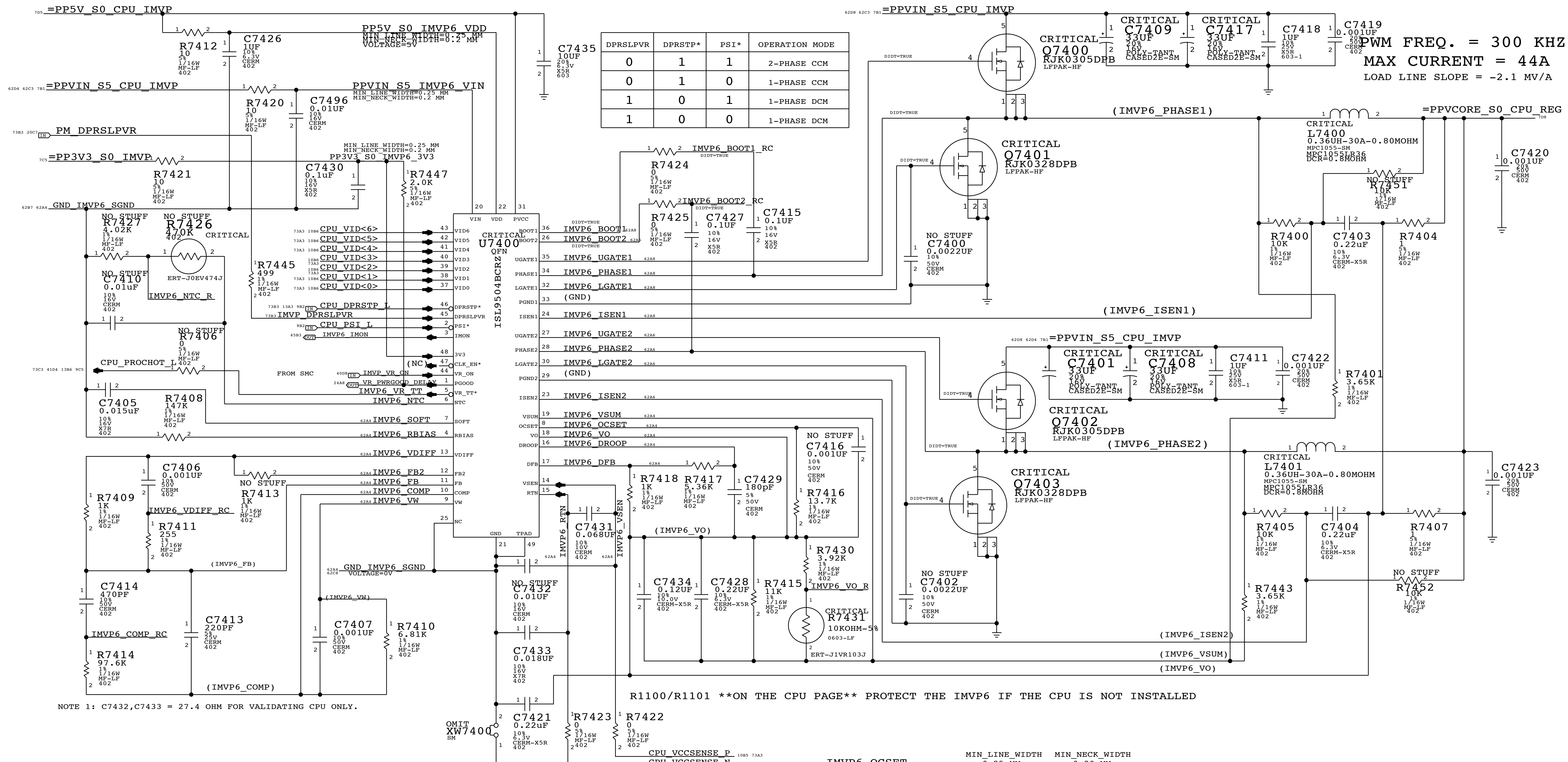

DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

NOTE 1: C7432,C7433 = 27.4 OHM FOR VALIDATING CPU ONLY.

IMVP6 CPU VCORE REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	1.5 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	1.5 MM	0.25 MM
IMVP6_LGATE2	1.5 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSENSE	0.25 MM	0.25 MM

SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

PAGE TITLE
IMVP6 CPU VCore Regulator

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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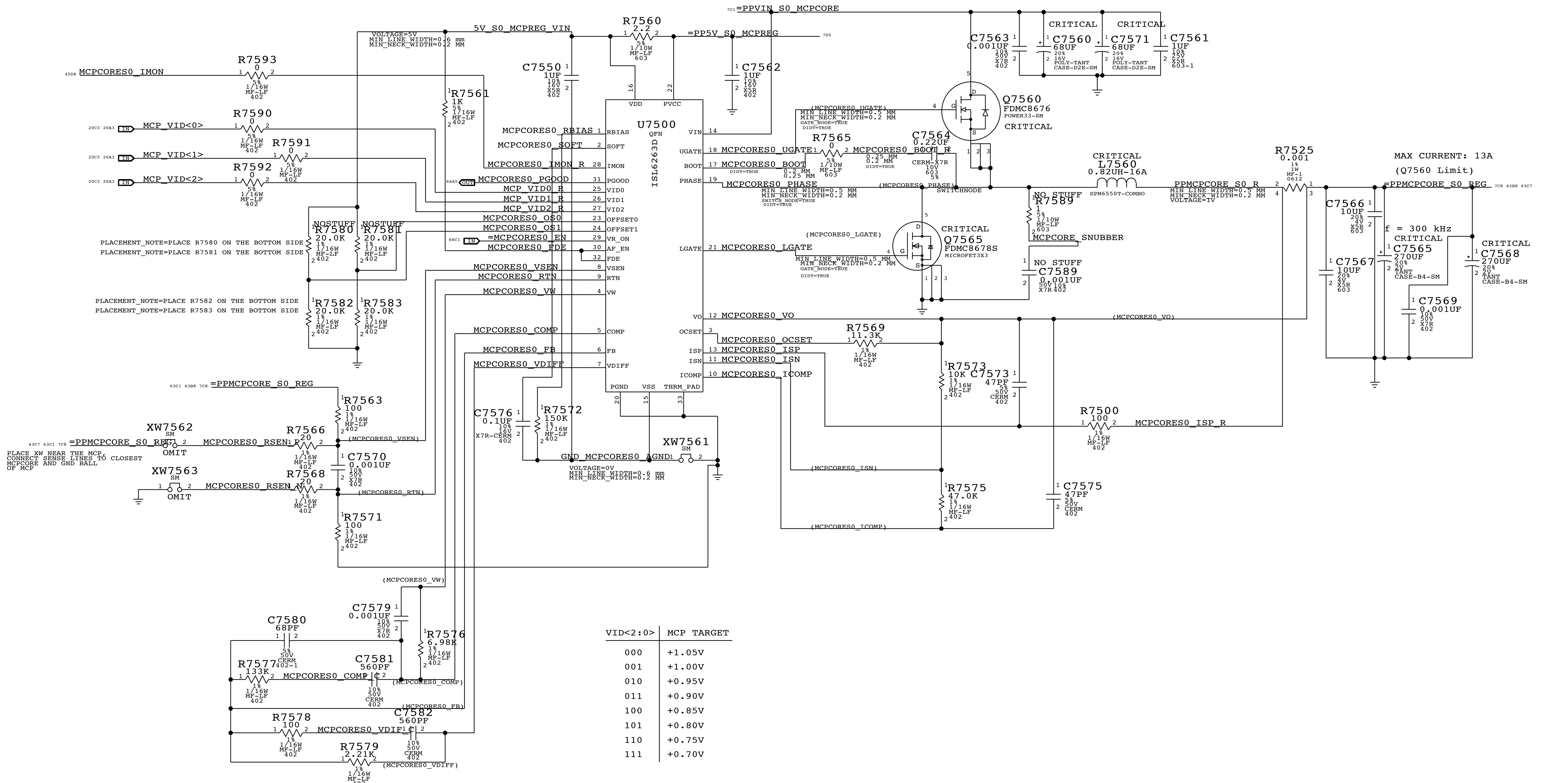
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MCP VCORE POWER SUPPLY



VID<2:0>	MCP TARGET
000	+1.05V
001	+1.00V
010	+0.95V
011	+0.90V
100	+0.85V
101	+0.80V
110	+0.75V
111	+0.70V

SYNC_MASTER=K19_MLB SYNC_DATE=12/10/2008

PAGE TITLE
MCP CORE REGULATOR

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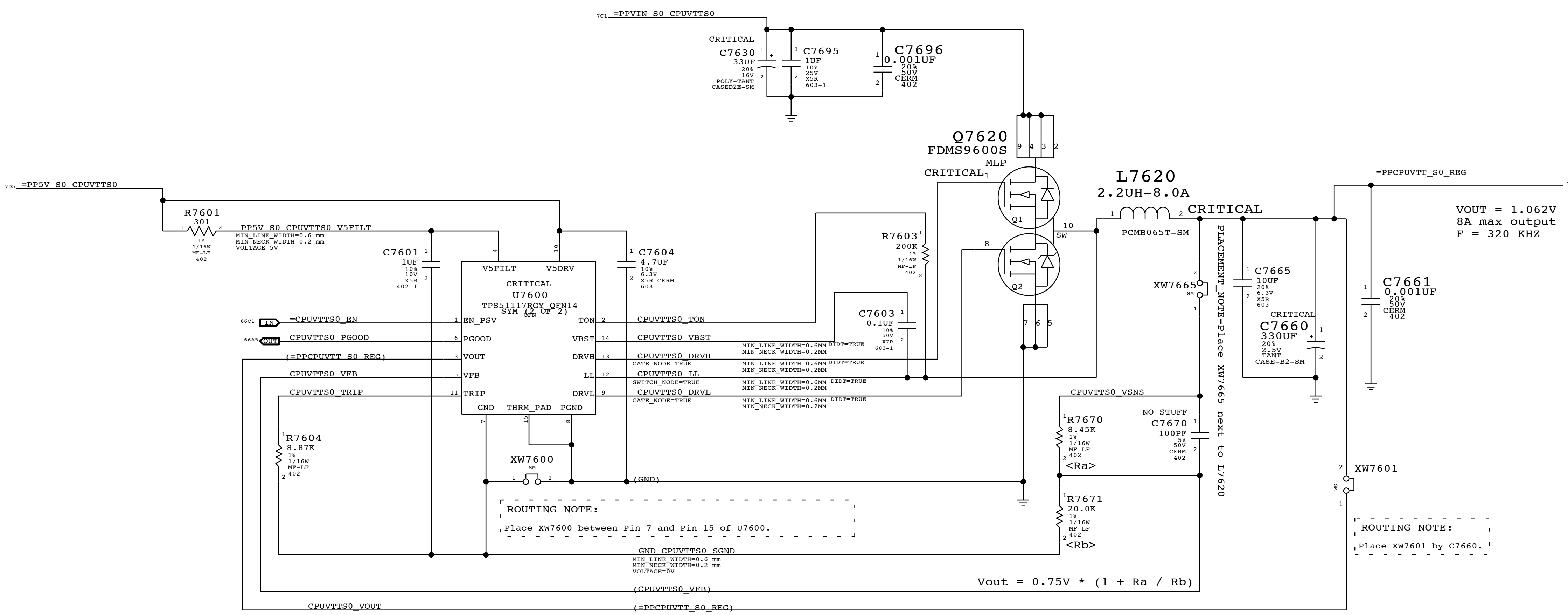
CPUVTT POWER SUPPLY



SYNC_MASTER=RAYMOND SYNC_DATE=02/08/2008

PAGE TITLE

CPU VTT(1.05V) SUPPLY

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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BRANCH

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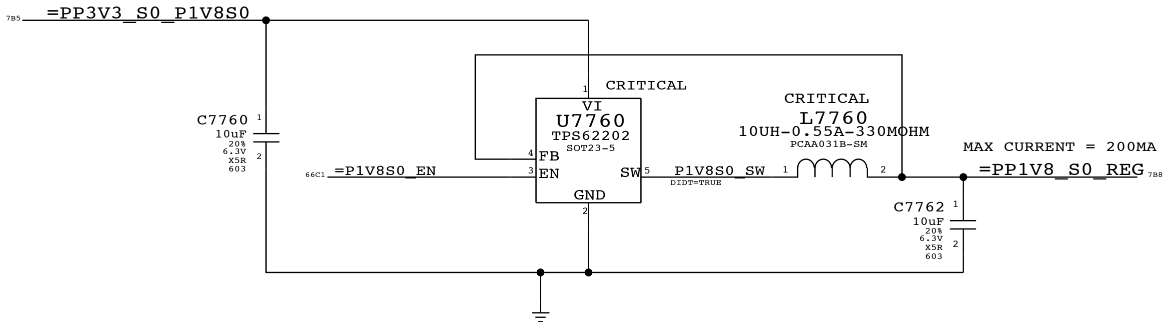
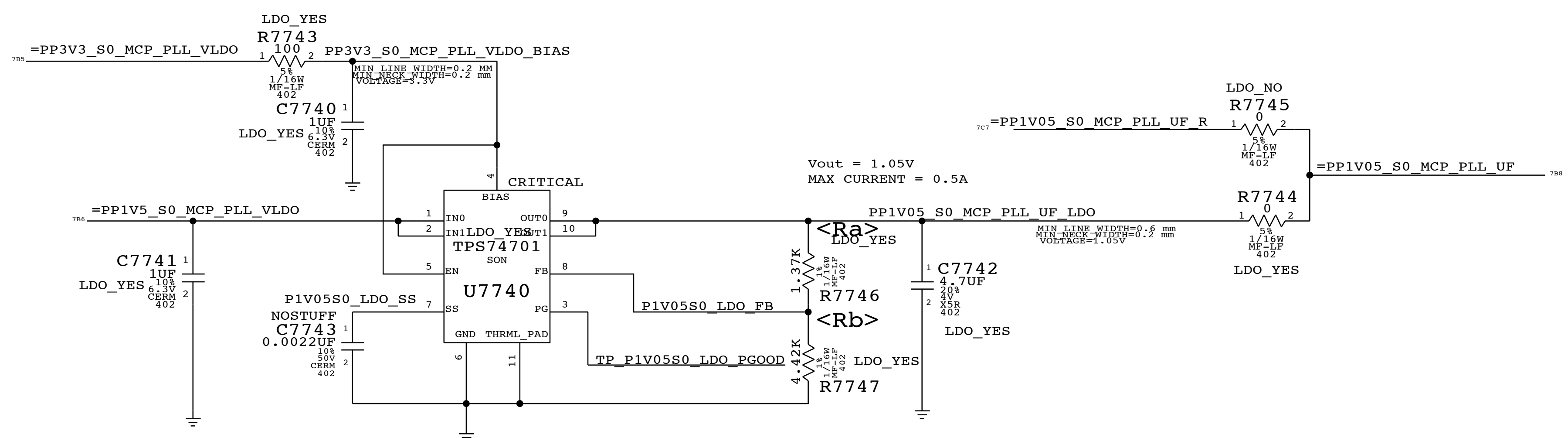
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

1.8V S0 SWITCHER

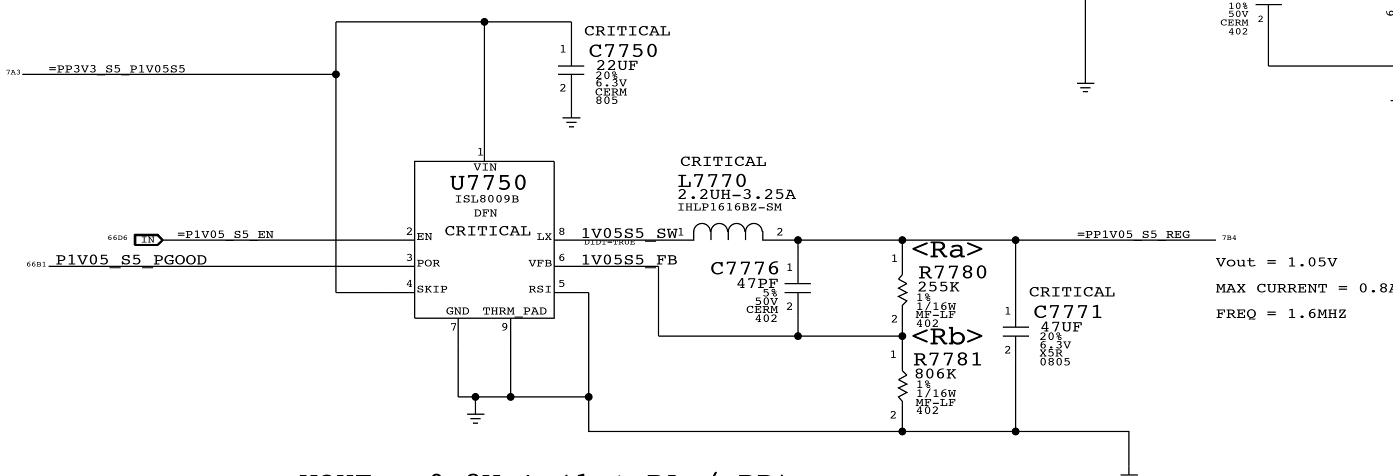


1.05V S0 PLL LDO



VOUT = 0.8V * (1 + RA / RB)

MCP 1.05V S5 (AUXC) SUPPLY



VOUT = 0.8V * (1 + RA / RB)

SYNC_MASTER=RAYMOND SYNC_DATE=01/23/2008

PAGE TITLE

MISC POWER SUPPLIES

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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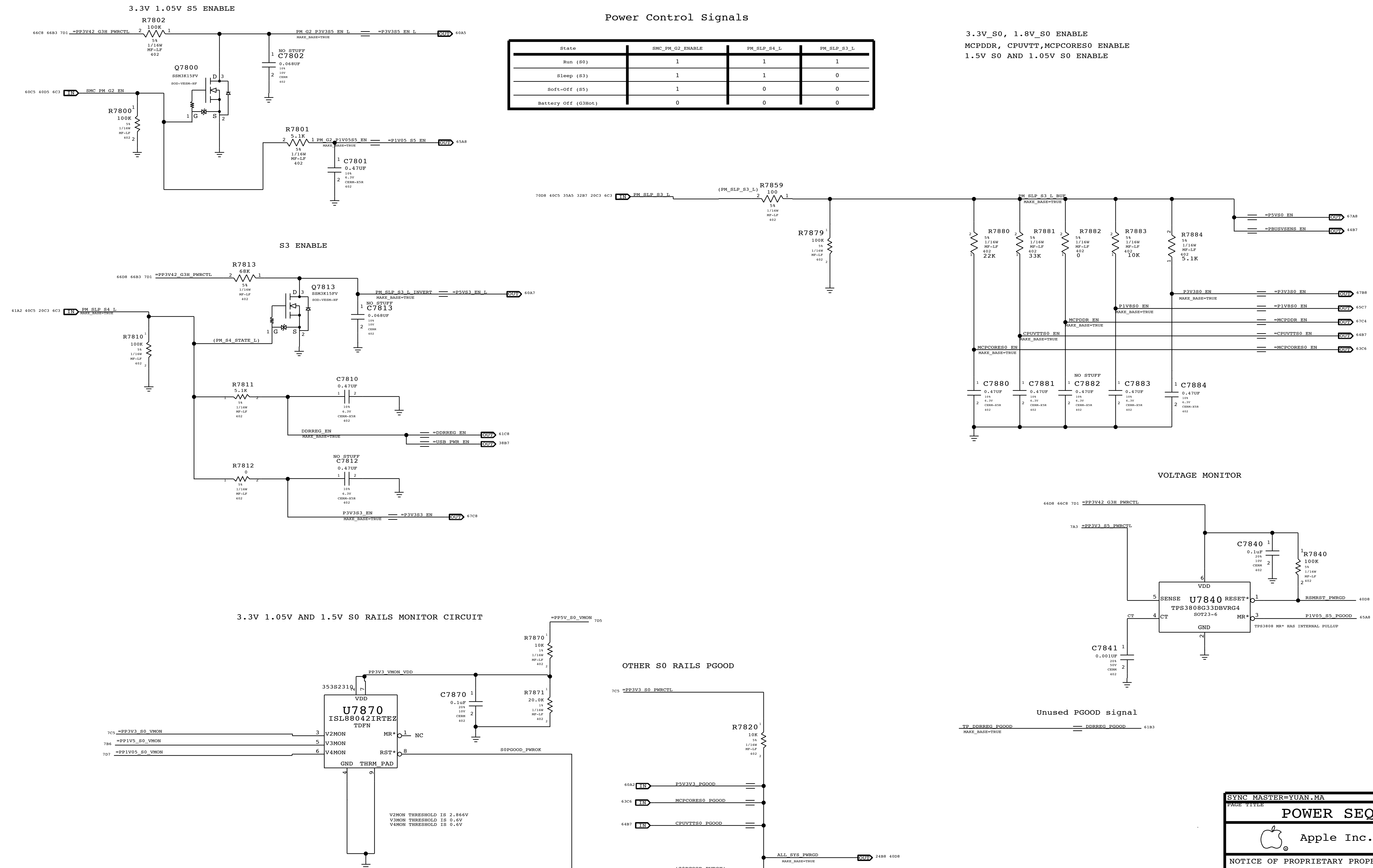
Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0



SYNC MASTER=YUAN.MA   SYNC DATE=12/11/2008

PAGE TITLE
POWER SEQUENCING

Apple Inc.

DRAWING NUMBER 051-7898   SIZE D

REVISION C.0.0

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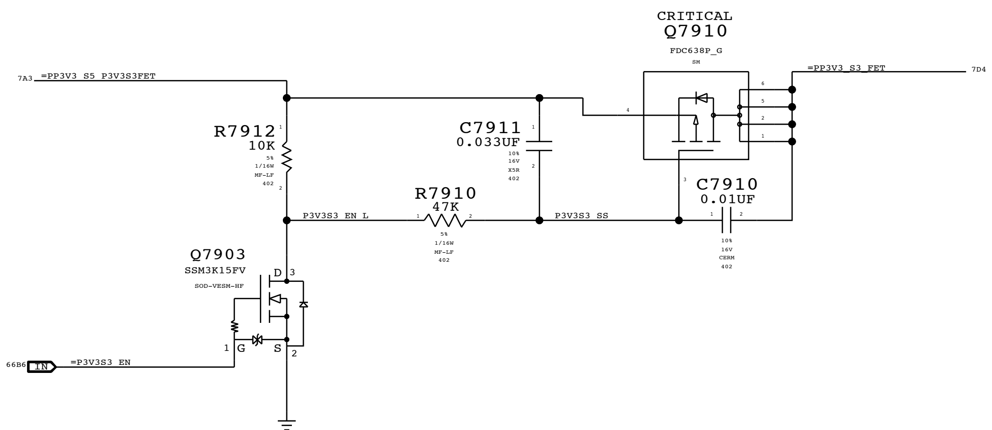
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

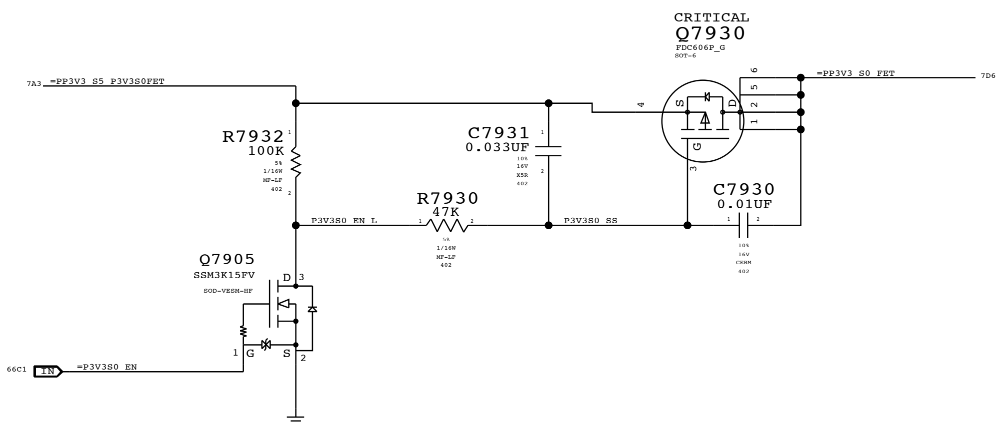
3.3V S3 FET



3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

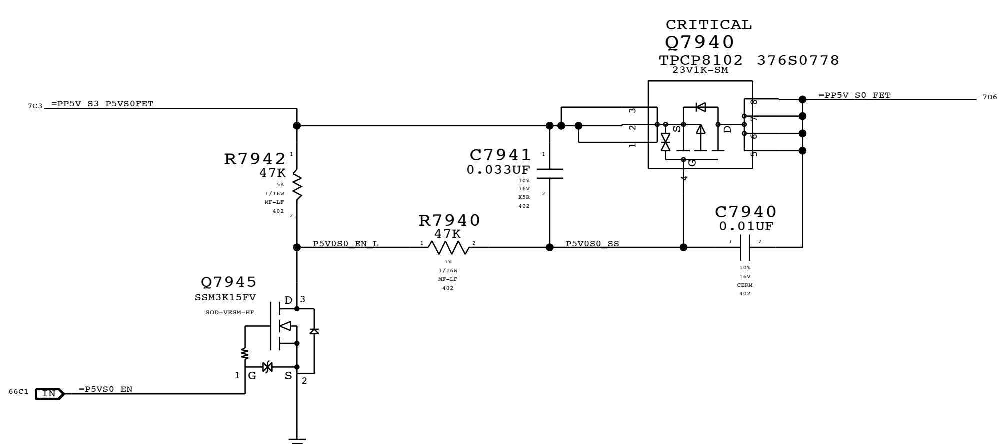
3.3V S0 FET



3.3V S0 FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

5.0V S0 FET

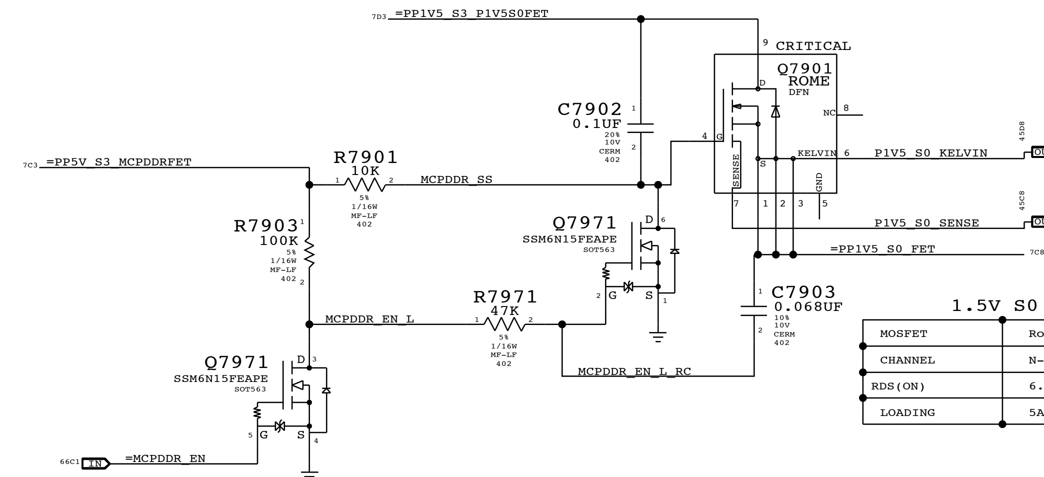


5.0V S0 FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	1.7 A (EDP)

1.5V S0 FET

(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)

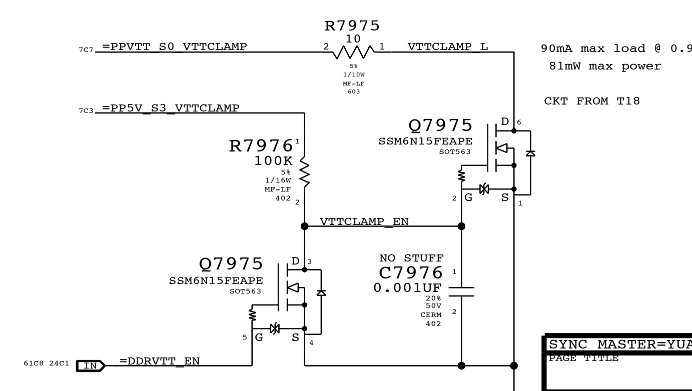


1.5V S0 FET

MOSFET	Rome SenseFET
CHANNEL	N-TYPE
RDS(ON)	6.3 mOHM @4.5V VGS
LOADING	5A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



SYNC_MASTER=YUAN.MA	SYNC_DATE=12/11/2008
PAGE TITLE	POWER FETS
Apple Inc.	DRAWING NUMBER 051-7898 SIZE D
	REVISION C.0.0
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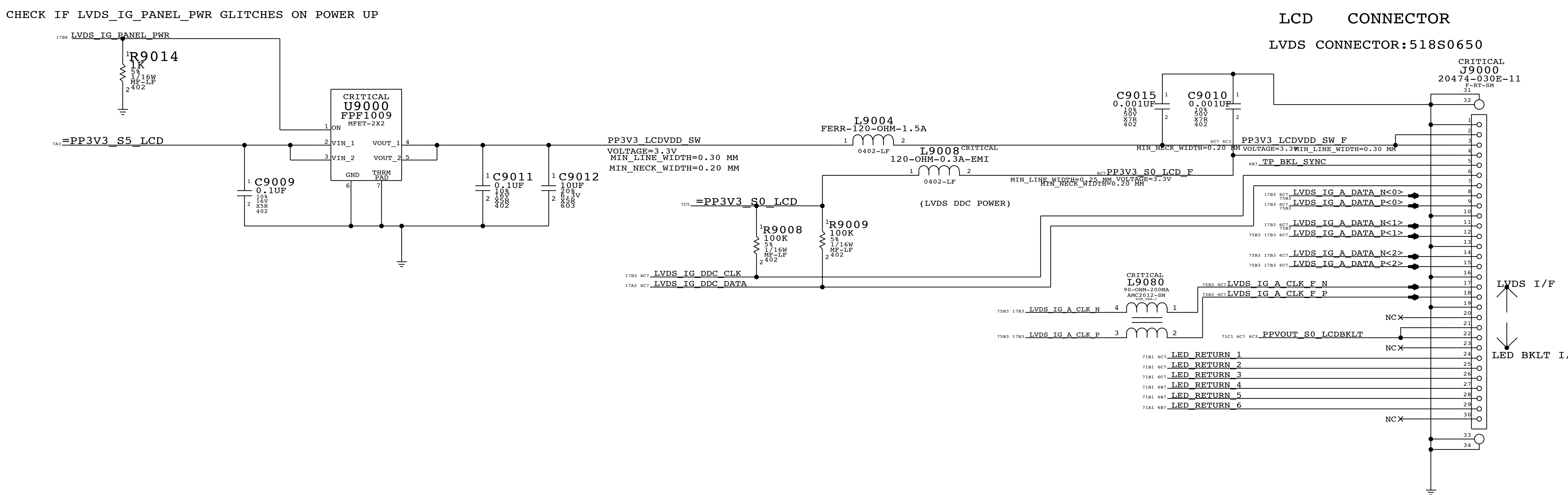
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=NMARTIN SYNC_DATE=04/04/2008

PAGE TITLE

LVDS CONNECTOR

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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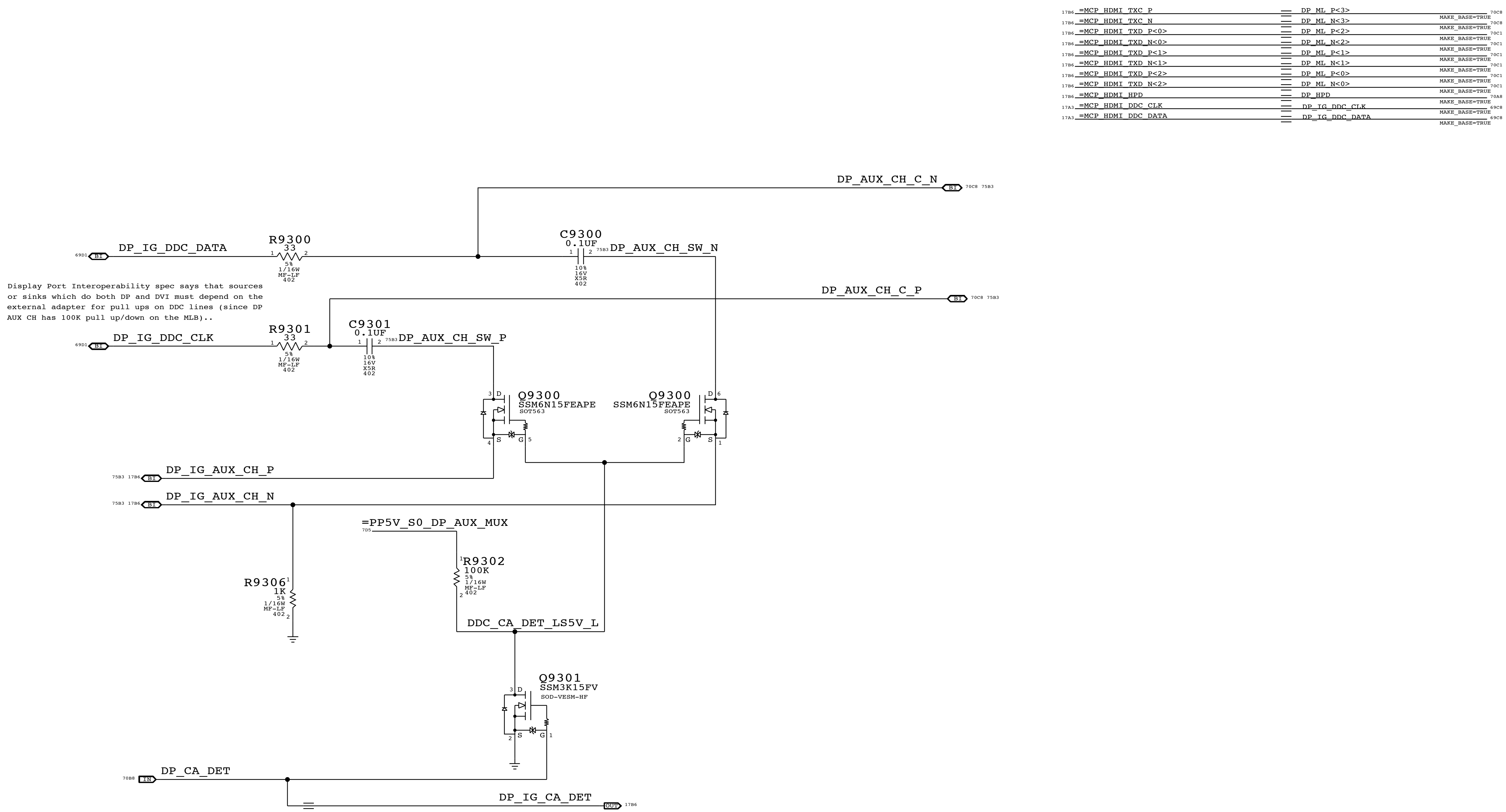
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

NOTICE OF PROPRIETARY PROPERTY:



SYNC_MASTER=AMASON SYNC_DATE=04/18/2008

PAGE TITLE

DISPLAYPORT SUPPORT

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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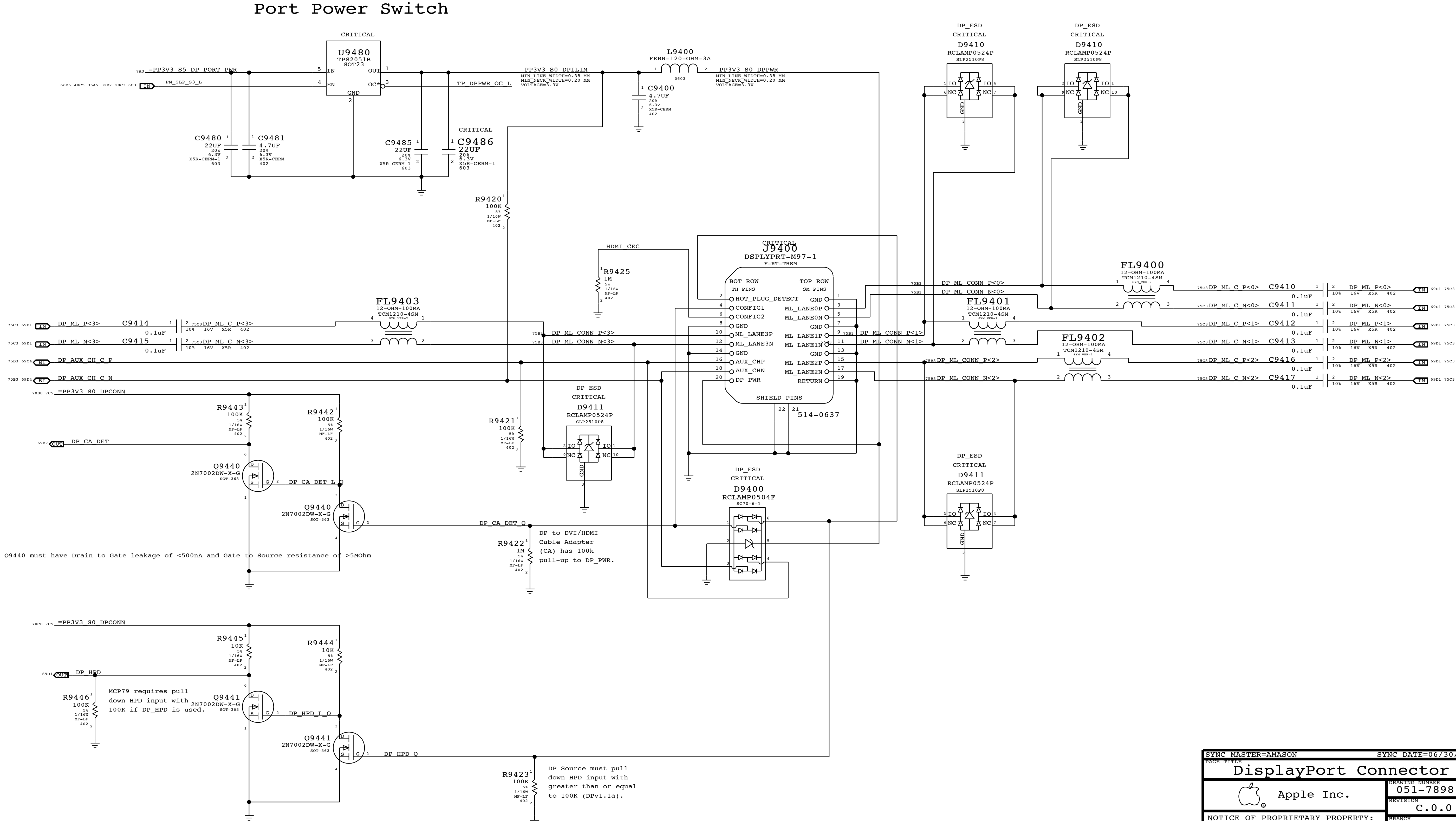
Port Power Switch



SYNC_MASTER=AMASON SYNC_DATE=06/30/2008

PAGE TITLE

DisplayPort Connector

Apple Inc.

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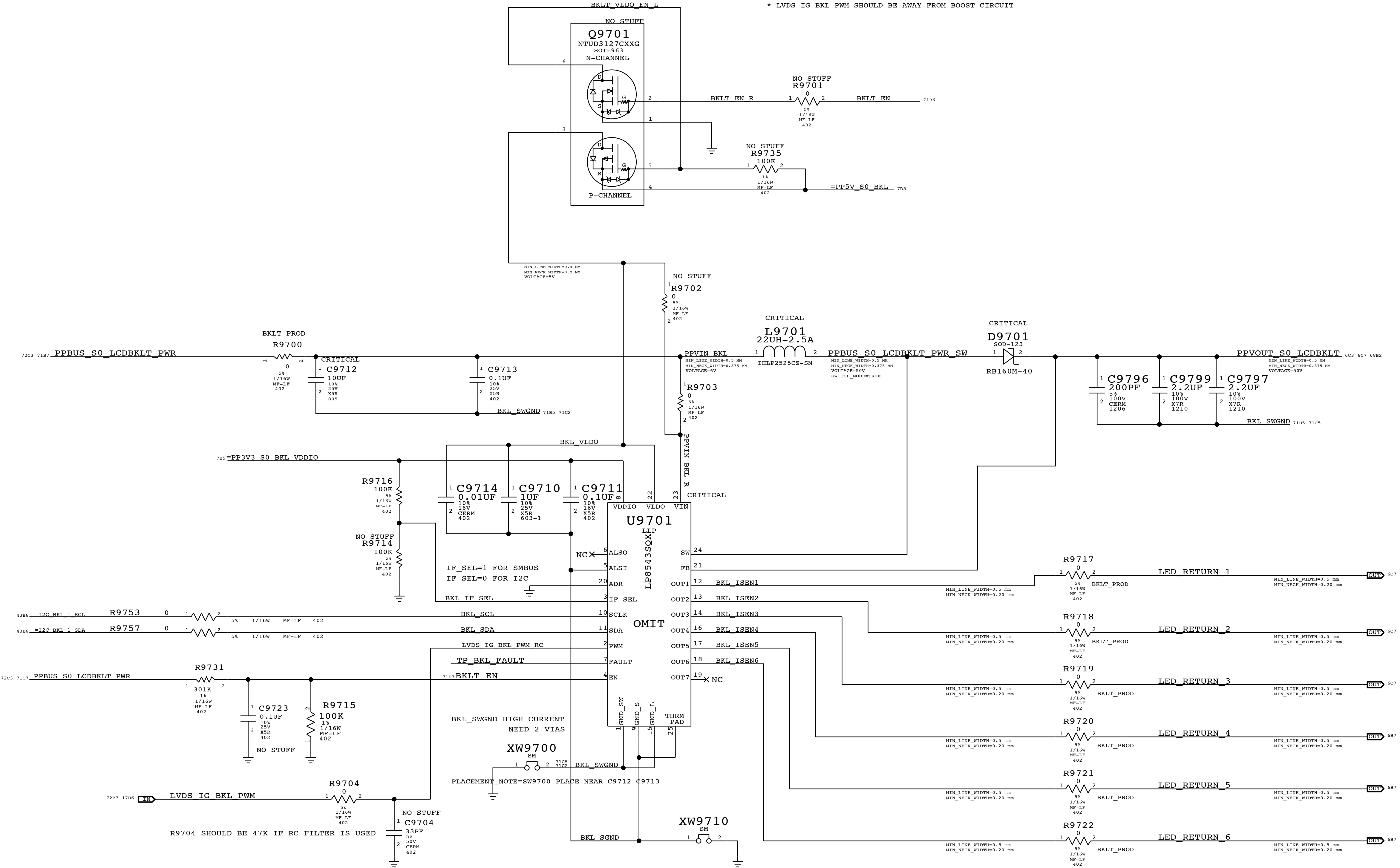
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
* LVDS_IG_BKL_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	6	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719,R9720,R9721,R9722		BKLT_ENG
116S0005	1	RES,1/16W,0.1 OHM,1%,0402,SM	R9700		BKLT_ENG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2670	1	IC,LP8543,WHT LED BKLT CTRLR,QFN24,PROD	U9701	CRITICAL	

SYNC MASTER=KIRAN SYNC DATE=12/05/2008

PAGE TITLE
LCD BACKLIGHT DRIVER

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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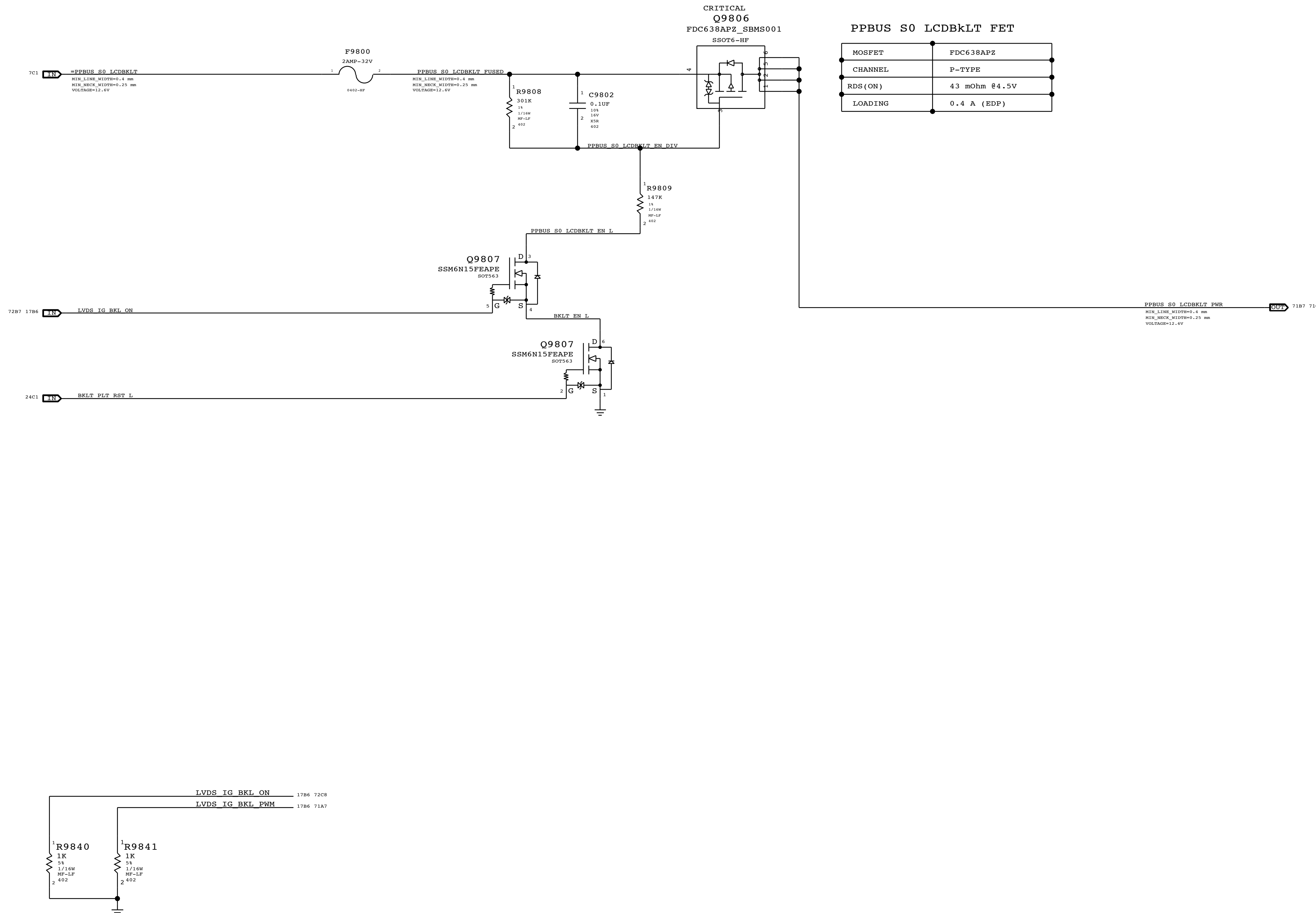

PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

MCP HAS INTERNAL 10K PULL-UP FOR THESE SIGNALS

SYNC_MASTER=YITE SYNC_DATE=06/30/2008

PAGE TITLE

LCD Backlight Support

Apple Inc.

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGE REFS
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	9C4 13D3
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	9C4 13D6
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	9C4 13D6
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	9C4 13D6
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	9B4 9C4 13C3 13D3
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	9B4 13D6
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	9B4 13D6
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	9B4 13D6
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	9C2 13B3 13C3
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	9C2 13D6
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	9C2 13D6
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	9C2 13D6
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	9B2 9C2 13B3
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	9B2 13D6
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	9B2 13D6
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	9B2 13D6
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	9D8 13C6 13D6
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	9D8 13B6
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	9D8 13B6
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	9C8 9D8 13C6
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	9C8 13B6
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	9D6 13B6
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9D6 13B6
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	9D6 13B3
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	9D6 13B3
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	9D6 13B6
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9D6 12C2 13A3
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	9D6 13A6
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	9D6 13B6
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	9C8 13A3
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	8B2 9B4
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	9C8 13B7
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	9C8 13A3
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	9D6 13A3
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	9C8 13A3
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	9B8 13A3
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	9C5 13B6 41D4 62C8
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	9B2 12C7 13A3
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	9B8 13A3
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	9C8 13A3
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	9C6 13B7 41C4
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	9B2 13A3
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	9B2 13A3
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9B2 13A3 62C7
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	9B2 13A3
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	13A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	13A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	13A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	13A6
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	9B6 13B3
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	9B6 13B3
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	12C3 13B3
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	12C3 13B3
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	13A4
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	13A4
	CPU_IERR_L	CPU_50S		CPU_IERR_L	9D6
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	20C7 62D8
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	62C7
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	9B4 25B1
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	9B3
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	9B3
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	9B3
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	9B3
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	9B6 9C6 12B3
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	9B6 9C6 12B3
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	9B6 9C6 12B3
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	9A6 9C6 12B6
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	9A6 9C6 12B3
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	9C6 12C6
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	9C5 12C6
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	12C4
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	10B6 62C7
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	10B5 62A5
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	10A5 62A5
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	

SYNC MASTER=T18 MLB SYNC DATE=01/04/2008

PAGE TITLE
CPU/FSB Constraints

Apple Inc.

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	14B5 26C5 26C7
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	14B5 26C5 26C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	14A5 26D5 26D7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	14B5 26C5 26C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	14B5 26C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	14B5 14C5 26C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	14C5 26C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	14C5 26C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	14C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	14C5 26C7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	14B7 26C2 26C4 26D2 26D4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	14B7 26C2 26C4
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	14B7 14C7 26B2 26B4 26C2 26C4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	14C7 26C2 26C4
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	14C7 26B5 26B7 26C5 26C7
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	14C7 14D7 26B5 26B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	14D7 26B5 26B7
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	14D7 26A5 26A7 26B5 26B7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	14A7 26C4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	14A7 26C2
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	14B7 26B4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	14B7 26C2
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	14B7 26B5
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	14B7 26B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	14B7 26B5
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	14B7 26A7
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	14D5 26C2
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	14D5 26D2
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	14D5 26C4
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	14D5 26C4
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	14D5 26B2
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	14D5 26C2
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	14D5 26C4
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	14D5 26C4
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	14D5 26B7
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	14D5 26B7
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	14D5 26B5
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	14D5 26B5
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	14D5 26B7
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	14D5 26B7
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	14D5 26A5
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	14D5 26A5
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	14B1 27C5 27C7
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	14B1 27C5 27C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	14A1 27D5 27D7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	14B1 27C5 27C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	14B1 27C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	14B1 14C1 27C5 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	14C1 27C5 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	14C1 27C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	14C1 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	14C1 27C7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	14B3 27C2 27C4 27D2 27D4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	14B3 27C2 27C4
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	14B3 14C3 27C2 27C4
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	14C3 27B2 27B4 27C2 27C4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	14C3 27B5 27B7 27C5 27C7
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	14C3 14D3 27B5 27B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	14D3 27B5 27B7
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	14D3 27A5 27A7 27B5 27B7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	14A3 27C4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	14A3 27C2
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	14B3 27C2
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	14B3 27B4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	14B3 27B5
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	14B3 27B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	14B3 27B5
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	14B3 27A7
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	14D1 27C2
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	14D1 27D2
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	14D1 27C4
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	14D1 27C4
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	14D1 27C4
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	14D1 27C4
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	14D1 27B2
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	14D1 27C2
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	14D1 27B7
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	14D1 27B7
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	14D1 27B5
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	14D1 27B5
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	14D1 27B7
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	14D1 27B7
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	14D1 27A5
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	14D1 27A5
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	15C6
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	15C6

SYNC MASTER=T18 MLB SYNC DATE=01/04/2008

PAGE TITLE
Memory Constraints

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_90D_HDD	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	6D5 29C7
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	6D5 29C7
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	16B3 29C5
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	16B3 29C5
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	6D5 16B6 29C7
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	6D5 16B6 29C7
	PCIE_90D	PCIE	PCIE_FW_R2D_P	34C3
	PCIE_90D	PCIE	PCIE_FW_R2D_N	34C3
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	16B3 34C1
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	16B3 34C1
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	16B6 34C1
	PCIE_90D	PCIE	PCIE_FW_D2R_N	16B6 34C1
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	34C3
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	34C3
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	16C3 29C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	16C3 29C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	6D5 29C7
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	6D5 29C7
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	16A6
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	69D1 70C1 70C8
	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	70C2 70C7
DP_ML	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	69D1 70C1 70C8
	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	70C2 70C7
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	17B6 69C7
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	17B6 69C7
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	69C6
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	69C5
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	69C4 70C8
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	69D4 70C8
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	17A6 23C7
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	17A6 23C7
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	17B3 68B3
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P	6C7 68C2
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	17B3 68B3
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N	6C7 68C2
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	6C7 17B3 68C2
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	6C7 17B3 68C2
I183 DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	70C3 70C4 70C5
I182	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	70C3 70C4 70C5
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	17A3 23C6
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	17A3 23C6
SATA_HDD_R2D	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_P	19D6 37A2
	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_N	19D6 37A2
	SATA_90D_HDD	SATA	SATA_HDD_R2D_P	6B7 37A5
	SATA_90D_HDD	SATA	SATA_HDD_R2D_N	6B7 37A5
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_P	37A4
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_N	37A4
SATA_HDD_D2R	SATA_90D_HDD	SATA	SATA_HDD_D2R_P	19D6 37B2
	SATA_90D_HDD	SATA	SATA_HDD_D2R_N	19D6 37B2
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_P	6B7 37B5
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_N	6B7 37B5
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_P	37B4
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_N	37B4
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	19D6 37C3
	SATA_100D	SATA	SATA_ODD_R2D_C_N	19D6 37C3
	SATA_100D	SATA	SATA_ODD_R2D_P	6B7 37C6
	SATA_100D	SATA	SATA_ODD_R2D_N	6A7 6B7 37C6
	SATA_100D	SATA	SATA_ODD_R2D_UF_P	37C4
	SATA_100D	SATA	SATA_ODD_R2D_UF_N	37C4
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	19D6 37C3
	SATA_100D	SATA	SATA_ODD_D2R_N	19D6 37C3
	SATA_100D	SATA	SATA_ODD_D2R_C_P	6B7 37C6
	SATA_100D	SATA	SATA_ODD_D2R_C_N	6B7 37C6
	SATA_100D	SATA	SATA_ODD_D2R_UF_P	37C4
	SATA_100D	SATA	SATA_ODD_D2R_UF_N	37C4
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	19A6

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

PAGE TITLE
MCP Constraints 1

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	12C3 18D7
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	18D2 18D7
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	18D2 18D7
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L	
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L	
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L	
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	18C5
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	18C5
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	18B3 40C8 42D3 42D5
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	18C3 40C8 42D5
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	18C3 24D4
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	18B3 24B4
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	24B1 40C8
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	24B1 42D3
USB_EXTA	USB_90D	USB	USB_EXTA_P	19D3 38A8
	USB_90D	USB	USB_EXTA_N	19D3 38A8
	USB_90D	USB	USB_EXTA_MUXED_P	38C4
	USB_90D	USB	USB_EXTA_MUXED_N	38C4
	USB_90D	USB	CONN_USB_EXTA_P	38C3
	USB_90D	USB	CONN_USB_EXTA_N	38C3
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	19D3 29B5
	USB_90D	USB	USB_CAMERA_N	19D3 29B5
	USB_90D	USB	USB_CAMERA_CONN_P	6D5 29B7
	USB_90D	USB	USB_CAMERA_CONN_N	6D5 29B7
USB_BT	USB_90D	USB	USB_BT_P	19D3 29B5
	USB_90D	USB	USB_BT_N	19C3 29B5
	USB_90D	USB	CONN_USB2_BT_P	6D5 29B7
	USB_90D	USB	CONN_USB2_BT_N	6D5 29B7
USB_TPAD	USB_90D	USB	USB_TPAD_P	19D3 48B8
	USB_90D	USB	USB_TPAD_N	19D3 48B8
	USB_90D	USB	USB_TPAD_R_P	48B7
	USB_90D	USB	USB_TPAD_R_N	48B7
USB_IR	USB_90D	USB	USB_IR_P	19D3 39D7
	USB_90D	USB	USB_IR_N	19D3 39D7
USB_EXTB	USB_90D	USB	USB_EXTB_P	19C3 38A4
	USB_90D	USB	USB_EXTB_N	19C3 38B4
	USB_90D	USB	CONN_USB_EXTB_P	38B3
	USB_90D	USB	CONN_USB_EXTB_N	38B3
USB_SD	USB_90D	USB	USB_CARDREADER_P	19C3 30C7
	USB_90D	USB	USB_CARDREADER_N	19C3 30C7
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	19C4
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	12B6 20C3 43D8
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	12B6 20C3 43D8
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	20C3 43B8
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	20C3 43B8
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	20D2 52C7
	HDA_55S	HDA	HDA_BIT_CLK_R	20A7 20D4
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	20D2 52C7
	HDA_55S	HDA	HDA_SYNC_R	20A7 20D4
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	20A7 20D4
	HDA_55S	HDA	HDA_RST_L	20D2 52C7
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	20D7 52C7
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	20D2 52C7
	HDA_55S	HDA	HDA_SDOUT_R	20A7 20D4
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	20C7
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	20B3 24B4
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	24B1 40C5
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	20B3 42A5 42C8
	SPI_55S	SPI	SPI_CLK	51C5
	SPI_55S	SPI	SPI_ALT_CLK	42C5 42D3
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	20B3 42A5 42C7
	SPI_55S	SPI	SPI_MOSI	51C4
	SPI_55S	SPI	SPI_ALT_MOSI	42C5 42D5
SPI_MISO	SPI_55S	SPI	SPI_MISO	20B3 42A5 42B7
	SPI_55S	SPI	SPI_MISO_R	51C4
	SPI_55S	SPI	SPI_ALT_MISO	42B5 42D5
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	20B3 42B7
	SPI_55S	SPI	SPI_CS0_L	
	SPI_55S	SPI	SPI_CS1_R_L	
	SPI_55S	SPI	SPI_CS1_R_L_USE_MLB	

SYNC MASTER=T18 MLB SYNC DATE=12/14/2007

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MCP Constraints 2

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	REFERENCES
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	17C6
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	17C6
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	17C3 32A5
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	31B6 32A3
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	17C3 31B6
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	17D3 31B6
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	31C4
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	17D6 31C1
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	31C4
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	17D6 31C1
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	17D6 31C1
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	17D6 31B1
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	31B4
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	31C6
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	17D3 31C8
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	17D3 31C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	17D3 31C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	17D3 31B6
	ENET_MII_55S	ENET_MII	ENET_RESET_L	17C3 31B7
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	31B3 33B8 33C8
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	31B3 33B8 33C8
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_P<3..0>	33B4 33C4 33C5
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_N<3..0>	33B4 33C4 33C5

SYNC_MASTER=T18_MLB SYNC_DATE=03/19/2008

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Ethernet Constraints

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

SD CARD INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	Net	
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	34B6 36C4
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	34C6 36C4
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	34B6 36C4
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	34B6 36C4
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	34B6 36B8
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	34B6 36B8
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	34B6 36B8
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	34B6 36B8

Port 2 Not Used

SD CARD NET PROPERTIES

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	Net	
I23	SD_DATA	SD_55S	SD_INTERFACE	SD_D<0>	30C2
I24	SD_DATA	SD_55S	SD_INTERFACE	SD_D<1>	30C2
I25	SD_DATA	SD_55S	SD_INTERFACE	SD_D<2>	30C2
I26	SD_DATA	SD_55S	SD_INTERFACE	SD_D<3>	30C2
I27	SD_DATA	SD_55S	SD_INTERFACE	SD_D<4>	30C2
I28	SD_DATA	SD_55S	SD_INTERFACE	SD_D<5>	30C2
I29	SD_DATA	SD_55S	SD_INTERFACE	SD_D<6>	30C2
I30	SD_DATA	SD_55S	SD_INTERFACE	SD_D<7>	30C2
I32	SD_CLK	SD_55S	SD_INTERFACE	SD_CLK	30C2
I31	SD_CMD	SD_55S	SD_INTERFACE	SD_CMD	30C2

SYNC MASTER=K19 MLB SYNC DATE=12/01/2008

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FireWire Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	6C5 6D5 43D2
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	6C5 6D5 43D2
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	43C2
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	43C2
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	43D5
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	43D5
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	6A7 43C5
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	6A7 43C5
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	43B5
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	43B5

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P
	1TO1_DIFFPAIR		CHGR_CSI_N
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P
	1TO1_DIFFPAIR		CHGR_CSO_N

SYNC MASTER=T18 MLB SYNC DATE=01/04/2008

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SMC Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

K24 SENSOR NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
	DIFFPAIR		CHGR_CSO_R_P	45A8 59B3
	DIFFPAIR		CHGR_CSO_R_N	45A8 59B3
	DIFFPAIR		CPUTHMSNS_D2_P	46C5
	DIFFPAIR		CPUTHMSNS_D2_N	46C5
	DIFFPAIR		CPU_THERMD_P	9C6 46D5
	DIFFPAIR		CPU_THERMD_N	9C6 46D5
	DIFFPAIR		ISNS_CPUVTT_P	45B7
	DIFFPAIR		ISNS_CPUVTT_N	45B7
	DIFFPAIR		ISNS_P1V5S0MCP_P	
	DIFFPAIR		ISNS_P1V5S0MCP_N	
	DIFFPAIR		ISNS_PVCORES0MCP_P	
	DIFFPAIR		ISNS_PVCORES0MCP_N	
	DIFFPAIR		MCPTHMSNS_D2_P	6C7 46B5
	DIFFPAIR		MCPTHMSNS_D2_N	6C7 46B5
	DIFFPAIR		MCP_THMDIODE_P	20C3 46B5
	DIFFPAIR		MCP_THMDIODE_N	20C3 46B5

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K24 SPECIAL CONSTRAINTS

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K24 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?
5X_DIELECTRIC	*	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

SYNC MASTER=M97 MLB

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K24 RULE DEFINITIONS

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