1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2010-10-12

SCHEM,FLYING_DUTCHMAN,MLB,K91F

REV B RELEASE, 01/31/11

ALIASES RESOLVED

Schematic / PCB #'s

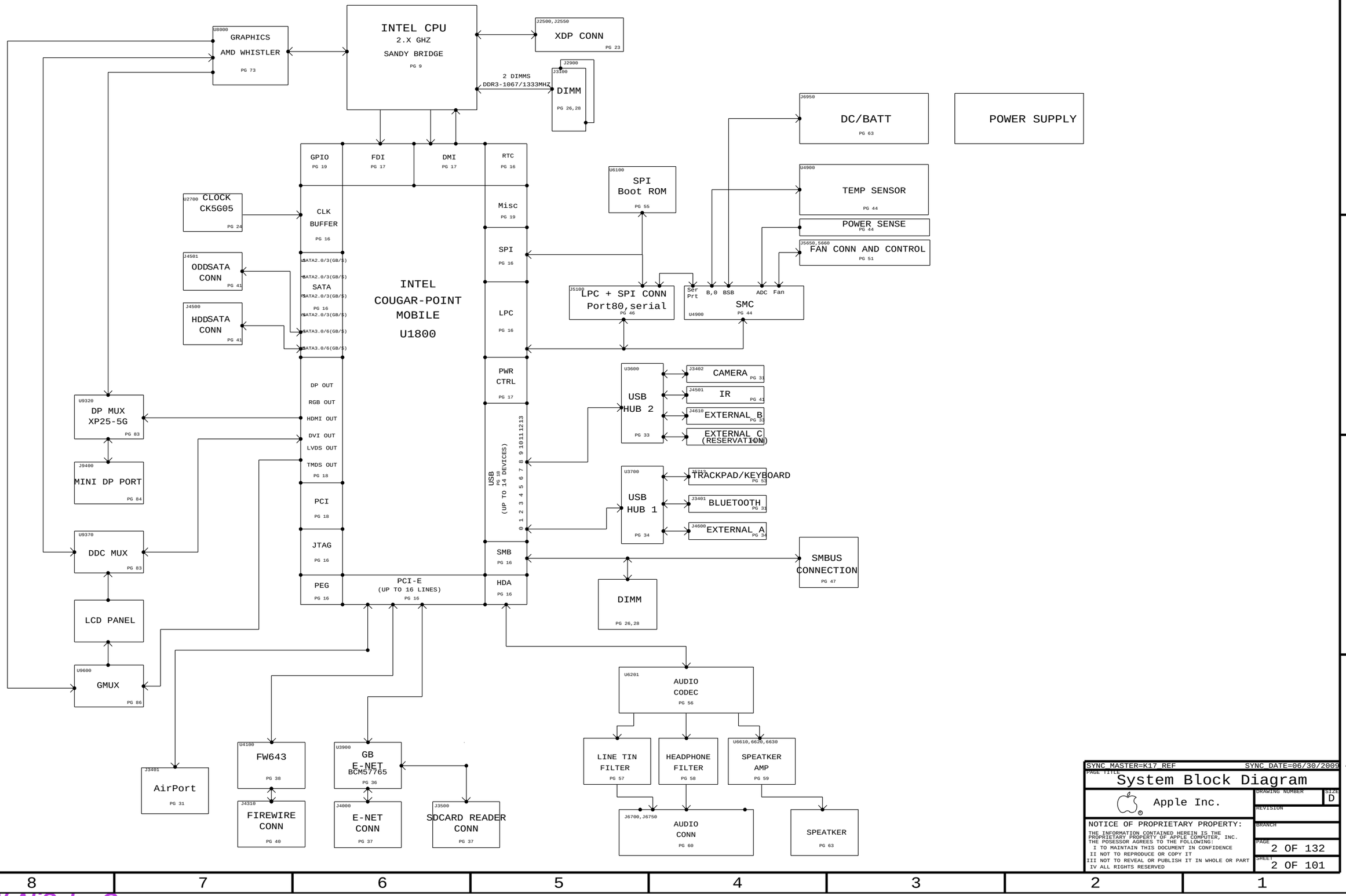
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8620	1	SCHEM,MLB,K91	SCH	CRITICAL	
820-2915	1	PCBF,MLB,K91	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Jan 31 12:49:37 2011

DRAWING TITLE: SCHEM,MLB,K91

Apple Inc.

DRAWING NUMBER | SIZE: D
REVISION
BRANCH
PAGE: 1 OF 132
SHEET: 1 OF 101



SYNC_MASTER=K17_REF SYNC_DATE=06/30/2009

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER | SIZE D

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K91 POWER SYSTEM ARCHITECTURE

J6900 AC ADAPTER IN — DCIN(16.5V) — F6905 6A FUSE — PP18V5_DCIN_CONN — R6990 — D6990 — PPBUS_G3H

R7020 — SMC_DCIN_ISENSE — U7000 ISL6259HRTZ PBUS SUPPLY/ BATTERY CHARGER (PAGE 64) — VIN — VOUT — PPVBAT_G3H

SMC_RESET_L

R7050 — SMC_BATT_ISENSE

F7040 8A FUSE — PPBUS_G3H

SMC_PBUS_VSENSE — Q5315 — ENABLE 3.425V G3HOT PM6640 U6990 (PAGE 62) — PP3V42_G3H

SMC PWRGD NCP303LSN U5000 (PAGE 45) — SMC_RESET_L

SMC AVREF SUPPLY REF3333 (PAGE 45) — VIN — VOUT — PP3V3_S5_AVREF_SMC

PP3V3_S5_SMC

SMC_TPAD_RST_L — SMC_ONOFF_L — U5001

J6950 — 3S2P (9 TO 12.6V) — PPVBATT_G3H_CONN — Q7055 — CHGR_BGATE — PPVBAT_G3H_CHGR_R

PP5V_S3_GFXIMVP6_VDD — GPU VCORE ISL6263C U8900 (PAGE 82) — VIN — VOUT — VR_ON — PGOOD — R5388/U5388

U5410 — SMC_GPU_ISENSE — SMC_GPU_VSENSE — PPVCORE_GPU

GPUVCORE_EN — GPUVCORE_PGOOD

PP5V_S0_CPUVTTS0 — 1.05V ISL95870 U7600 (PAGE 70) — CPUVTTS0_EN — CPUVTTS0_PGOOD

R7640 — PPCPUVTT_S0 — SMC_CPU_FSB_ISENSE

TPS22924 U4202 (PAGE 39) — PP1V0_FW_FWPHY — FW_PWR_EN

SMC_CPU_HI_ISENSE — CPU VCORE ISL95831 U7400 (PAGE 67) — VIN — VOUT — VR_ON — PGOOD — CPUIMVP7_VR_ON

SMC_CPU_ISENSE — SMC_CPU_VSENSE — PPVCORE_S0_CPU

CPUIMVP7_AXG_PGOOD

COUGAR_POINT U1800 (PAGE 16~21) — PWRBTN — SYS_RESET — RSMRST — ACPRESENT — PLTRST — PROCPWRGD — DRAMPWROK — PS_PWRGD

PM_PWRBTN_L — PLT_RERST_L — CPU_PWRGD — PM_MEM_PWRGD

PM_PCH_PWRGD — U2850

GMUX U9600 XP25-5 (PAGE 86)

PB16B EG_RAIL1_EN — P1V1GPU_EN
PB17A EG_RAIL2_EN — P3V3GPU_EN
PB17B EG_RAIL3_EN — GPUVCORE_EN
PB18A EG_RAIL4_EN
PL32A — PM_ALL_GPU_PGOOD

SMC U4900 (PAGE 44) — P60 — SMC_PM_G2_EN — RC DELAY — P3V3S5_EN

PP5V_S3_DDRREG

P1V0GPU_EN — EN1 VIN VOUT1 1.003V(L/H) EN2 VOUT2 1.503V(R/H) ISL6236 U9500 (PAGE 85) POK1 POK2 — P1V0GPU_PGOOD — P1V5FB_PGOOD — P1V5FB_EN

R5413 — PP1V5_GPU_REG — SMC_GPU_1V8_ISENSE — PP1V0_S0GPU_REG

DDRREG_EN — DDRVTT_EN

VIN VLDOIN 1.5V S5 VOUT1 — 0.75V S3 VOUT2 — TPS51116 U7300 (PAGE 66) — PGOOD

PPDDR_S3_REG — PPVTT_S0_DDR_LDO — DDRREG_PGOOD

R7350 — SMC_DDR_ISENSE — U5440 — SMC_CPU_DDR_VSENSE — PP1V5_S3

4.5V VIN MAX8840 EN U6200 — VOUT — PP3V3_S0 — PP4V5_AUDIO_ANALOG

CPU U1000 (PAGE 9~14) — SM_DRAMPWROK — VCCCPUPWRGD — RESET#

P1V5CPU_EN — VIN ON SLG5AP020 U7801 G — PP1V5_S3 — Q7801 — PP1V5_S3RS0 — P1V5S0FET_GATE

Q7860 — PP5V_S0 — P5VS0_EN

P5VS3_EN — P3V3S5_EN — VIN VREG5 5V (L/H) 3.3V (R/H) TPS51125 U7201 (PAGE 65) EN1 EN2 VOUT1 VOUT2 PGOOD — PP5V_S3 — PP3V3_S5

Q9806 — BKLT_PLT_RST_L && LCD_BKLT_NO — BKLT_EN — VIN LP8550 U9701 (PAGE 87) ENA VOUT — PPVOUT_S0_LCDBKLT — P5V3V3_PGOOD

Q4260 — PFWBOOST — SMC_ADAPTER_EN&&PM_SLP_S3_L

Q7870 — PP3V3_S0GPU — P3V3GPU_EN

Q7810 — PP3V3_S3 — P3V3S3_EN

Q7830 — PP3V3_S0_FET — P3V3S0_EN

TPS22924 U4201 (PAGE 39) — EN — PP3V3_FW_FWPHY — FW_PWR_EN

Q7922 — PP3V3_ENET — PM_SLP_S3_L&&WOL_EN||SMC_ADAPTER_EN

PP1V8_S0 — P1V8FB_EN — VIN ON SLG5AP020 U7880 G — PP1V8_GPUIFPX — Q7880 — P1V8GPUIFPXFET_GATE

U7980 — PM_ALL_GPU_PGOOD — ALL_SYS_PWRGD — RSMRST_PWRGD — SMC_ONOFF_L — PP3V3_S0_PWRCTL — P1V8S0_PGOOD — P5V3V3_PGOOD — S0PGOOD_PWROK

SMC H8S2117 U4900 (PAGE 45)

PWRGD(P12) — RSMRST_IN(P13) — RSMRST_OUT(P61) — 99ms DLY — PWR_BUTTON(P90) — IMVP_VR_ON(P16) — SYSRST(P43) — P17(BTN_OUT) — RES*

SMC_ADAPTER_EN — PM_RSMRST_L — CPUIMVP_VR_ON — PM_SYSRST_L — PM_PWRBTN_L — SMC_RESET_L

PM_SLP_S5_L — SLP_S5_L(P95)
PM_SLP_S4_L — SLP_S4_L(P94)
PM_SLP_S3_L — SLP_S3_L(P93)

COUGAR-POINT MOBILE U1800 (PAGE 16~21)

SLP_S5#(E4) — PM_SLP_S5_L — RC DELAY — P5VS3_EN
RC DELAY — DDRREG_EN
— P3V3S3_EN
SLP_S4#(H7) — PM_SLP_S4_L
SLP_S3#(P12) — PM_SLP_S3_L

R7978 — PM_SLP_S3_L_R

RC DELAY — P1V8S0_EN
RC DELAY — P1V2S0_EN
RC DELAY — CPUVTTS0_EN
RC DELAY — P1V5CPU_EN

P5VS0_EN
P3V3S0_EN
PBUSVSENS_EN

P1V8S0_EN — VIN ISL8014A U7720 (PAGE 70) EN VOUT PGOOD — PP1V8_S0 — P1V8S0_PGOOD

Q7850 — PP1V2_S0 — P1V2S0_EN

P1V2ENET_EN — VIN ISL8014A U7760 (PAGE 70) EN VOUT PGOOD — PP1V2_ENET — P1V2ENET_PGOOD

PP3V3_S0 — PP1V5_S0 — PP1V05_S0 — U7971 ISL88042IRTJJZ (PAGE 72) — VCC — V2MON — V3MON — V4MON — RST — TRST = 200mS

SYNC_MASTER=K17_REF — SYNC_DATE=06/30/2009

PAGE TITLE: Power Block Diagram

Apple Inc.

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SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Revision History

Apple Inc.

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1468	PCBA,MLB,K91F,DG64	K91_COMMON,SODIMM:FOXCONN,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DG64
639-1972	PCBA,MLB,K91F,DL83	K91_COMMON,SODIMM:HYBRID,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL83
639-1971	PCBA,MLB,K91F,DL82	K91_COMMON,SODIMM:MOLEX,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL82
639-1469	PCBA,MLB,K91F,DG65	K91_COMMON,SODIMM:FOXCONN,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DG65
639-1970	PCBA,MLB,K91F,DL86	K91_COMMON,SODIMM:HYBRID,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL86
639-1956	PCBA,MLB,K91F,DL7W	K91_COMMON,SODIMM:MOLEX,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL7W
639-1470	PCBA,MLB,K91F,DG66	K91_COMMON,SODIMM:FOXCONN,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DG66
639-1974	PCBA,MLB,K91F,DL87	K91_COMMON,SODIMM:HYBRID,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL87
639-1976	PCBA,MLB,K91F,DL88	K91_COMMON,SODIMM:MOLEX,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL88
639-1471	PCBA,MLB,K91F,DG67	K91_COMMON,SODIMM:FOXCONN,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DG67
639-1973	PCBA,MLB,K91F,DL81	K91_COMMON,SODIMM:HYBRID,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL81
639-1954	PCBA,MLB,K91F,DL7T	K91_COMMON,SODIMM:MOLEX,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL7T
639-1573	PCBA,MLB,K91,DHMV	K91_COMMON,SODIMM:FOXCONN,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DHMV
639-1945	PCBA,MLB,K91,DL7Q	K91_COMMON,SODIMM:HYBRID,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DL7Q
639-1953	PCBA,MLB,K91,DL7R	K91_COMMON,SODIMM:MOLEX,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DL7R
639-1574	PCBA,MLB,K91,DHMW	K91_COMMON,SODIMM:FOXCONN,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DHMW
639-1959	PCBA,MLB,K91,DL80	K91_COMMON,SODIMM:HYBRID,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DL80
639-1960	PCBA,MLB,K91,DL7Y	K91_COMMON,SODIMM:MOLEX,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DL7Y
085-1901	K91/K91F DEVELOPMENT BOM	K91_DEVEL:ENG

K91 BOM GROUPS

BOM GROUP	BOM OPTIONS
K91_COMMON	ALTERNATE,COMMON,K91_COMMON1,K91_COMMON2,K91_PROGPARTS,K91_PROGPARTS1,UVGLUE_K91_K91F,K91_PVT
K91_COMMON1	CPUMEM_S0,SMC_DEBUG_YES,HUB1_2NONREM,HUB2_2NONREM,USBHUB_2513B
K91_COMMON2	GPUVID_1P11V,KB_BL,T29:YES,ENET_SD:B0,T29BST:Y,SDRV_PD,SDRVI2C:MCU,T29_DP_HPD:ALL_OR
K91_PVT	BMON:PROD,VREFMRGN_NOT,XDP,XDP_CPU_BPM,BKLT:PROD,ISNS_ON:NO,LPCPLUS_R:YES
K91_PROGPARTS	GMUX_PROG,IR_PROG,TPAD_PROG:PVT,ENETROM_PROG:PVT,T29ROM:PROG,T29MCU:PROG
K91_PROGPARTS1	SMC_PROG:PVT,BOOTROM_PROG:PVT
K91_DEVEL:ENG	SNB_CPT_XDP,BMON:ENG,GMUX_JTAG_CONN,VREFMRGN,LPCPLUS_CONN:YES,LPCPLUS_R:YES,BKLT:ENG,S0PGOOD_ISL,CPURIPPLE_ENG,IMVPISNS_ENG,ISNS_ON:YES,DEBUG_ADC,DIGI_MIC
K91_DEVEL:PVT	SNB_CPT_XDP,LPCPLUS_CONN:YES,LPCPLUS_R:YES
SNB_CPT_XDP	XDP,XDP_CONN,XDP_CPU_BPM,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4031	1	IC,CPU,SNB,SR030,PRQ,D2,2.0,45W,4+2,1.20,6M,BGA	U1000	CRITICAL	CPU:2_0GHZ
337S4032	1	IC,CPU,SNB,SR00W,PRQ,D2,2.2,45W,4+2,1.30,6M,BGA	U1000	CRITICAL	CPU:2_2GHZ
337S4033	1	IC,CPU,SNB,SR00U,PRQ,D2,2.3,45W,4+2,1.30,8M,BGA	U1000	CRITICAL	CPU:2_3GHZ
337S4029	1	IC,PCH,COUGARPOINT,SLH9D,PRQ,BD82HM65	U1800	CRITICAL	
337S3936	1	IC,GPU,AMD,WHISTLER,962FCBGA,40NM,ES	U8000	CRITICAL	GPU:WHISTLER
337S3979	1	IC,GPU,AMD,SEYMOUR,M2 LP,ES1,962BGA	U8000	CRITICAL	GPU:SEYMOUR
338S0945	1	IC,ASSP,LIGHTRIDGE,S LHAJ,PRQ,FCBGA,15X15MM	U3600	CRITICAL	T29:YES
343S0534	1	IC,ASIC,GBIT ETHNET&SD CTRLR,686 QFN8X8,B0	U3900	CRITICAL	ENET_SD:B0
343S0494	1	IC,ASIC,GBIT ETHNET&SD CTRLR,686 QFN8X8,A0	U3900	CRITICAL	ENET_SD:A0
338S0753	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
333S0543	4	IC,SGRAM,GDDR5,32MX32.1.25GHz,E-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_512_SAMSUNG
333S0564	4	IC,SDRAM,GDDR5,32MX32,1.25GHz,A-DIE1.35V	U8400,U8450,U8500,U8550	CRITICAL	FB_512_HYNIX
333S0571	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,C-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_SAMSUNG
333S0572	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,M-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_HYNIX
333S0543	2	IC,SGRAM,GDDR5,32MX32.1.25GHz,E-DIE,HF	U8500,U8550	CRITICAL	FB_256_SAMSUNG
333S0564	2	IC,SDRAM,GDDR5,32MX32,1.25GHz,A-DIE1.35V	U8500,U8550	CRITICAL	FB_256_HYNIX
353S3055	1	IC,PI3VEDP212,X2 DISPLAYPORT 2:1 MUX,QFN	U9390	CRITICAL	
725-1479	1	MLB LOCTITE UV EB CPU,PCH,T29,GPU,K91	UV_GLUE_K91_K91F	CRITICAL	UVGLUE_K91_K91F
516S0806	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,FOXCONN	J3100	CRITICAL	SODIMM:FOXCONN
516-0246	1	CONN,204P,SODIMM,SOCKET,DDR3,P=0.6M,FOXCONN	J2900	CRITICAL	SODIMM:FOXCONN
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:MOLEX
516-0245	1	CONN,204P,SODIMM,SOCKET,DDR3,P=0.6M,MOLEX	J2900	CRITICAL	SODIMM:MOLEX
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:HYBRID
516-0246	1	CONN,204P,SODIMM,SOCKET,DDR3,P=0.6M,FOXCONN	J2900	CRITICAL	SODIMM:HYBRID

ETHERNET ROM

335S0663	1	IC,FLASH,SERIAL,SPI,1MBIT,2V7,8P,SOIC	U3990	CRITICAL	ENETROM_BLANK
341S2685	1	IC,ENET,1MBITFLASH,CIV REV01,K74/K75,K40	U3990	CRITICAL	ENETROM_PROG:A0_SD
341S2973	1	IC,ENET,1MBITFLASH,CIV REV01,K60/K62	U3990	CRITICAL	ENETROM_PROG:B0_SD
341S3026	1	IC,ENET,1MBITFLASH,CIV REV01,K901/K91/K92	U3990	CRITICAL	ENETROM_PROG:EVT
341S3096	1	IC,ENET ROM,1MBIT,DVT,PVT,K901/K91x	U3990	CRITICAL	ENETROM_PROG:PVT

Alternate Parts

(Alternate) (Primary)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
353S2805	353S2603		ALL	Fairchild wafer option
128S0264	128S0257		ALL	Sanyo alt to Kemet
128S0303	128S0282		ALL	Panasonic alt to Sanyo
353S3085	353S1658		ALL	ST Micro alt to LT
376S0972	376S0612		ALL	ROHM alt to Toshiba N-FET
376S0855	376S0613		ALL	Diodes alt to Toshiba dual N-FET
138S0676	138S0691		ALL	Murata alt to Samsung cap
138S0652	138S0648		ALL	Samsung / Murata alt for Taiyo Yuden
138S0681	138S0638		ALL	Taiyo Yuden alt for Samsung
152S0685	152S0796		ALL	Sale/Vishay/TDK alt for Cyntec
376S0977	376S0859		ALL	Diodes alt for Rohm
353S2592	353S3199		ALL	1024x1 24BIT CMOS OLED REV 3C ULTRAVUE FOR NON MDU
335S0550	335S0777		ALL	add 4K byte as alternative to 2K
371S0679	371S0652		ALL	NXP alternate for pin diodes
138S0671	138S0673		ALL	Taiyo Yuden alt for Murata 10 uF caps

EFI ROM

335S0740	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341S2893	1	IC,EFI,ROM,PROTO0, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S2934	1	IC,EFI,ROM,PROTO1, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S2991	1	IC,EFI,ROM,PROTO2, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S2894	1	IC,EFI,ROM,EVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:EVT
341S2895	1	IC,EFI,ROM,DVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:DVT
341S2896	1	IC,EFI,ROM,PVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PVT

PSOC

341S2902	1	IC,TP PSOC,K9x,PROTO0	U5701	CRITICAL	TPAD_PROG:PROTO0
341S2940	1	IC,TP PSOC,K9x,PROTO1	U5701	CRITICAL	TPAD_PROG:PROTO1
341S3001	1	IC,TP PSOC,K9x,PROTO2	U5701	CRITICAL	TPAD_PROG:PROTO2
341S3024	1	IC,TP PSOC,K9x,EVT	U5701	CRITICAL	TPAD_PROG:EVT
341S3099	1	IC,TP PSOC,K9x,DVT,PVT	U5701	CRITICAL	TPAD_PROG:PVT

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DDKG]	CRITICAL	EEEE:DDKG
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG63]	CRITICAL	EEEE:DG63
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG64]	CRITICAL	EEEE:DG64
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG65]	CRITICAL	EEEE:DG65
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG66]	CRITICAL	EEEE:DG66
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG67]	CRITICAL	EEEE:DG67
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DHMV]	CRITICAL	EEEE:DHMV
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DHMW]	CRITICAL	EEEE:DHMW
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL81]	CRITICAL	EEEE:DL81
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL82]	CRITICAL	EEEE:DL82
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL83]	CRITICAL	EEEE:DL83
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL84]	CRITICAL	EEEE:DL84
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL85]	CRITICAL	EEEE:DL85
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL86]	CRITICAL	EEEE:DL86
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL87]	CRITICAL	EEEE:DL87
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL88]	CRITICAL	EEEE:DL88
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL89]	CRITICAL	EEEE:DL89
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7Q]	CRITICAL	EEEE:DL7Q
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7R]	CRITICAL	EEEE:DL7R
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7T]	CRITICAL	EEEE:DL7T
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7V]	CRITICAL	EEEE:DL7V
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7W]	CRITICAL	EEEE:DL7W
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7Y]	CRITICAL	EEEE:DL7Y
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL80]	CRITICAL	EEEE:DL80

Programmables - All Builds

341S2830	1	IC,CPLD,LATTICE,GMUX,K91/K91F	U9600	CRITICAL	GMUX_PROG
336S0042	1	IC,PLD,LATTICE,LFXP2-5E-5,132 BALL CSBGA	U9600	CRITICAL	GMUX_BLANK
341S2384	1	IR,ENCORE II,CY7C63833-LFXC	U4800	CRITICAL	IR_PROG
341S3129	1	IC,T29 EEPROM,PVT,K9x	U3690	CRITICAL	T29ROM:PROG
335S0777	1	IC,EEPROM,SERIAL,8KB,SOIC	U3690	CRITICAL	T29ROM:BLANK
341S3128	1	IC,PROGRMD,LPC1112A,T29 PORT MCU,PVT,HVQFN25	U9330	CRITICAL	T29MCU:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S2957	1	IC,GPU ROM,K91/F,K92,PROG	U8701	CRITICAL	GPUROM:PROG
335S0724	1	IC,GPU ROM,K91/F,K92,BLANK	U8701	CRITICAL	GPUROM:BLANK

SMC

338S0895	1	IC,SMC,HSB/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2854	1	IC,SMC,DEVELOPMENT-PROTO0,K91	U4900	CRITICAL	SMC_PROG:PROTO0
341S2935	1	IC,SMC,DEVELOPMENT-PROTO1,K91	U4900	CRITICAL	SMC_PROG:PROTO1
341S2994	1	IC,SMC,DEVELOPMENT-PROTO2,K91	U4900	CRITICAL	SMC_PROG:PROTO2
341S2861	1	IC,SMC,DEVELOPMENT-EVT,K91	U4900	CRITICAL	SMC_PROG:EVT
341S2864	1	IC,SMC,DEVELOPMENT-DVT,K91	U4900	CRITICAL	SMC_PROG:DVT
341S2867	1	IC,SMC,DEVELOPMENT-PVT,K91	U4900	CRITICAL	SMC_PROG:PVT

SYNC_MASTER=K17_REF SYNC_DATE=05/28/2009

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Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST

TRUE	PP5V S0	101	3 TPs per Fan
TRUE	FAN LT PWM	51	
TRUE	FAN LT TACH	51	

J5660 (RIGHT FAN CONN)

TRUE	PP5V S0	101	2 TPs
TRUE	FAN RT PWM	51	
TRUE	FAN RT TACH	51	
TRUE	GND		5 TPs per Fan

J6780 (MIC CONN)

TRUE	BI MIC N	60 61	
TRUE	BI MIC SHIELD	60 61	
TRUE	BI MIC P	60 61	

J6781 & J6782 (SPEAKERS CONN)

TRUE	SPKRCONN L OUT P	59 60 98
TRUE	SPKRCONN L OUT N	59 60 98
TRUE	SPKRCONN R OUT P	59 60 98
TRUE	SPKRCONN R OUT N	59 60 98
TRUE	SPKRCONN S OUT P	59 60 98
TRUE	SPKRCONN S OUT N	59 60 98

J9000 (LVDS CONN)

TRUE	PP3V3 SW LCD	84 87 88 89 90 82	
TRUE	PP3V3 S0	84 87 88 89 90 82	
TRUE	PPVOUT S0 LCDBKLT	26 28 32 35 36 37 40 41 45 47	2 TP needed
TRUE	LVDS DDC CLK	82 83	
TRUE	LVDS DDC DATA	82 83	
TRUE	LVDS CONN A DATA P<0>	82 83 97	
TRUE	LVDS CONN A DATA N<0>	82 83 97	
TRUE	LVDS CONN A DATA P<1>	82 83 97	
TRUE	LVDS CONN A DATA N<1>	82 83 97	
TRUE	LVDS CONN A DATA P<2>	82 83 97	
TRUE	LVDS CONN A DATA N<2>	82 83 97	
TRUE	LVDS CONN A CLK F P	82 97	
TRUE	LVDS CONN A CLK F N	82 97	
TRUE	LVDS CONN B DATA P<0>	82 83 97	
TRUE	LVDS CONN B DATA N<0>	82 83 97	
TRUE	LVDS CONN B DATA P<1>	82 83 97	
TRUE	LVDS CONN B DATA N<1>	82 83 97	
TRUE	LVDS CONN B DATA P<2>	82 83 97	
TRUE	LVDS CONN B DATA N<2>	82 83 97	
TRUE	LVDS CONN B CLK F P	82 97	
TRUE	LVDS CONN B CLK F N	82 97	
TRUE	LED RETURN 1	82 88	
TRUE	LED RETURN 2	82 88	
TRUE	LED RETURN 3	82 88	
TRUE	LED RETURN 4	82 88	
TRUE	LED RETURN 5	82 88	
TRUE	LED RETURN 6	82 88	
TRUE	GND		4 TPs

J4500 (SATA ODD CONN)

TRUE	PP5V SW ODD	41	3 TPs
TRUE	SMC ODD DETECT	41 44	
TRUE	SATA ODD D2R C P	41	
TRUE	SATA ODD D2R C N	41	
TRUE	SATA ODD R2D P	41 92	
TRUE	SATA ODD R2D N	41 92	
TRUE	SATA ODD D2R UF P	41 92	
TRUE	SATA ODD D2R UF N	41 92	
TRUE	GND		5 TPs

J4501 (SATA HDD CONN)

TRUE	PP5V S0 HDD FLT	41
TRUE	SATA HDD R2D P	41 92
TRUE	SATA HDD R2D N	41 92
TRUE	SATA HDD D2R C N	41 92
TRUE	SATA HDD D2R C P	41 92
TRUE	GND	

J5815 (KBD BACKLIGHT CONN)

TRUE	KBDLED ANODE	53
TRUE	SMC KDBLED PRESENT L	53
TRUE	GND	

FUNC_TEST

TRUE	GND	
TRUE	GND	6 TPs

USB PORTS

TRUE	PP5V S3 RTUSB A F	42	
TRUE	USB2 LT1 N	42 98	
TRUE	USB2 LT1 P	42 98	
TRUE	GND		
TRUE	PP5V S3 RTUSB B F	42	
TRUE	USB LT2 N	42 98	
TRUE	USB LT2 P	42 98	
TRUE	GND		

J3401 & J3402 (AIRPORT/BT/CAMERA CONN)

TRUE	PCIE AP D2R P	16 31 93
TRUE	PCIE AP D2R N	16 31 93
TRUE	PCIE AP R2D P	31 93
TRUE	PCIE AP R2D N	31 93
TRUE	PCIE CLK100M AP CONN_P	31 98
TRUE	PCIE CLK100M AP CONN_N	31 98
TRUE	AP CLKREQ Q L	31
TRUE	PCIE WAKE L	17 25 31 84
TRUE	WIFI EVENT L	31 44 45
TRUE	AP RESET CONN L	31
TRUE	PP3V3 WLAN	31 45
TRUE	PP5V S3 ALSCAMERA F	31
TRUE	SMBUS SMC A S3 SDA	6 31 44 47 53 54 96
TRUE	SMBUS SMC A S3 SCL	6 31 44 47 53 54 96
TRUE	USB CAMERA CONN P	31 92
TRUE	USB CAMERA CONN N	31 92
TRUE	CONN USB2 BT P	98
TRUE	CONN USB2 BT N	98
TRUE	SMBUS SMC 0 S0 SCL	31 44 47 59 79 96
TRUE	SMBUS SMC 0 S0 SDA	31 44 47 59 79 96

J6950 (BAT CONN)

TRUE	SYS DETECT L	62

J5800 (IPD FLEX CONN)

TRUE	PP18V5 S4	53
TRUE	Z2 HOST INTN	52 53
TRUE	Z2 MOSI	52 53
TRUE	Z2 CS L	52 53
TRUE	Z2 DEBUG3	52 53
TRUE	Z2 MISO	52 53
TRUE	Z2 BOOST EN	53
TRUE	Z2 SCLK	52 53
TRUE	Z2 CLKIN	52 53
TRUE	Z2 KEY ACT L	52 53
TRUE	Z2 RESET	52 53
TRUE	PSOC F CS L	52 53
TRUE	PICKB L	52 53
TRUE	PSOC MISO	52 53
TRUE	PSOC MOSI	52 53
TRUE	PSOC SCLK	52 53
TRUE	SMBUS SMC A S3 SCL	6 31 44 47 53 54 96
TRUE	SMBUS SMC A S3 SDA	6 31 44 47 53 54 96

J6900 (DC POWER CONN)

TRUE	ADAPTER SENSE	62
TRUE	PP18V5 DCIN FUSE	62
TRUE	GND	

J6950 (MAIN BATT CONN)

TRUE	PPVBAT G3H CONN	62 63
TRUE	SMBUS SMC BSA SCL	6 44 47 62 63 96
TRUE	SMBUS SMC BSA SDA	6 44 47 62 63 96
TRUE	NC SMC BS ALRT L	6
TRUE	GND	

J6995 (BAT LED CONN)

TRUE	PP3V42 G3H	6 7 25 42 44 45 46 47 52 62 63 72
TRUE	SMBUS SMC BSA SDA	6 44 47 62 63 96
TRUE	SMBUS SMC BSA SCL	6 44 47 62 63 96
TRUE	SMC BIL BUTTON L	44 45 62
TRUE	GND	

J5713 (KEY BOARD CONN)

TRUE	PP3V3 S3	21 72 87
TRUE	PP3V42 G3H	21 72 87 48 51 72 78 79 93
TRUE	WS KBD1	52 53
TRUE	WS KBD2	52
TRUE	WS KBD3	52
TRUE	WS KBD4	52
TRUE	WS KBD5	52
TRUE	WS KBD6	52
TRUE	WS KBD7	52
TRUE	WS KBD8	52
TRUE	WS KBD9	52
TRUE	WS KBD10	52
TRUE	WS KBD11	52
TRUE	WS KBD12	52
TRUE	WS KBD13	52
TRUE	WS KBD14	52
TRUE	WS KBD15 CAP	52
TRUE	WS KBD16 NUM	52
TRUE	WS KBD17	52
TRUE	WS KBD18	52
TRUE	WS KBD19	52
TRUE	WS KBD20	52
TRUE	WS KBD21	52
TRUE	WS KBD22	52
TRUE	WS KBD23	52
TRUE	WS KBD ONOFF L	52
TRUE	WS LEFT SHIFT KBD	52
TRUE	WS LEFT OPTION KBD	52
TRUE	WS CONTROL KBD	52

J6950 (BIL CABLE CONN)

TRUE	PP5V S3 IR R	41
TRUE	SMC LID R	62
TRUE	IR RX OUT	41 43
TRUE	SYS LED ANODE	41 45
TRUE	GND	

FUNC_TEST

TRUE	BKLT EN	8 52
TRUE	TP ISSP SCLK P1 1	8 52
TRUE	TP ISSP SDATA P1 0	8 52
TRUE	LCD BKLT PWM	87 88
TRUE	LPCPLUS GPIO	19 46
TRUE	LPCPLUS RESET L	25 46 87 93
TRUE	LPC AD<0..3>	16 44 46 87 93
TRUE	LPC CLK33M LPCPLUS	25 46 93
TRUE	LPC FRAME L	16 44 46 87 93
TRUE	LPC PWRDWN L	17 44 46
TRUE	LPC SERIRQ	16 44 46
TRUE	PM CLKRUN L	17 44 46
TRUE	PM SYSRST L	17 25 44
TRUE	SMC MD1	44 46
TRUE	SMC NMI	44 46
TRUE	SMC ONOFF L	44 45 52
TRUE	SMC RESET L	42 44 45 46 63
TRUE	SMC RX L	42 44 45 46
TRUE	SMC TCK	44 45 46
TRUE	SMC TDI	44 45 46
TRUE	SMC TDO	44 45 46
TRUE	SMC TMS	44 45 46
TRUE	SMC TRST L	44 46
TRUE	SMC TX L	42 44 45 46
TRUE	SPIROM USE MLB	19 46 55
TRUE	SPI ALT CLK	46
TRUE	SPI ALT CS L	46
TRUE	SPI ALT MISO	46
TRUE	SPI ALT MOSI	46
TRUE	SYS LED ANODE R	41

NO_TEST=TRUE

TRUE	T29 D2R P<1..0>	33 84 95
TRUE	T29 D2R N<1..0>	33 84 95
TRUE	T29 D2R C P<1..0>	84 85 95
TRUE	T29 D2R C N<1..0>	84 85 95
TRUE	T29 R2D C P<1..0>	33 84 95
TRUE	T29 R2D C N<1..0>	33 84 95
TRUE	T29 R2D P<1..0>	84 95
TRUE	T29 R2D N<1..0>	84 95
TRUE	T29DPA ML P<3..0>	84 85 95
TRUE	T29DPA ML N<3..0>	84 85 95
TRUE	DP T29SNK0 AUXCH C P	33 78 95
TRUE	DP T29SNK0 AUXCH C N	33 78 95
TRUE	DP T29SNK0 AUXCH P	33 95
TRUE	DP T29SNK0 AUXCH N	33 95
TRUE	DP T29SNK0 ML C P<3..0>	33 78 95
TRUE	DP T29SNK0 ML C N<3..0>	33 78 95
TRUE	DP T29SNK0 ML P<3..0>	33 95
TRUE	DP T29SNK0 ML N<3..0>	33 95
TRUE	DP T29SNK1 AUXCH C P	33 78 95
TRUE	DP T29SNK1 AUXCH C N	33 78 95
TRUE	DP T29SNK1 AUXCH P	33 95
TRUE	DP T29SNK1 AUXCH N	33 95
TRUE	DP T29SNK1 ML C P<3..0>	33 78 95
TRUE	DP T29SNK1 ML C N<3..0>	33 78 95
TRUE	DP T29SNK1 ML P<3..0>	33 95
TRUE	DP T29SNK1 ML N<3..0>	33 95
TRUE	TP DP T29SRC AUXCH CN	33
TRUE	TP DP T29SRC AUXCH CP	33
TRUE	TP DP T29SRC ML CP<3..0>	33
TRUE	TP DP T29SRC ML CN<3..0>	33
TRUE	DP SDRVA ML C P<0>	84 95
TRUE	DP SDRVA ML C N<0>	84 95
TRUE	DP SDRVA ML C P<2>	84 95
TRUE	DP SDRVA ML C N<2>	84 95
TRUE	DP SDRVA ML P<0>	84 95
TRUE	DP SDRVA ML N<0>	84 95
TRUE	DP SDRVA ML P<2>	84 95
TRUE	DP SDRVA ML N<2>	84 95
TRUE	TP T29 PCIE RESET0 L	33
TRUE	TP T29 PCIE RESET1 L	33
TRUE	TP T29 PCIE RESET2 L	33
TRUE	TP T29 PCIE RESET3 L	33
TRUE	T29DPA D2R1 AUXCH N	85 95
TRUE	T29DPA D2R1 AUXCH P	85 95
TRUE	T29 D2R1 BIAS	

POWER RAILS

FUNC_TEST

TRUE	PM SLP S3 L	17 29 44
TRUE	PP0V75 S0 DDRVTT	66 72 26 28 29
TRUE	PP18V5 S3	44 67 69
TRUE	PP1V05 S0	17 28 72
TRUE	PP1V05 S0GPU	23 35 39
TRUE	PP1V05 S5	72 103
TRUE	PP1V0 FW FWPHY	7 38 39
TRUE	PP1V2 ENET	7 36 70
TRUE	PP1V2 S0	7 70 87
TRUE	PP1V5 S3	7 26 28 29
TRUE	PP1V5 S3RS0	66 71 98
TRUE	PP1V8R1V55 S0GPU_ISNS	
TRUE	PP1V8R1V55 S0GPU_ISNS_R	
TRUE	PP1V8 GPUIFPX	7 71 100
TRUE	PP1V8 S0	71 87
TRUE	PP3V3 ENET	7 14 17 20 22 25 78
TRUE	PP3V3 FW FWPHY	99 99 83
TRUE	PP3V3 S0	53 56 60 6 7 12 16
TRUE	PP3V3 S0GPU	32 38 39
TRUE	PP3V3 S3	39 40 41 49 50 51
TRUE	PP3V3 S5	61 73 74 84 87 88
TRUE	PP3V3 S5 AVREF_SMC	44
TRUE	PP3V42 G3H	20 47 48 25 42 48
TRUE	PP5V S0	72 86 88 53 64 67 68 69 71
TRUE	PP5V S3	41 46 53 68 69 71 101
TRUE	PP5V S5	7 53 65 71
TRUE	PPBUS G3H	63 88
TRUE	PPDCIN G3H	48 49 62 7 48 62 63
TRUE	PPVCORE GPU	7 48 74 81
TRUE	PPVCORE S0 CPU	7 12 14 48 68 101
TRUE	PPVCORE S0 GFX	
TRUE	PPVP FW	7 39 40
TRUE	PPVTTDDR S3	7 30 66

NC NO_TESTS

NO_TEST

TRUE	TP FW643 NAND TREE	38
TRUE	TP FW643 OCR10 CTL	38
TRUE	TP FW643 SCIFCLK	38
TRUE	TP FW643 SCIFDAIN	38
TRUE	TP FW643 SCIFDOUT	38
TRUE	TP FW643 SCIFMC	38
TRUE	TP FW643 SDA	38
TRUE	TP FW643 SE	38
TRUE	TP FW643 SM	38
TRUE	TP FW643 CE	38
TRUE	TP FW643 FW620 L	38
TRUE	TP FW643 JASI EN	38
TRUE	DMI S2N N<1>	90 97
TRUE	DMI S2N P<1>	90 97
TRUE	FDI DATA N<1>	90 97
TRUE	FDI DATA P<1>	90 97
TRUE	FDI FSYNC<1..0>	90 97
TRUE	FDI LSYNC<1..0>	90 97
TRUE	FDI INT	9 97 98
TRUE	TP FW643 VAUX ENABLE	38
TRUE	TP FW643 VBUF	38
TRUE	TP FW643 TCK	38
TRUE	TP FW643 TDO	38
TRUE	TP FW643 TMS	38
TRUE	TP SMC P10	44 45
TRUE	TP P7 7	52
TRUE	TP PSOC SCL	52
TRUE	TP PSOC SDA	52
TRUE	TP SMC P24	44 45
TRUE	DC TEST BH1 BG2	12
TRUE	DC TEST BH3 BJ2	12
TRUE	TP USB HUB1 OCS1	24
TRUE	TP USB HUB1 PRTPWR1	24
TRUE	TP USB HUB2 OCS1	24
TRUE	TP USB HUB2 PRTPWR1	24
TRUE	TP DC TEST A62	12
TRUE	TP DC TEST D65	12
TRUE	TP SMC PF5	44 45

ICT Test Points

CPU NO_TESTS

NO_TEST

TP CPU RSVD<65..62>	TRUE	MAKE_BASE=TRUE	NC TP CPU RSVD<65..62>
TP CPU RSVD<58..45>	TRUE	MAKE_BASE=TRUE	NC TP CPU RSVD<58..45>
TP CPU RSVD<43..32>	TRUE	MAKE_BASE=TRUE	NC TP CPU RSVD<43..32>
TP CPU RSVD<27..26>	TRUE	MAKE_BASE=TRUE	NC TP CPU RSVD<27..26>
TP CPU RSVD<24..15>	TRUE	MAKE_BASE=TRUE	NC TP CPU RSVD<24..15>
TP CPU RSVD<2..1>	TRUE	MAKE_BASE=TRUE	NC TP CPU RSVD<2..1>
TP CPU RSVD NCTF<8..5>	TRUE	MAKE_BASE=TRUE	NC TP CPU RSVD NCTF<8..5>

NC NO_TESTS

NO_TEST

NC CRT IG BLUE	TRUE	MAKE_BASE=TRUE	NC CRT IG BLUE
NC CRT IG GREEN	TRUE	MAKE_BASE=TRUE	NC CRT IG GREEN
NC CRT IG RED	TRUE	MAKE_BASE=TRUE	NC CRT IG RED
NC CRT IG DDC CLK	TRUE	MAKE_BASE=TRUE	NC CRT IG DDC CLK
NC CRT IG DDC DATA	TRUE	MAKE_BASE=TRUE	NC CRT IG DDC DATA
NC CRT IG HSYNC	TRUE	MAKE_BASE=TRUE	NC CRT IG HSYNC
NC CRT IG VSYNC	TRUE	MAKE_BASE=TRUE	NC CRT IG VSYNC
NC LVDS IG CTRL CLK	TRUE	MAKE_BASE=TRUE	NC LVDS IG CTRL CLK
NC LVDS IG CTRL DATA	TRUE	MAKE_BASE=TRUE	NC LVDS IG CTRL DATA
NC PCH LVDS VBG	TRUE	MAKE_BASE=TRUE	NC PCH LVDS VBG
NC HDA SDIN1	TRUE	MAKE_BASE=TRUE	NC HDA SDIN1
NC HDA SDIN2	TRUE	MAKE_BASE=TRUE	NC HDA SDIN2
NC HDA SDIN3	TRUE	MAKE_BASE=TRUE	NC HDA SDIN3

NC NO_TESTS

NO_TEST

TRUE	TP AUD GPIO 2	56
TRUE	TP AUD GPIO 1	56
TRUE	TP AUD LO1 L N	56
TRUE	TP AUD LO1 L P	56
TRUE	TP BKL FAULT	88
TRUE	TP SPI DESCRIPTOR OVERRIDE L	44
TRUE	TP XDPPCH HOOK2	23
TRUE	TP XDPPCH HOOK3	23
TRUE	TP GMUX PL6B	87
TRUE	PM RSMRST L	17 72
TRUE	CPUIMVP BOOT1	67 68
TRUE	CPUIMVP BOOT2	67 68
TRUE	CPUIMVP UGATE2	67 68
TRUE	TP 1V05 S0 PCH VCCAPLLEXP	20

NC PCI PME L	TRUE	MAKE_BASE=TRUE	NC PCI PME L
NC PCI CLK33M OUT3	TRUE	MAKE_BASE=TRUE	NC PCI CLK33M OUT3
NC PCIE CLK100M PE4N	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PE4N
NC PCIE CLK100M PE4P	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PE4P
NC PCIE CLK100M PE5N	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PE5N
NC PCIE CLK100M PE5P	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PE5P
NC PCIE CLK100M PE6N	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PE6N
NC PCIE CLK100M PE6P	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PE6P
NC PCIE CLK100M PE7N	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PE7N
NC PCIE CLK100M PE7P	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PE7P
NC PSOC P1 3	TRUE	MAKE_BASE=TRUE	NC PSOC P1 3
NC SATA B D2RN	TRUE	MAKE_BASE=TRUE	NC SATA B D2RN
NC SATA B D2RP	TRUE	MAKE_BASE=TRUE	NC SATA B D2RP
NC SATA B R2D CN	TRUE	MAKE_BASE=TRUE	NC SATA B R2D CN
NC SATA B R2D CP	TRUE	MAKE_BASE=TRUE	NC SATA B R2D CP
NC SATA D D2RN	TRUE	MAKE_BASE=TRUE	NC SATA D D2RN
NC SATA D D2RP	TRUE	MAKE_BASE=TRUE	NC SATA D D2RP
NC SATA D R2D CN	TRUE	MAKE_BASE=TRUE	NC SATA D R2D CN
NC SATA D R2D CP	TRUE	MAKE_BASE=TRUE	NC SATA D R2D CP
NC SATA E D2RN	TRUE	MAKE_BASE=TRUE	NC SATA E D2RN
NC SATA E D2RP	TRUE	MAKE_BASE=TRUE	NC SATA E D2RP
NC SATA E R2D CN	TRUE	MAKE_BASE=TRUE	NC SATA E R2D CN
NC SATA E R2D CP	TRUE	MAKE_BASE=TRUE	NC SATA E R2D CP
NC SATA F D2RN	TRUE	MAKE_BASE=TRUE	NC SATA F D2RN
NC SATA F D2RP	TRUE	MAKE_BASE=TRUE	NC SATA F D2RP
NC SATA F R2D CN	TRUE	MAKE_BASE=TRUE	NC SATA F R2D CN
NC SATA F R2D CP	TRUE	MAKE_BASE=TRUE	NC SATA F R2D CP
TP SMC P41	TRUE	MAKE_BASE=TRUE	NC SMC P41

PCH ALIASES

NC LPC DREQ0 L			NC LPC DREQ0 L
NC CLINK CLK	TRUE	MAKE_BASE=TRUE	NC CLINK CLK
NC CLINK DATA	TRUE	MAKE_BASE=TRUE	NC CLINK DATA
NC CLINK RESET L	TRUE	MAKE_BASE=TRUE	NC CLINK RESET L
NC PCIE CLK100M PEBN	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PEBN
NC PCIE CLK100M PEBP	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PEBP

NC NO_TESTS

NO_TEST

NC FW643 AVREG	TRUE	MAKE_BASE=TRUE	NC FW643 AVREG
NC FW643 TDI	TRUE	MAKE_BASE=TRUE	NC FW643 TDI
NC DP IG C HPD	TRUE	MAKE_BASE=TRUE	NC DP IG C HPD
NC DP IG C CTRL CLK	TRUE	MAKE_BASE=TRUE	NC DP IG C CTRL CLK
NC DP IG C CTRL DATA	TRUE	MAKE_BASE=TRUE	NC DP IG C CTRL DATA
TP DP IG C MLP<3..0>	TRUE	MAKE_BASE=TRUE	NC DP IG C MLP<3..0>
TP DP IG C MLN<3..0>	TRUE	MAKE_BASE=TRUE	NC DP IG C MLN<3..0>
NC DP IG C AUXP	TRUE	MAKE_BASE=TRUE	NC DP IG C AUXP
NC DP IG C AUXN	TRUE	MAKE_BASE=TRUE	NC DP IG C AUXN
NC DP IG D HPD	TRUE	MAKE_BASE=TRUE	NC DP IG D HPD
NC DP IG D CTRL CLK	TRUE	MAKE_BASE=TRUE	NC DP IG D CTRL CLK
NC DP IG D CTRL DATA	TRUE	MAKE_BASE=TRUE	NC DP IG D CTRL DATA
TP DP IG D MLP<3..0>	TRUE	MAKE_BASE=TRUE	NC DP IG D MLP<3..0>
TP DP IG D MLN<3..0>	TRUE	MAKE_BASE=TRUE	NC DP IG D MLN<3..0>
NC DP IG D AUXP	TRUE	MAKE_BASE=TRUE	NC DP IG D AUXP
NC DP IG D AUXN	TRUE	MAKE_BASE=TRUE	NC DP IG D AUXN
NC SDVO TVCLKINN	TRUE	MAKE_BASE=TRUE	NC SDVO TVCLKINN
NC SDVO TVCLKINP	TRUE	MAKE_BASE=TRUE	NC SDVO TVCLKINP
NC SDVO STALLN	TRUE	MAKE_BASE=TRUE	NC SDVO STALLN
NC SDVO STALLP	TRUE	MAKE_BASE=TRUE	NC SDVO STALLP
NC SDVO INTN	TRUE	MAKE_BASE=TRUE	NC SDVO INTN
NC SDVO INTP	TRUE	MAKE_BASE=TRUE	NC SDVO INTP
NC GPU BUFRST L	TRUE	MAKE_BASE=TRUE	NC GPU BUFRST L
TP GPU GSTATE<0>	TRUE	MAKE_BASE=TRUE	NC GPU GSTATE<0>
NC GPU GSTATE<1>	TRUE	MAKE_BASE=TRUE	NC GPU GSTATE<1>
TP GPU MIOA D<9..0>	TRUE	MAKE_BASE=TRUE	NC GPU MIOA D<9..0>
NC GPU MIOA DE	TRUE	MAKE_BASE=TRUE	NC GPU MIOA DE
NC LVDS EG BKL PWM	TRUE	MAKE_BASE=TRUE	NC LVDS EG BKL PWM
TP LVDS IG B CLKN	TRUE	MAKE_BASE=TRUE	NC LVDS IG B CLKN
TP LVDS IG B CLKP	TRUE	MAKE_BASE=TRUE	NC LVDS IG B CLKP
TP LVDS IG BKL PWM	TRUE	MAKE_BASE=TRUE	NC LVDS IG BKL PWM
NC SMC BS ALRT L	TRUE	MAKE_BASE=TRUE	NC SMC BS ALRT L
MEM A BA<2..0>	TRUE		MEM B BA<2..0>
MEM A CKE<1..0>	TRUE		MEM B CKE<1..0>
MEM A CLK N<1..0>	TRUE		MEM B CLK N<1..0>
MEM A CLK P<1..0>	TRUE		MEM B CLK P<1..0>
MEM A CS L<1..0>	TRUE		MEM B CS L<1..0>
MEM A ODT<1..0>	TRUE		MEM B ODT<1..0>
MEM A SA<1..0>			MEM B SA<1..0>
MEM A DQ<63..0>	TRUE		MEM B DQ<63..0>
MEM A DQS N<7..0>	TRUE		MEM B DQS N<7..0>
MEM A DQS P<7..0>	TRUE		MEM B DQS P<7..0>
FB A0 DQ<31..0>	TRUE		FB B0 DQ<31..0>
FB A0 A<8..0>	TRUE		FB B0 A<8..0>
FB A0 ABI L	TRUE		FB B0 ABI L
FB A0 EDC<3..0>	TRUE		FB B0 EDC<3..0>
FB A0 WCLK N<1..0>	TRUE		FB B0 WCLK N<1..0>
FB A0 WCLK P<1..0>	TRUE		FB B0 WCLK P<1..0>
FB A0 DBI L<3..0>	TRUE		FB B0 DBI L<3..0>
FB A1 DQ<31..0>	TRUE		FB B1 DQ<31..0>
FB A1 A<8..0>	TRUE		FB B1 A<8..0>
FB A1 ABI L	TRUE		FB B1 ABI L
FB A1 EDC<3..0>	TRUE		FB B1 EDC<3..0>
FB A1 WCLK N<1..0>	TRUE		FB B1 WCLK N<1..0>
FB A1 WCLK P<1..0>	TRUE		FB B1 WCLK P<1..0>
FB A1 DBI L<3..0>	TRUE		FB B1 DBI L<3..0>
MEM A A<15..0>	TRUE		MEM B A<15..0>
MEM A CAS L	TRUE		MEM B CAS L
MEM A RAS L	TRUE		MEM B RAS L
MEM A WE L	TRUE		MEM B WE L

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE

Functional / ICT Test

Apple Inc.

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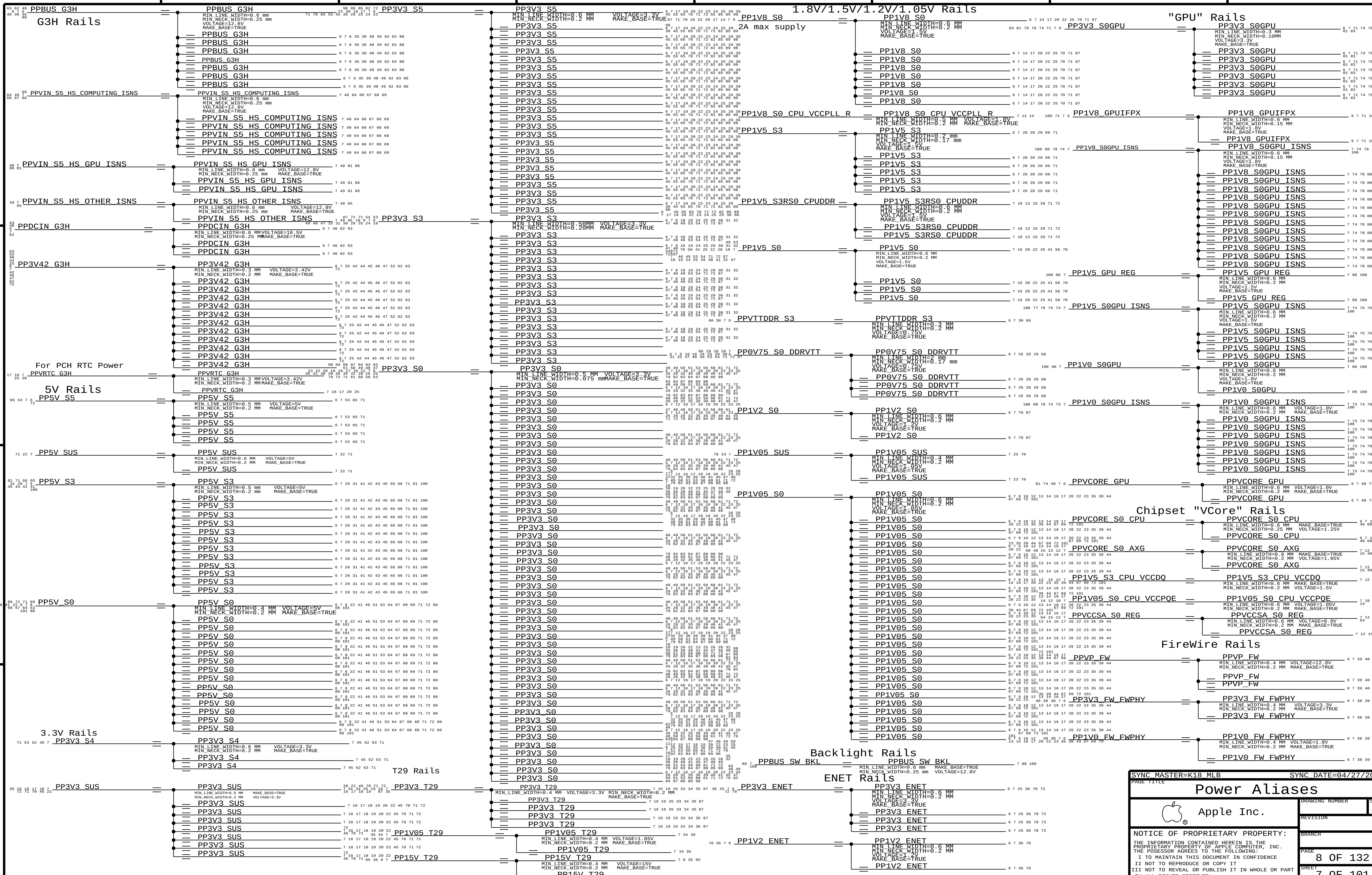

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

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Power Aliases

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Thermal Module Holes

ZT0984 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0987 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0980 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0981 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0985 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0986 STDOFF-4.5OD.98H-1.1-3.48-TH

Fan Holes

ZT0930 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0988 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0989 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0991 STDOFF-4.5OD.98H-1.1-3.48-TH

Frame Holes

ZT0915 3R2P5 — GND
ZT0940 3R2P5 — GND
ZT0950 TH — GND — SL-3.1X2.7-6CIR-NSP
ZT0960 3R2P5 — GND
ZT0990 3R2P5 — GND

Left Speaker Holes

ZT0934 STDOFF-4.0OD3.0H-TH
ZT0935 STDOFF-4.0OD3.0H-TH

Keyboard / IPD Conn Protect

ZT0952 4.0OD1.85H-M1.6X0.35
ZT0953 4.0OD1.85H-M1.6X0.35

Tall EMI pogo pins

SH0902 POGO-2.0OD-3.5H-K86-K87
SH0903 POGO-2.0OD-3.5H-K86-K87
SH0904 POGO-2.0OD-3.5H-K86-K87
SH0900 POGO-2.0OD-3.5H-K86-K87
SH0916 POGO-2.0OD-3.5H-K86-K87

Short (IO Row) EMI pogo pins

SH0910 1.4DIA-SHORT-SILVER-K99
SH0912 1.4DIA-SHORT-SILVER-K99
SH0901 1.4DIA-SHORT-SILVER-K99
SH0914 1.4DIA-SHORT-SILVER-K99
SH0911 1.4DIA-SHORT-SILVER-K99
SH0913 1.4DIA-SHORT-SILVER-K99
SH0917 1.4DIA-SHORT-SILVER-K99
GND_CHASSIS_AUDIO_JACK

Heat spreader mounting boss for T29 router

SH0920 STDOFF-4.0OD1.85H-SM
SH0923 STDOFF-4.0OD1.85H-SM

Heat spreader mounting boss for PCH

SH0921 STDOFF-4.0OD2.23H-SM
SH0922 STDOFF-4.0OD2.23H-SM

R0921 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_R2D_P0 — C0901 0.01UF 10% 10V X5R 201
R0922 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_R2D_N0 — C0902 0.01UF 10% 10V X5R 201
R0923 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_R2D_P1 — C0903 0.01UF 10% 10V X5R 201
R0924 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_R2D_N1 — C0904 0.01UF 10% 10V X5R 201

T29 / GMUX JTAG Signals

JTAG_ISP_TCK — JTAG_ISP_TCK
JTAG_ISP_TDI — JTAG_ISP_TDI
JTAG_ISP_TDO — JTAG_ISP_TDO
T29_LSEO_LSOE3 — T29_LSEO_LSOE3 (MAKE_BASE=TRUE, NO_TEST=TRUE)
T29_LSEO_LSOE2 — T29_LSEO_LSOE2 (MAKE_BASE=TRUE, NO_TEST=TRUE)

GMUX ALIASES

PM_ALL_GPU_PGOOD — PM_ALL_GPU_PGOOD
TP_LVDS_MUX_SEL_EG — TP_LVDS_MUX_SEL_EG (NO_TEST=TRUE)
EG_RESET_L — EG_RESET_L
LVDS_IG_BKL_ON — LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR — LVDS_IG_PANEL_PWR
PPVOUT_S0_LCDBKLT — PPVOUT_S0_LCDBKLT
GMUX_VSYNC — GMUX_VSYNC
PEX_CLKREQ_L — PEX_CLKREQ_L
PEG_CLKREQ_L — PEG_CLKREQ_L
PM_ENET_EN — PM_ENET_EN

FW_PLUG_DET_L — FW_PLUG_DET_L
FW643_WAKE_L — FW643_WAKE_L
TP_SMC_EXCARD_PWR_EN — TP_SMC_EXCARD_PWR_EN
NC_PCIE_EXCARD_D2R_N — NC_PCIE_EXCARD_D2R_N (TRUE)
NC_PCIE_EXCARD_D2R_P — NC_PCIE_EXCARD_D2R_P (TRUE)
NC_PCIE_EXCARD_R2D_C_N — NC_PCIE_EXCARD_R2D_C_N (TRUE)
NC_PCIE_EXCARD_R2D_C_P — NC_PCIE_EXCARD_R2D_C_P (TRUE)
NC_PCIE_CLK100M_EXCARD_N — NC_PCIE_CLK100M_EXCARD_N (TRUE)
NC_PCIE_CLK100M_EXCARD_P — NC_PCIE_CLK100M_EXCARD_P (TRUE)
NC_PEG_B_CLKRQ_L_GPIO56 — NC_PEG_B_CLKRQ_L_GPIO56 (TRUE)
NC_PCIECLKRQ4_L_GPIO26 — NC_PCIECLKRQ4_L_GPIO26 (TRUE)
TP_ISSP_SCLK_P1_1 — TP_ISSP_SCLK_P1_1
TP_ISSP_SDATA_P1_0 — TP_ISSP_SDATA_P1_0

GND
GND
GND
GND
GND

NC_PCH_CLKOUT_DPN — NC_PCH_CLKOUT_DPN (TRUE)
NC_PCH_CLKOUT_DPP — NC_PCH_CLKOUT_DPP (TRUE)
NC_PCH_GPIO64_CLKOUTFLEX0 — NC_PCH_GPIO64_CLKOUTFLEX0 (TRUE)
NC_PCH_GPIO65_CLKOUTFLEX1 — NC_PCH_GPIO65_CLKOUTFLEX1 (TRUE)
NC_PCH_GPIO66_CLKOUTFLEX2 — NC_PCH_GPIO66_CLKOUTFLEX2 (TRUE)
NC_PCH_GPIO67_CLKOUTFLEX3 — NC_PCH_GPIO67_CLKOUTFLEX3 (TRUE)

NC_FSB_CLK133M_PCHP — NC_FSB_CLK133M_PCHP (NO_TEST=TRUE)
NC_FSB_CLK133M_PCHN — NC_FSB_CLK133M_PCHN (NO_TEST=TRUE)
NC_LT_GAIN_TP — NC_LT_GAIN_TP (NO_TEST=TRUE)
NC_RT_GAIN_TP — NC_RT_GAIN_TP (NO_TEST=TRUE)
NC_SW_GAIN_TP — NC_SW_GAIN_TP (NO_TEST=TRUE)

PP5V_S0 — XW0901 — PP5V_S0_AUDIO — XW0902 — PP5V_S0_AUDIO_AMP_L — XW0903 — PP5V_S0_AUDIO_AMP_R

CPU signals

CPU_VID<0..6> — CPUIMVP_VID<0..6>
GFX_VID<0..6> — GFXIMVP_VID<0..6>
MEMVTT_EN — MEMVTT_EN

Unused PEG signals

NC_PEG_D2R_P<15..12> — =PEG_D2R_P<15..12>
NC_PEG_D2R_N<15..12> — =PEG_D2R_N<15..12>
NC_PEG_R2D_C_P<15..12> — =PEG_R2D_C_P<15..12>
NC_PEG_R2D_C_N<15..12> — =PEG_R2D_C_N<15..12>

T29 Signals Through PEG

PCIE_T29_D2R_P<3..0> — =PEG_D2R_P<11..8>
PCIE_T29_D2R_N<3..0> — =PEG_D2R_N<11..8>
PCIE_T29_R2D_C_P<3..0> — =PEG_R2D_C_P<11..8>
PCIE_T29_R2D_C_N<3..0> — =PEG_R2D_C_N<11..8>

GPU signals

PEG_D2R_P<7..0> — =PEG_D2R_P<7..0>
PEG_D2R_N<7..0> — =PEG_D2R_N<7..0>
PEG_R2D_C_P<7..0> — =PEG_R2D_C_P<7..0>
PEG_R2D_C_N<7..0> — =PEG_R2D_C_N<7..0>

Unused T29 Ports

T29_D2R_P<3..2> — NC_T29_D2RP<3..2> (NO_TEST=TRUE)
T29_D2R_N<3..2> — NC_T29_D2RN<3..2> (NO_TEST=TRUE)
T29_R2D_C_P<3..2> — NC_T29_R2D_CP<3..2> (NO_TEST=TRUE)
T29_R2D_C_N<3..2> — NC_T29_R2D_CN<3..2> (NO_TEST=TRUE)

DP_EG_AUXCH_N — DP_EG_AUXCH_N
DP_EG_AUXCH_P — DP_EG_AUXCH_P
NC_DPB_EG_AUX_CHN — NC_DPB_EG_AUX_CHN
NC_DPB_EG_AUX_CHP — NC_DPB_EG_AUX_CHP
NC_DPB_EG_DDC_CLK — NC_DPB_EG_DDC_CLK
NC_DPB_EG_DDC_DATA — NC_DPB_EG_DDC_DATA
NC_DPB_EG_MLN<3..0> — DPB_EG_ML_N<3..0>
NC_DPB_EG_MLP<3..0> — DPB_EG_ML_P<3..0>

LCD_BKLT_EN
R0901 4.7K 5% 1/16W MF-LF 402

T29BST:N
R0950 0 5% 1/8W MF-LF 805 — PPBUS_G3H — PP15V_T29

TP_CPU_VTT_SELECT — TP_CPU_VTT_SELECT

TP_LVDS_IG_B_CLKP — TP_LVDS_IG_B_CLKP
TP_LVDS_IG_B_CLKN — TP_LVDS_IG_B_CLKN
TP_LVDS_IG_BKL_PWM — TP_LVDS_IG_BKL_PWM
NC_GPU_XTALOUT — NC_GPU_XTALOUT (NO_TEST=TRUE)
NC_LVDS_IG_A_DATAP<3> — NC_LVDS_IG_A_DATAP<3> (NO_TEST=TRUE)
NC_LVDS_IG_A_DATAN<3> — NC_LVDS_IG_A_DATAN<3> (NO_TEST=TRUE)
NC_LVDS_IG_B_DATAP<3> — NC_LVDS_IG_B_DATAP<3> (NO_TEST=TRUE)
NC_LVDS_IG_B_DATAN<3> — NC_LVDS_IG_B_DATAN<3> (NO_TEST=TRUE)

NC_USB_HUB1_OCS4 — NC_USB_HUB1_OCS4
NC_USB_HUB2_OCS4 — NC_USB_HUB2_OCS4

PP3V3_S3
NOSTUFF R0903 10K 5% 1/16W MF-LF 402 — USB_EXTC_N
NOSTUFF R0904 10K 5% 1/16W MF-LF 402 — USB_EXTC_P

PP3V3_S3
NOSTUFF R0913 10K 5% 1/16W MF-LF 402 — USB_SDCARD_P
NOSTUFF R0914 10K 5% 1/16W MF-LF 402 — USB_SDCARD_N

PP3V3_S3
R0915 10K 5% 1/16W MF-LF 402 — USB_T29A_N
R0916 10K 5% 1/16W MF-LF 402 — USB_T29A_P

R0926 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_D2R_P1 — C0906 0.01UF 10% 10V X5R 201
R0927 51 5% 1/20W MF 201 — T29_A_BIAS_R — T29_A_BIAS_D2R_N1 — C0907 0.01UF 10% 10V X5R 201

DP_A_BIAS2 — C0905 0.01UF 10% 10V X5R 201
DP_A_BIAS0 — C0908 0.01UF 10% 10V X5R 201

NC_DP_IG_MLP<3..0> — TP_DP_IG_B_MLP<3..0>
NC_DP_IG_MLN<3..0> — TP_DP_IG_B_MLN<3..0>
DP_IG_AUX_CH_P — DP_IG_AUX_CH_P
DP_IG_AUX_CH_N — DP_IG_AUX_CH_N
DP_IG_DDC_CLK — DP_IG_DDC_CLK
DP_IG_DDC_DATA — DP_IG_DDC_DATA
DP_IG_HPD — DP_IG_HPD

GND — MIN_LINE_WIDTH=0.6 mm — MIN_NECK_WIDTH=0.095 mm — VOLTAGE=0V

Digital Ground

SYNC_MASTER=K18_MLB
SYNC_DATE=04/27/2010
PAGE TITLE: Signal Aliases
Apple Inc.
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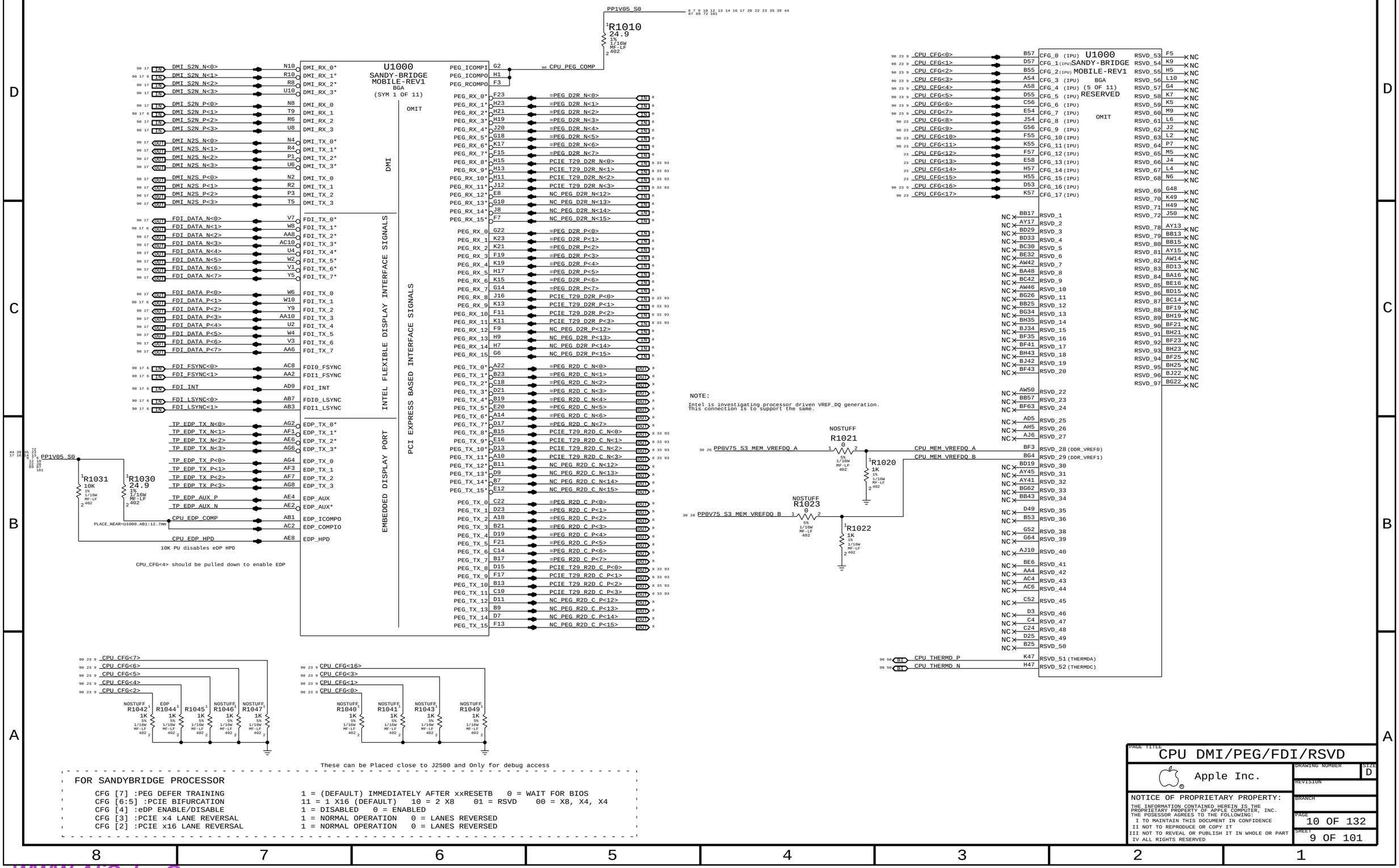

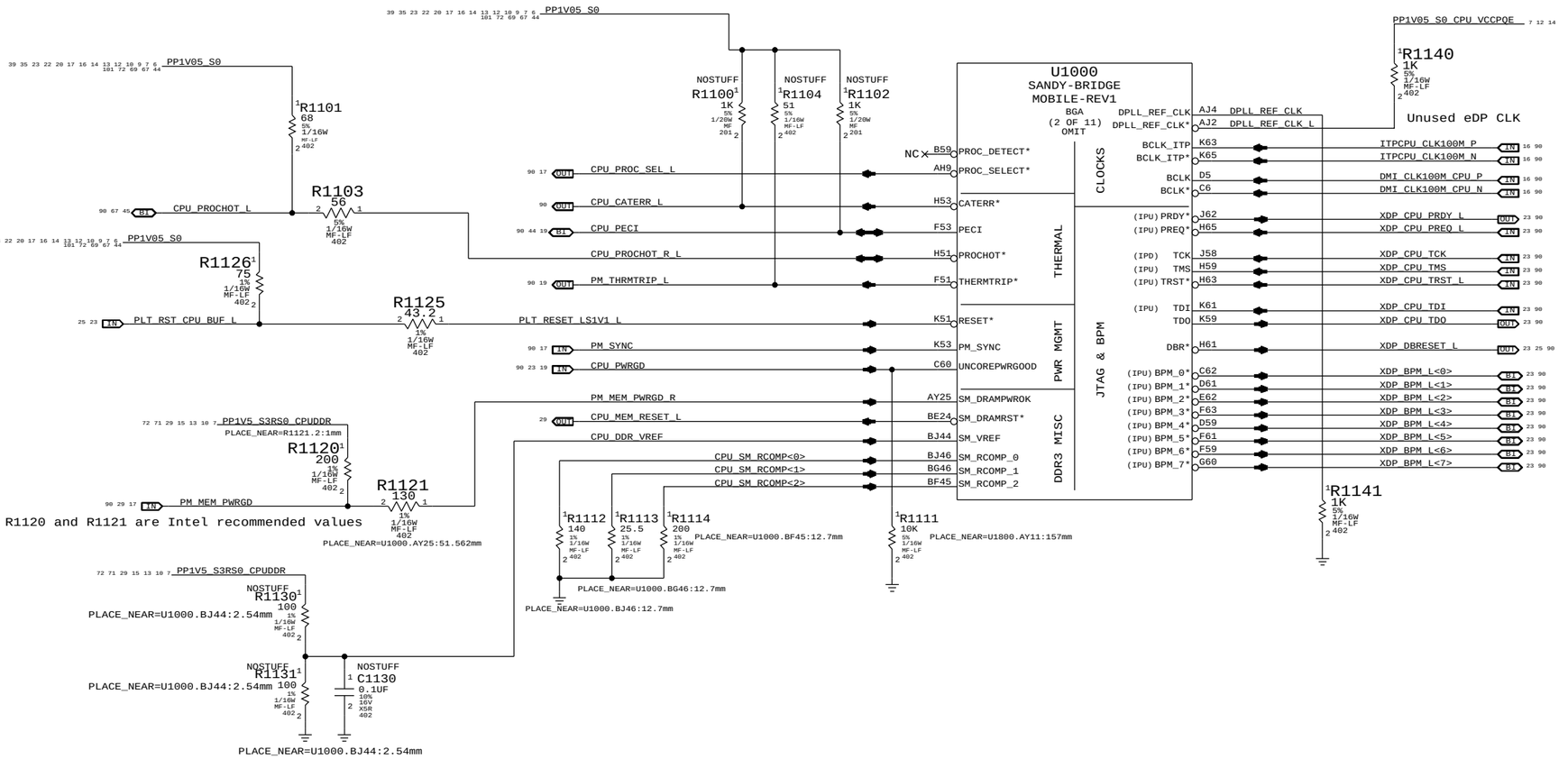

PAGE TITLE
CPU CLOCK/MISC/JTAG

Apple Inc.

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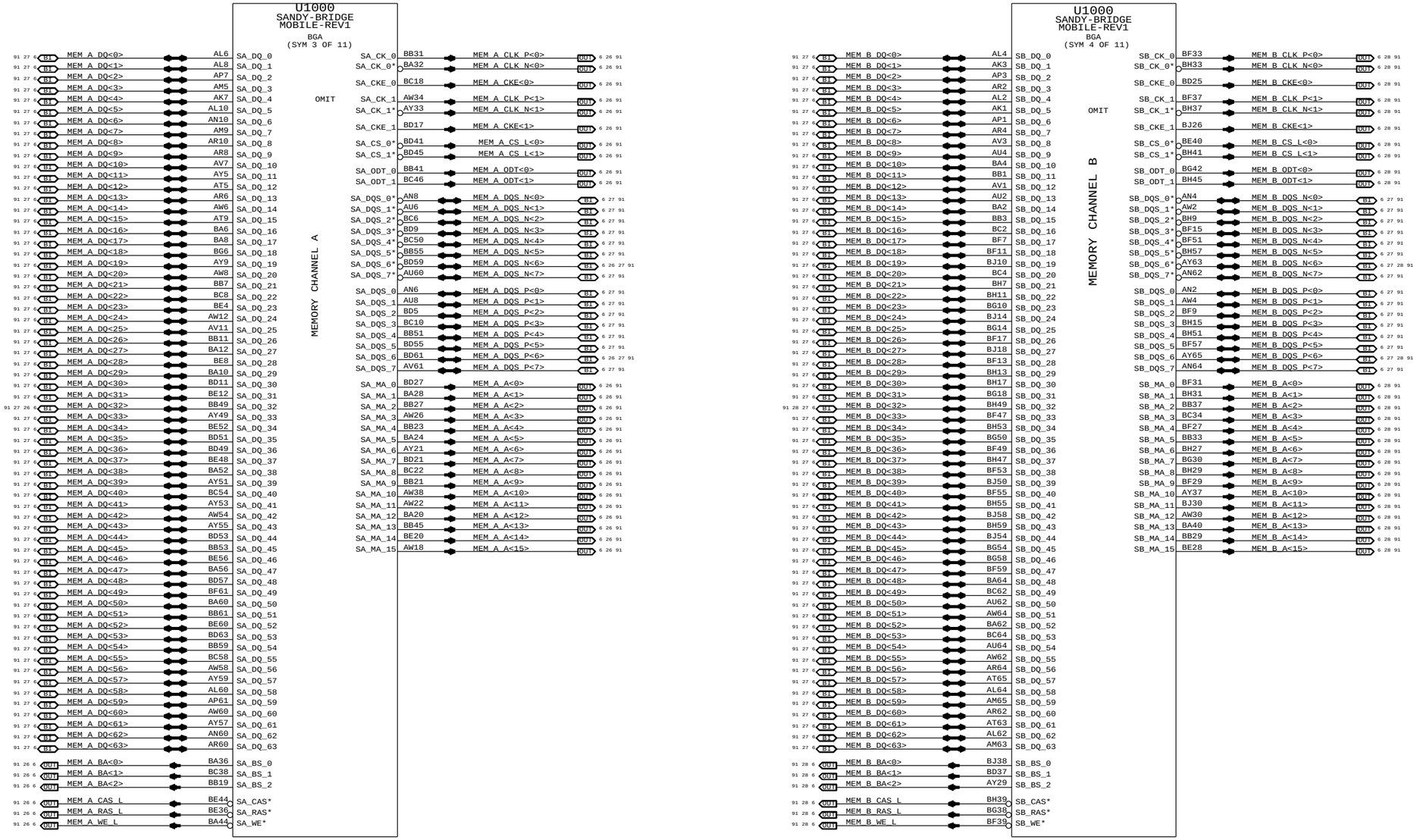

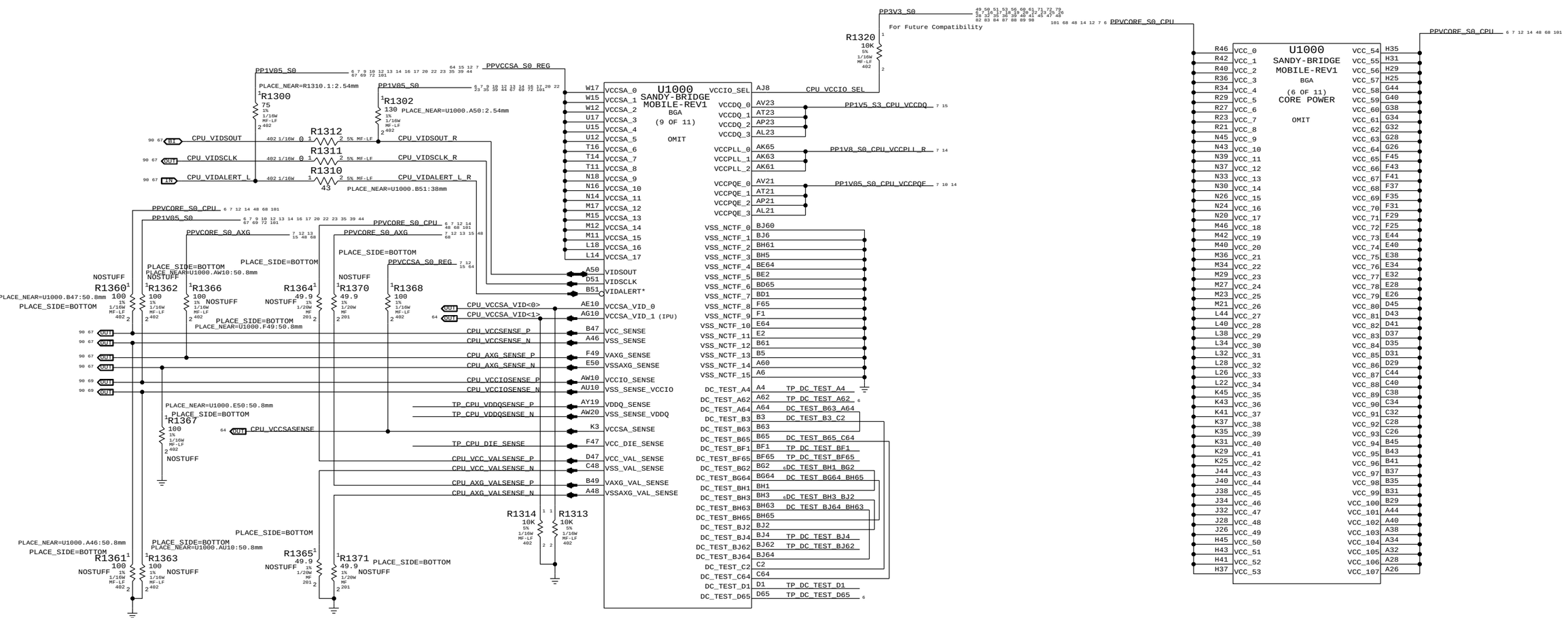

PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.
NOTE: Intel validation sense lines per doc 439028 rev1.0
HR_PPDG sections 6.2.1 and 6.3.1.

SYNC_MASTER=K92_MLB SYNC_DATE=08/03/2010

PAGE TITLE: CPU POWER

Apple Inc.

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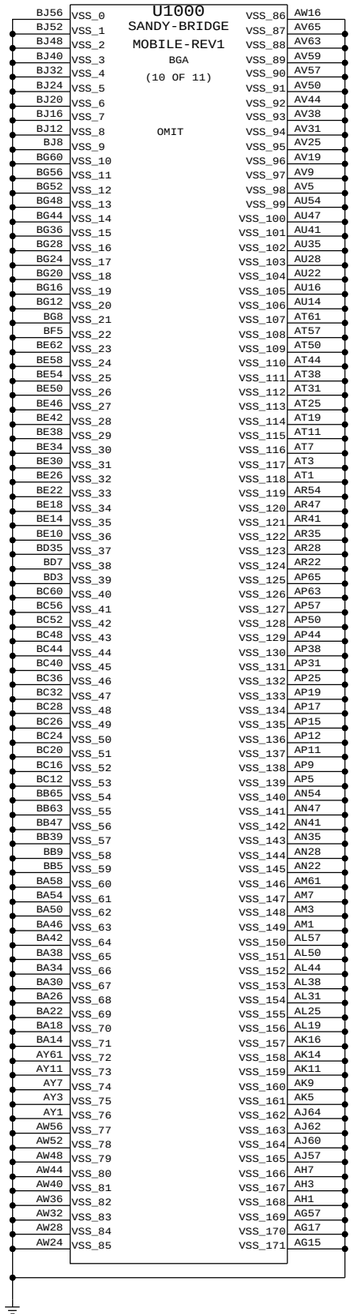
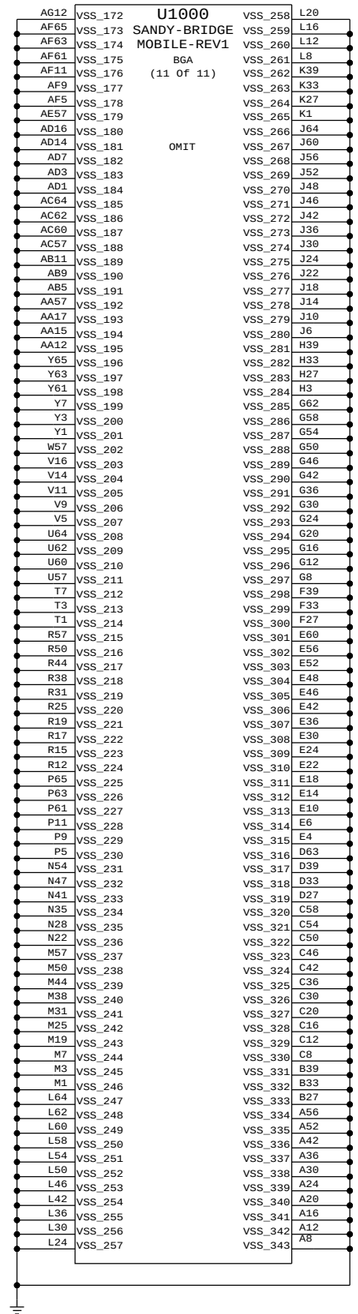
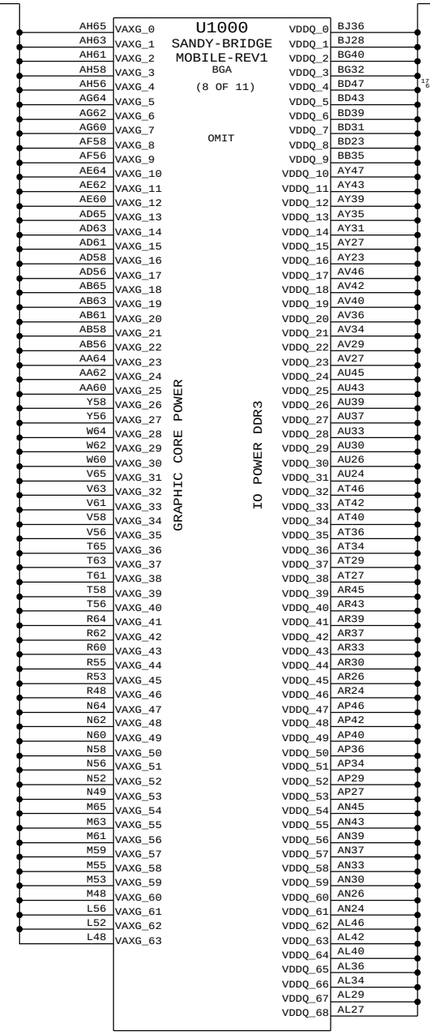


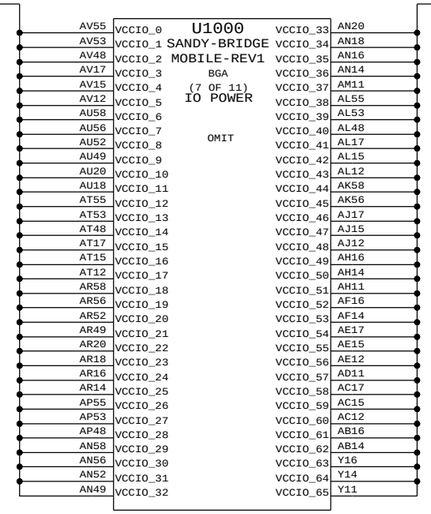


PPVCORE_S0_AXG
68 48 15 12 7



PP1V5_S3RS0_CPUDDR
7 10 15 29 71 72

PP1V05_S0
17 16 14 13 12 11 9 7 6
69 67 44 39 35 23 22 20



PP1V05_S0
67 69 72 103
17 20 22 23 33 38 39 44

PP1V05_S0
68 70 71 102
16 18 19 21 24 32 34 37

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Apple Inc.

CPU VCORE DECOUPLING

Intel recommendation: 4x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 28x 1uF 0402 (NOSTUFF)
Apple Implementation: 4x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 16x 22uF 0603, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0603 (NOSTUFF)

101 68 48 12 7 6 PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C16C7):
Place on bottom side of U1000

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1613 C1614 C1615 C1616 C1617 C1618 C1619
1UF 20% 10V X5R 402

NOSTUFF C16A0 C16A1 C16A2 C16A3 C16A4 C16A5 C16A6 C16A7 C16A8 C16A9 C16B0 C16B1 C16B2 C16B3 C16B4 C16B5 C16B6 C16B7 C16B8 C16B9
1UF 20% 6.3V X5R 0201

NOSTUFF C16C0 C16C1 C16C2 C16C3 C16C4 C16C5 C16C6 C16C7
1UF 20% 6.3V X5R 0201

PLACEMENT_NOTE (C1620-C1623):
Place near U1000 on bottom side

CRITICAL C1620 C1621 C1622 C1623
10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1624-C16D5):
Place near inductors on bottom side.

CRITICAL C1624 C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639
22UF 20% 6.3V X5M CERM1 0603

NOSTUFF C16D0 C16D1 C16D2 C16D3 C16D4 C16D5
22UF 20% 6.3V X5M CERM1 0603

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

CRITICAL C1640 C1641 C1642 C1643
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

NOSTUFF C1644
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

PLACEMENT_NOTE (C1646-C1671):
Place on bottom side of U1000

39 35 23 18 1 PP1V05_S0
26 17 16 11 72 69 67 44

C1646 C1647 C1648 C1649 C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657 C1658
C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671
1UF 20% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

CRITICAL C1672 C1673 C1674 C1675 C1676 C1677 C1678 C1679 C1680 C1681
10UF 20% 6.3V X5R 603

Place near inductors on bottom side

CRITICAL C1682 C1683
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

CRITICAL

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601
0.010
1% 1/4W MF 0603

PP1V05_S0_CPU_VCCPQE 7 10 12

C1684
1UF 10% 16V X5R 402

CPU VCCPLL DECOUPLING

87 71 70 25 22 20 17 7 6 PP1V8_S0

R1600
0
5% 1/16W MF-LF 402

PP1V8_S0_CPU_VCCPLL_R 7 12

PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA

C1685
1UF 10% 16V X5R 402

C1686
1UF 10% 16V X5R 402

CRITICAL C1687
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

PLACE_NEAR=U1000.AK61:5 mm

CPU VCCPLL Low pass filter

SYNC_MASTER=K92_MLB SYNC_DATE=08/19/2010

PAGE TITLE
CPU DECOUPLING-I

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VAXG DECOUPLING

Intel recommendation: 2x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 6x 22uF 0805, 2x 22uF 0805 (NOSTUFF), 6x 10uF 0603, 2x 10uF 0603 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)
Apple Implementation: 2x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 6x 22uF 0603, 2x 22uF 0603 (NOSTUFF), 6x 10uF 0402, 2x 10uF 0402 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)

68 48 13 12 7 PPVCORE_S0_AXG

PLACEMENT_NOTE (C1700-C1708):
Place on bottom side of U1000

C1700 1UF 10% 10V X5R 402
C1701 1UF 10% 10V X5R 402
C1702 1UF 10% 10V X5R 402
C1703 1UF 10% 10V X5R 402
C1704 1UF 10% 10V X5R 402
C1705 1UF 10% 10V X5R 402
C1706 1UF 10% 10V X5R 402
C1707 1UF 10% 10V X5R 402
C1708 1UF 10% 10V X5R 402
NOSTUFF C1709 1UF 10% 10V X5R 402
NOSTUFF C1710 1UF 10% 10V X5R 402
NOSTUFF C1711 1UF 10% 10V X5R 402
NOSTUFF C1712 1UF 10% 10V X5R 402
NOSTUFF C1713 1UF 10% 10V X5R 402
NOSTUFF C1714 1UF 10% 10V X5R 402
NOSTUFF C1715 1UF 10% 10V X5R 402
NOSTUFF C1716 1UF 10% 10V X5R 402
NOSTUFF C1717 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1718-C1723):
Place close to U1000 on bottom side

C1718 10UF 20% 6.3V CERM-X5R 0402-1
C1719 10UF 20% 6.3V CERM-X5R 0402-1
C1720 10UF 20% 6.3V CERM-X5R 0402-1
C1721 10UF 20% 6.3V CERM-X5R 0402-1
C1722 10UF 20% 6.3V CERM-X5R 0402-1
C1723 10UF 20% 6.3V CERM-X5R 0402-1
NOSTUFF C1724 10UF 20% 6.3V CERM-X5R 0402-1
NOSTUFF C1725 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1726-C1731):
Place near inductors on bottom side.

C1726 22UF 20% 6.3V X5R-CERM1 0603
C1727 22UF 20% 6.3V X5R-CERM1 0603
C1728 22UF 20% 6.3V X5R-CERM1 0603
C1729 22UF 20% 6.3V X5R-CERM1 0603
C1730 22UF 20% 6.3V X5R-CERM1 0603
C1731 22UF 20% 6.3V X5R-CERM1 0603
NOSTUFF C1732 22UF 20% 6.3V X5R-CERM1 0603
NOSTUFF C1733 22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1734-C1735):
Place near inductors on bottom side.

C1734 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
C1735 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
NOSTUFF C1737 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

PLACEMENT_NOTE (C1738-C1747):

72 71 29 13 10 7 PP1V5_S3RS0_CPUDDR

Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V X5R 603
C1749 10UF 20% 6.3V X5R 603
C1750 10UF 20% 6.3V X5R 603
C1751 10UF 20% 6.3V X5R 603
C1752 10UF 20% 6.3V X5R 603
C1753 10UF 20% 6.3V X5R 603
C1754 10UF 20% 6.3V X5R 603
C1755 10UF 20% 6.3V X5R 603

Place near inductors on bottom side

C1756 330UF-0.0060HM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1700 0.010 1% 1/4W MF 0603

PP1V5_S3_CPU_VCCDQ 7 12

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402

PLACEMENT_NOTE (C1758-C1762):

64 12 7 PPVCCSA_S0_REG

Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V X5R 603
C1764 10UF 20% 6.3V X5R 603
C1765 10UF 20% 6.3V X5R 603
C1766 10UF 20% 6.3V X5R 603
C1767 10UF 20% 6.3V X5R 603

C1768 270UF 20% 2V TANT CASE-B4-SM

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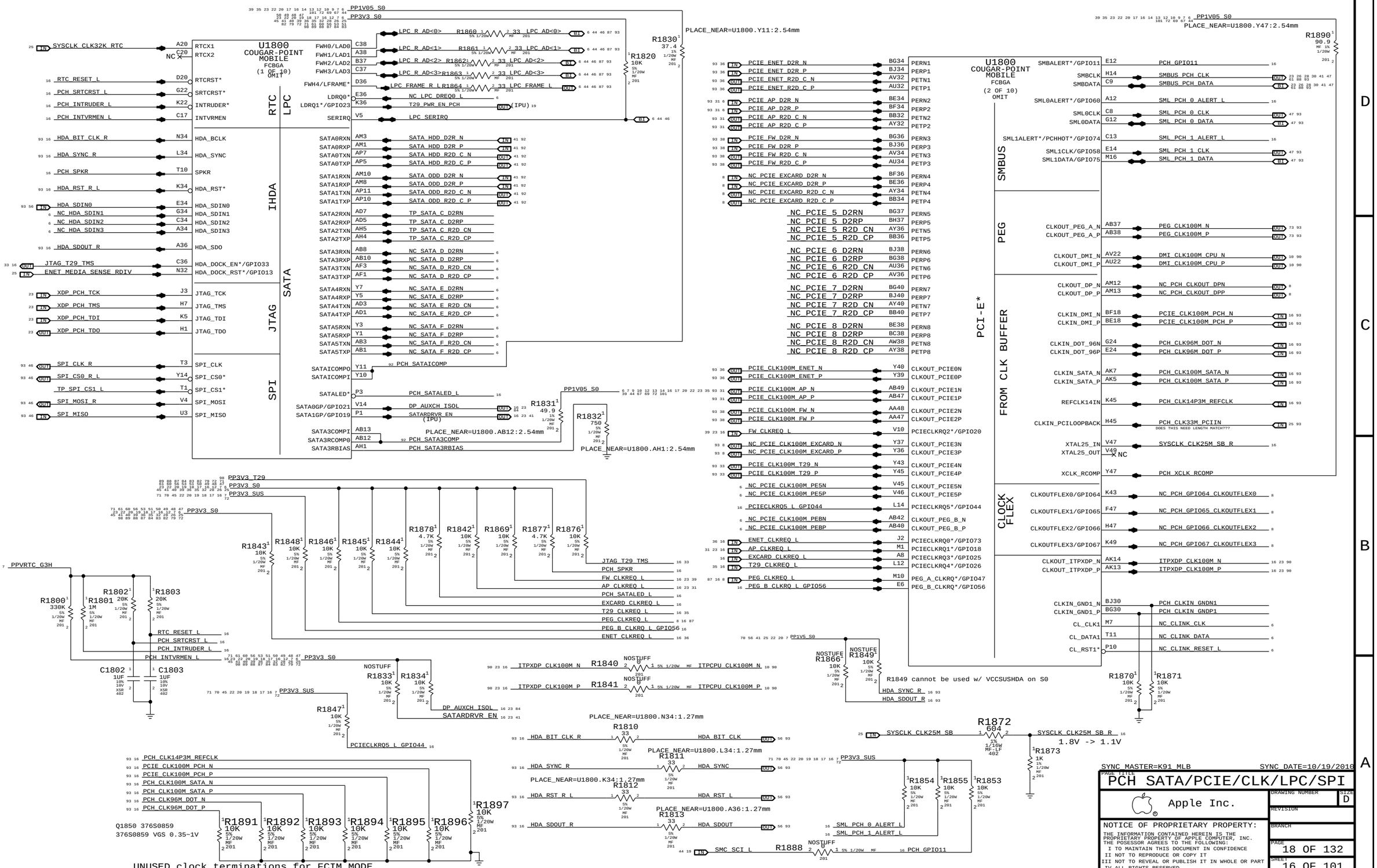

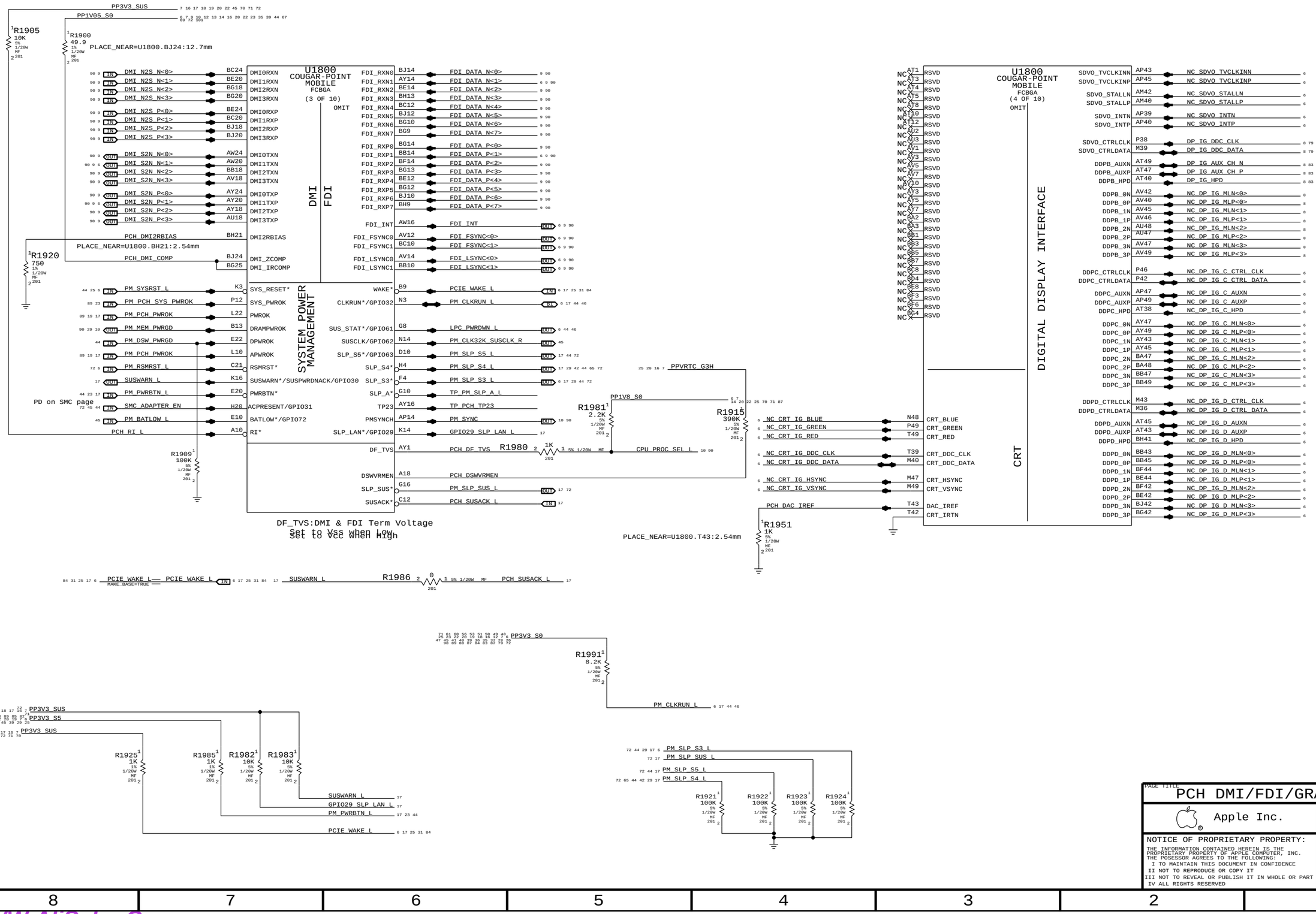

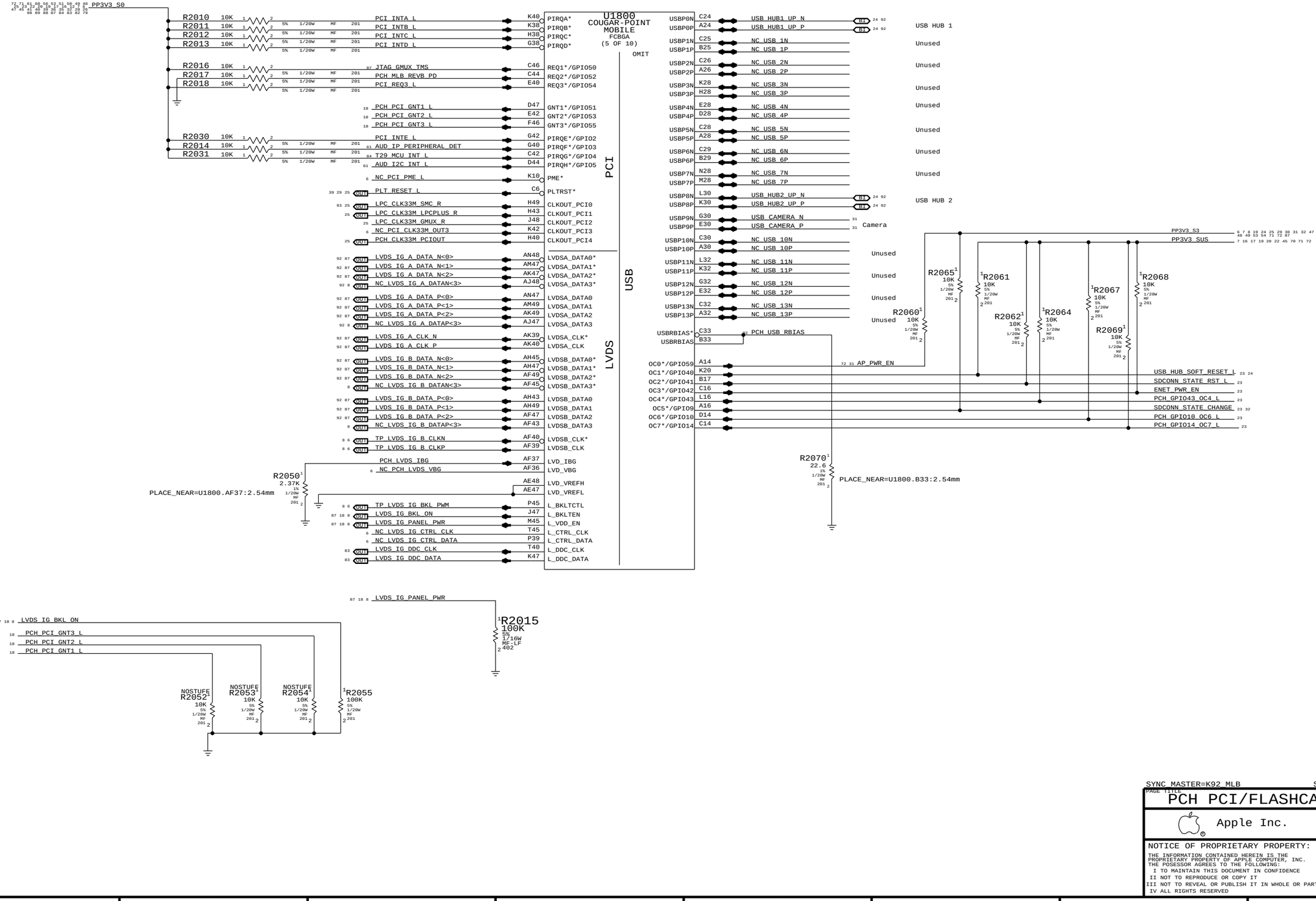

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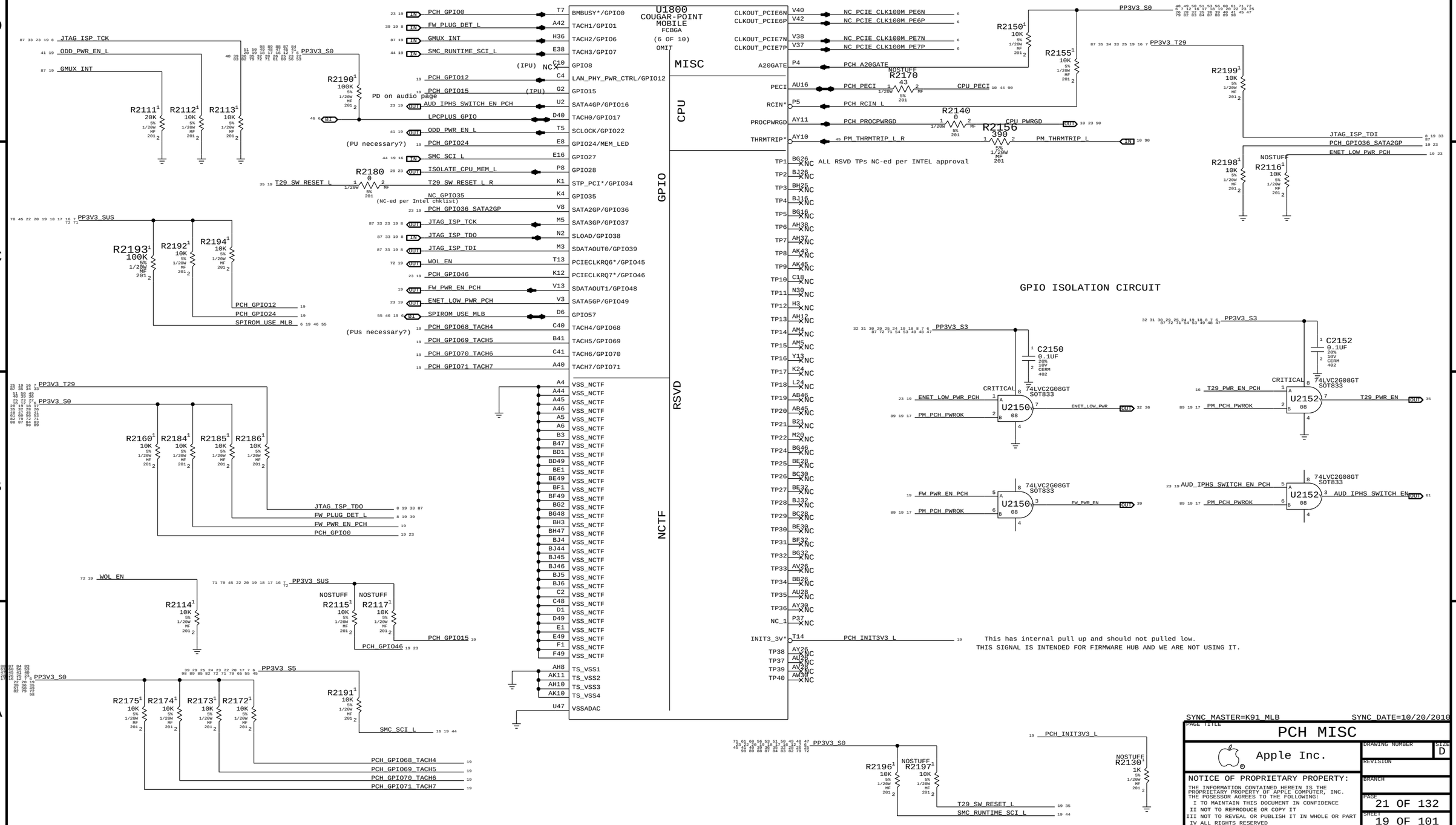

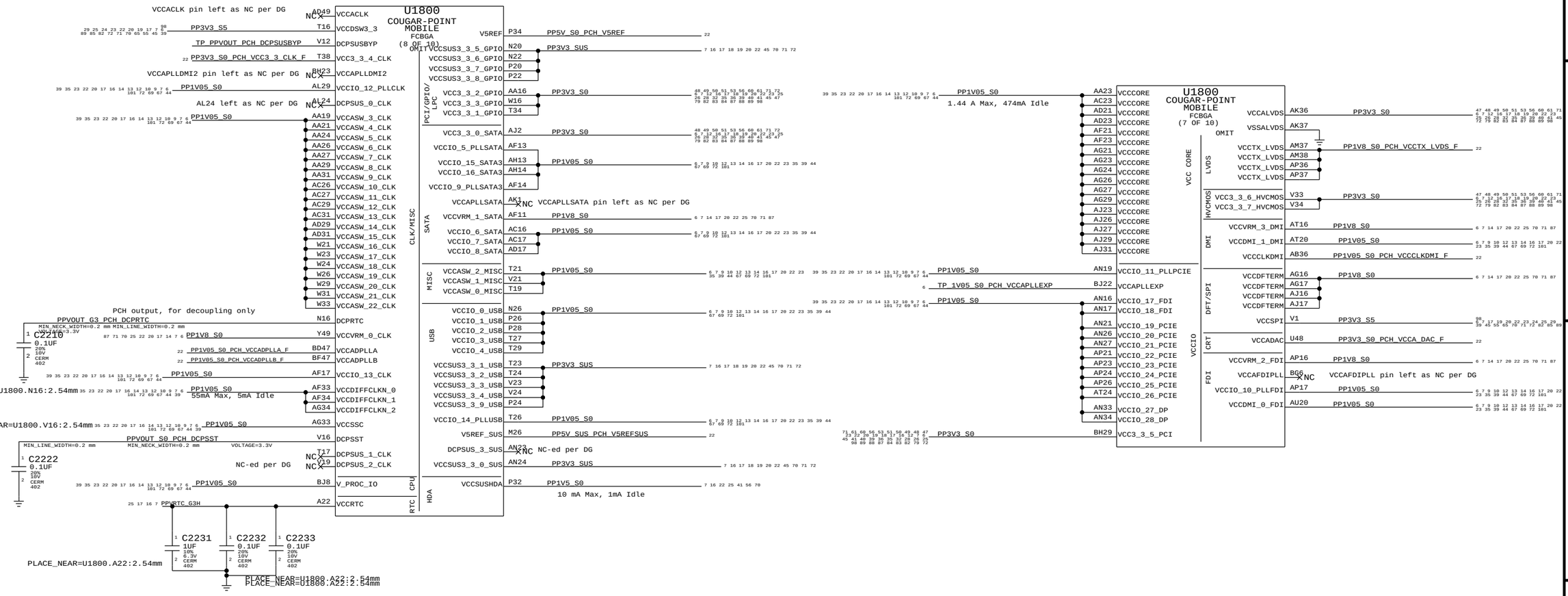

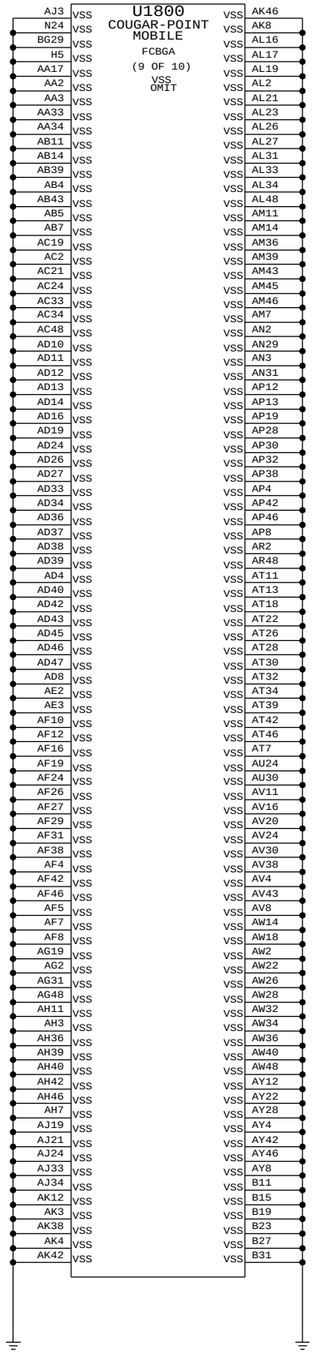

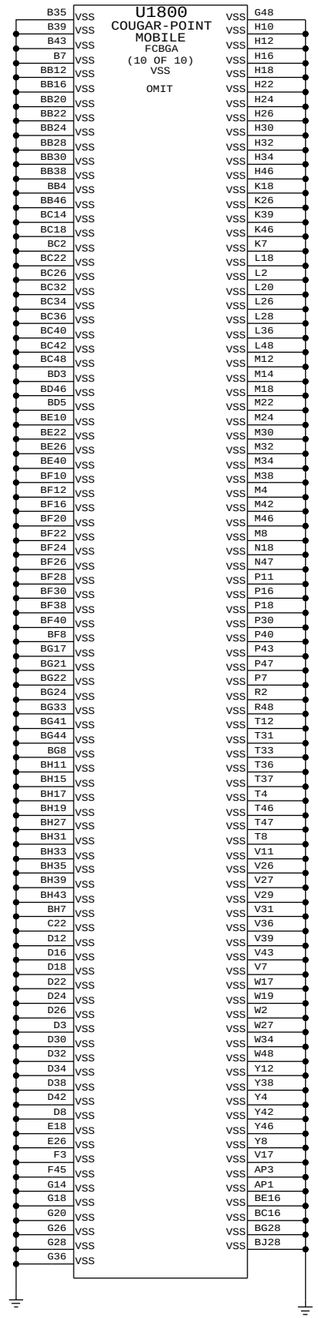

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CRITICAL
L2406
10UH-0.45A
1210-HF
PP1V05_S0
PP1V05_S0_PCH_VCCCLKDMI_R
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
R2415
1
5%
1/16W
MF-LF
402
PP1V05_S0_PCH_VCCCLKDMI_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
C2411
1UF
10%
16V
X5R
402
PLACE_NEAR=U1800.AB36:2.54mm

PCH VCCSUS3_3 BYPASS
(PCH SUSPEND USB 3.3V PWR)
PP3V3_SUS
C2484
0.1UF
10%
16V
XSR
402
C2413
0.1UF
10%
16V
XSR
402
PLACE_NEAR=U1800.P24:2.54mm
PLACE_NEAR=U1800.V24:2.54mm

PP1V8_S0
C2440
0.1UF
20%
10V
CERM
402
PLACE_NEAR=U1800.AJ16:2.54mm

PCH VCCIO BYPASS
(PCH USB 1.05V PWR)
PP1V05_S0
C2444
1UF
10%
6.3V
CERM
402
C2452
1UF
10%
6.3V
CERM
402
PLACE_NEAR=U1800.AH13:2.54mm
PLACE_NEAR=U1800.AC17:2.54mm
C2446
1UF
10%
6.3V
CERM
402
PLACE_NEAR=U1800.P28:2.54mm

CRITICAL
L2407
0.1UH
0805
PP1V8_S0
PP1V8_S0_PCH_VCCTX_LVDS_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.8V
CRITICAL
C2400
22UF
20%
6.3V
CERM
805
C2406
0.01UF
10%
16V
CERM
402
C2408
0.01UF
10%
16V
CERM
402
PLACE_NEAR=U1800.AM37:2.54mm
PLACE_NEAR=U1800.AM37:2.54mm
PLACE_NEAR=U1800.AM37:2.54mm

PCH VCCSUSHDA BYPASS
PP1V5_S0
C2441
0.1UF
20%
10V
CERM
402
PLACE_NEAR=U1800.P32:2.54mm
PP1V05_S0
C2475
1UF
10%
6.3V
CERM
402
PLACE_NEAR=U1800.AG33:2.54mm
PP3V3_SUS
C2476
1UF
10%
6.3V
CERM
402
PLACE_NEAR=U1800.P22:2.54mm

PP1V05_S0
C2416
4.7UF
20%
6.3V
XSR
402
C2417
0.1UF
10%
16V
XSR
402
C2430
0.1UF
10%
16V
XSR
402
PLACE_NEAR=U1800.BJ8:2.54mm
PLACE_NEAR=U1800.BJ8:2.54mm
PLACE_NEAR=U1800.BJ8:2.54mm

PP3V3_S5
C2442
1UF
10%
6.3V
CERM
402
PLACE_NEAR=U1800.V1:2.54mm

R2450
0
5%
1/20W
MF
201
PP3V3_S0
PP3V3_S0_PCH_VCCA_DAC_F
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
CRITICAL
C2450
10UF
20%
6.3V
CERM
805
C2451
0.1UF
10%
16V
XSR
402
C2455
0.01UF
10%
16V
CERM
402
PLACE_NEAR=U1800.U48:2.54mm
PLACE_NEAR=U1800.U48:2.54mm
PLACE_NEAR=U1800.U48:2.54mm

PCH VCCIO BYPASS
PP1V05_S0
C2419
1UF
10%
6.3V
CERM
402
PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)
PLACE_NEAR=U1800.AT20:2.54mm

PP3V3_S5
C2499
0.1UF
20%
10V
CERM
402
PLACE_NEAR=U1800.T16:2.54mm

PP1V05_S0
C2434
1UF
10%
6.3V
CERM
402
PLACE_NEAR=U1800.AF34:2.54mm
PP1V05_S0
C2469
1UF
10%
6.3V
CERM
402
PLACE_NEAR=U1800.AF17:2.54mm

PCH VCCCORE BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C2481
1UF
10%
6.3V
CERM
402
C2482
1UF
10%
6.3V
CERM
402
C2483
1UF
10%
6.3V
CERM
402
C2460
10UF
20%
6.3V
CERM
805
PLACE_NEAR=U1800.AD21:2.54mm
PLACE_NEAR=U1800.AG24:2.54mm
PLACE_NEAR=U1800.AG25:2.54mm
PLACE_NEAR=U1800.AG26:2.54mm

PP3V3_S0
PP5V_S0
1 mA
R2405
100
5%
1/16W
MF-LF
402
NC
D2400
BAT54DW-X-G
SOT-363
PCH V5REF Filter & Follower
(PCH Reference for 5V Tolerance on PCI)
NEED PWR CONSTRAINT
PP5V_S0_PCH_V5REF
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
<1 MA
PP5V_S0_PCH_V5REF
C2439
1UF
10%
16V
X5R
402
PLACE_NEAR=U1800.P34:2.54mm

PP3V3_S0
R2451
0
5%
1/16W
MF-LF
402
PP3V3_S0_PCH_VCC3_3_CLK_R
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=3.3V
CRITICAL
L2451
10UH-0.12A-0.36OHM
0603
PP3V3_S0_PCH_VCC3_3_CLK_F
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=3.3V
CRITICAL
C2453
10UF
20%
6.3V
X5R
603
C2454
1UF
10%
10V
X5R
402
PLACE_NEAR=U1800.T38:2.54mm
PLACE_NEAR=U1800.T38:2.54mm

PP1V05_S0
C2426
1UF
10%
6.3V
CERM
402
C2456
1UF
10%
6.3V
CERM
402
C2496
1UF
10%
6.3V
CERM
402
C2428
22UF
20%
6.3V
CERM
805
C2420
22UF
20%
6.3V
CERM
805
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm

PP3V3_SUS
PP5V_SUS
1 mA S0-S5
R2404
10
5%
1/16W
MF-LF
402
NC
D2400
BAT54DW-X-G
SOT-363
PCH V5REF_SUS Filter & Follower
(PCH Reference for 5V Tolerance on USB)
NEED PWR CONSTRAINT
PP5V_SUS_PCH_V5REFSUS
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
MAKE_BASE=TRUE
<1 MA S0-S5
PP5V_SUS_PCH_V5REFSUS
C2438
0.1UF
10%
16V
CERM
402
PLACE_NEAR=U1800.M26:2.54mm

PP1V05_S0
R2490
0
5%
1/16W
MF-LF
402
PP1V05_S0_PCH_VCCADPLLA_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V
CRITICAL
L2490
10UH-0.12A-0.36OHM
0603
PCH VCCADPLLA Filter
(PCH DPLLA PWR)
PP1V05_S0_PCH_VCCADPLLA_F
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
NO STUFF
68 mA
CRITICAL
C2491
220UF
20%
2.5V
POLY-TANT
CASE-B2-SM1
C2492
1UF
10%
6.3V
CERM
402
PLACE_NEAR=U1800.BD47:2.54MM
PLACE_NEAR=U1800.BD47:2.54MM

PP1V05_S0
R2491
0
5%
1/16W
MF-LF
402
PP1V05_S0_PCH_VCCADPLLB_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V
CRITICAL
L2491
10UH-0.12A-0.36OHM
0603
PCH VCCADPLLB Filter
(PCH DPLLB PWR)
PP1V05_S0_PCH_VCCADPLLB_F
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
NO STUFF
69 mA
CRITICAL
C2493
220UF
20%
2.5V
POLY-TANT
CASE-B2-SM1
C2494
1UF
10%
6.3V
CERM
402
PLACE_NEAR=U1800.BF47:2.54MM
PLACE_NEAR=U1800.BF47:2.54MM

PP1V05_S0
C2429
1UF
10%
6.3V
CERM
402
C2414
1UF
10%
6.3V
CERM
402
C2407
1UF
10%
6.3V
CERM
402
C2463
1UF
10%
6.3V
CERM
402
C2401
10UF
20%
10V
X5R-CERM
0805
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm

PP3V3_S0
C2421
0.1UF
10%
16V
XSR
402
PLACE_NEAR=U1800.BH29:2.54mm

PP3V3_S0
C2423
0.1UF
10%
16V
XSR
402
PLACE_NEAR=U1800.AJ2:2.54mm

PP3V3_S0
C2424
0.1UF
10%
16V
XSR
402
PLACE_NEAR=U1800.V33:2.54mm

PP3V3_S0
C2486
0.1UF
10%
25V
XSR
402
C2485
0.1UF
10%
25V
XSR
402
PLACE_NEAR=U1800.T34:2.54mm
PLACE_NEAR=U1800.AA16:2.54mm

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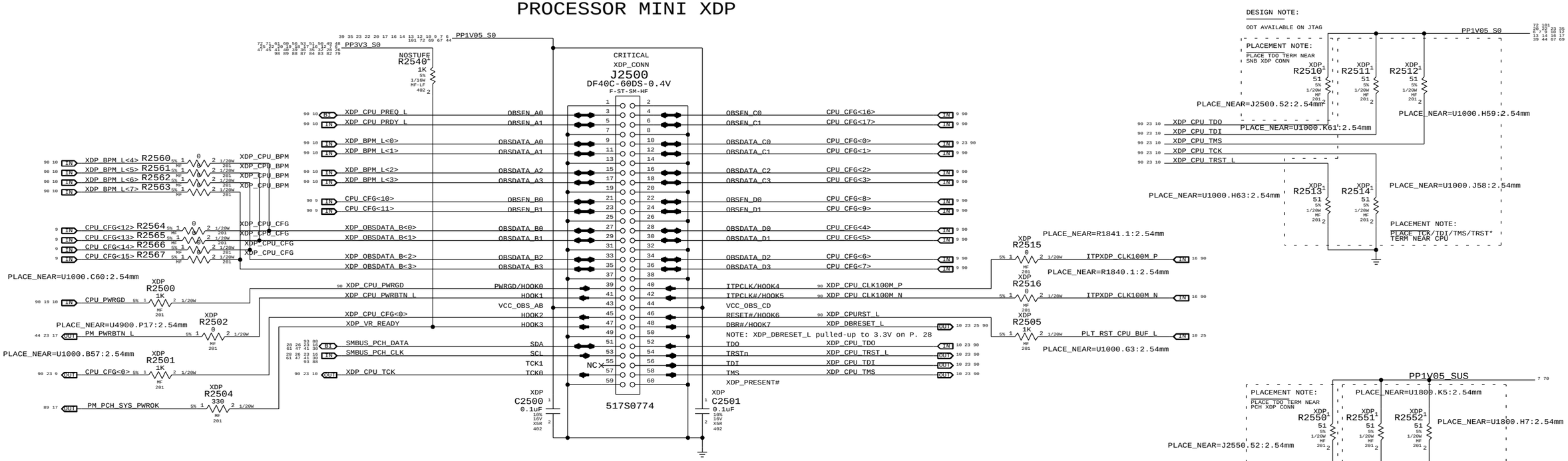
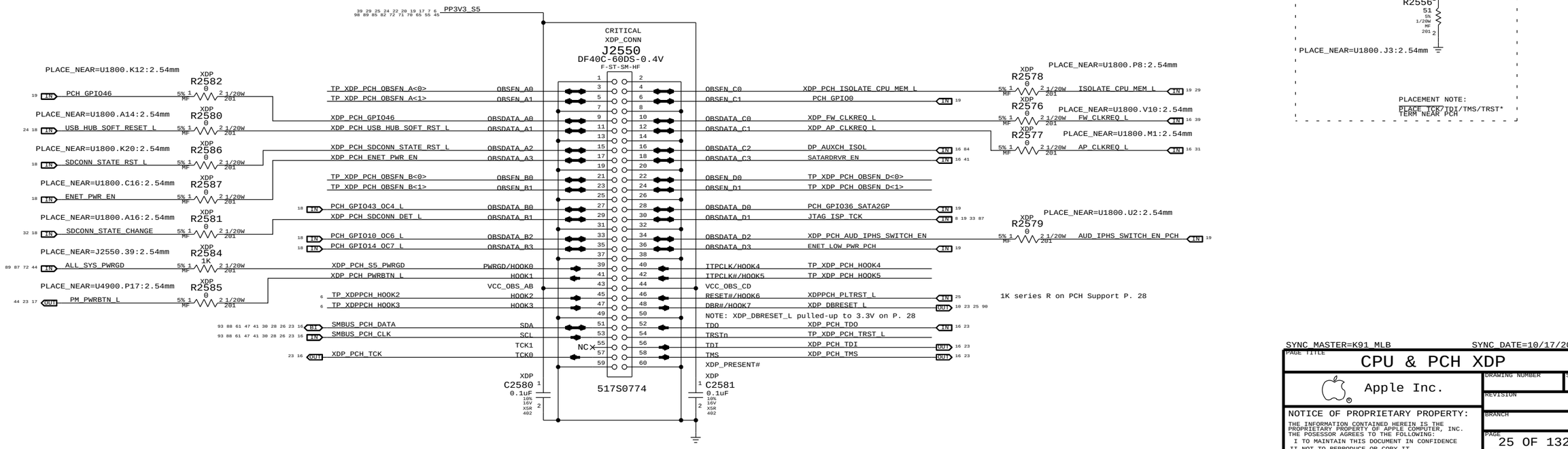
PROCESSOR MINI XDP



PCH MINI XDP



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BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U2600,U2650	CRITICAL	USBHUB_2061
338S0923	2	SMSC USX2513B	U2600,U2650	CRITICAL	USBHUB_2513B

T29 - no longer used, pulled up to 3V3 S0

IR Receiver

External B

External C

Bluetooth

Trackpad/Keyboard

External A

SD Card/Express Card

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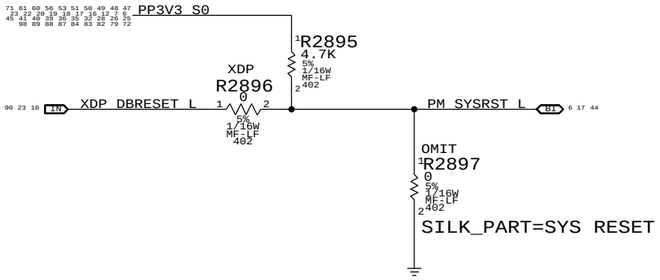
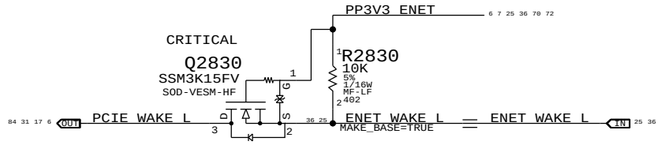
PCH Reset Button

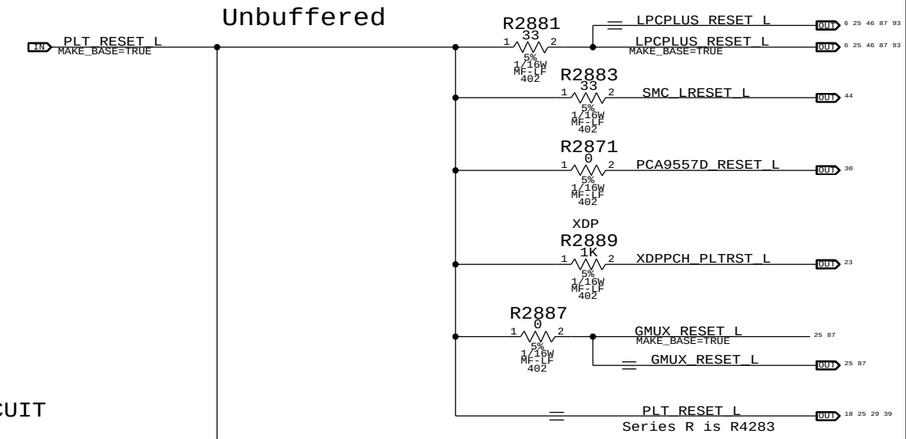


Ethernet WAKE# Isolation



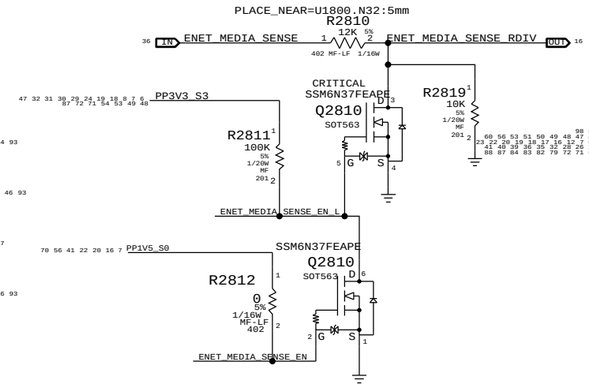
Platform Reset Connections

Unbuffered



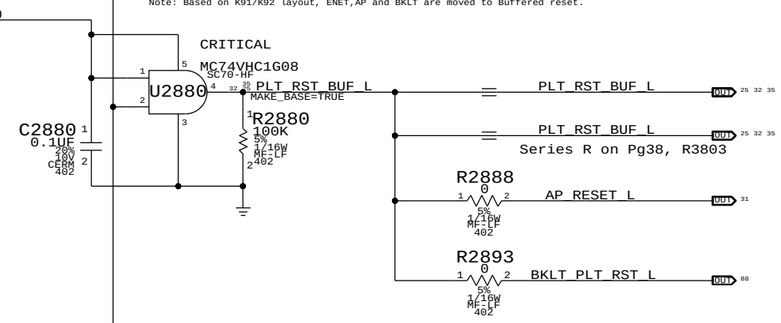
Series R is R4283

ENET_MEDIA_SENSE ISOLATION CIRCUIT



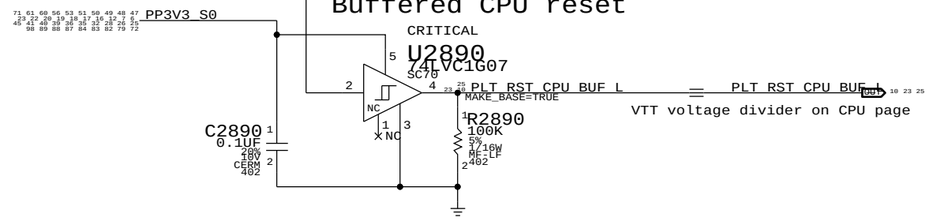
Buffered

Note: Based on K91/K92 layout, ENET,AP and BKLT are moved to Buffered reset.



Series R on Pg38, R3803

Buffered CPU reset



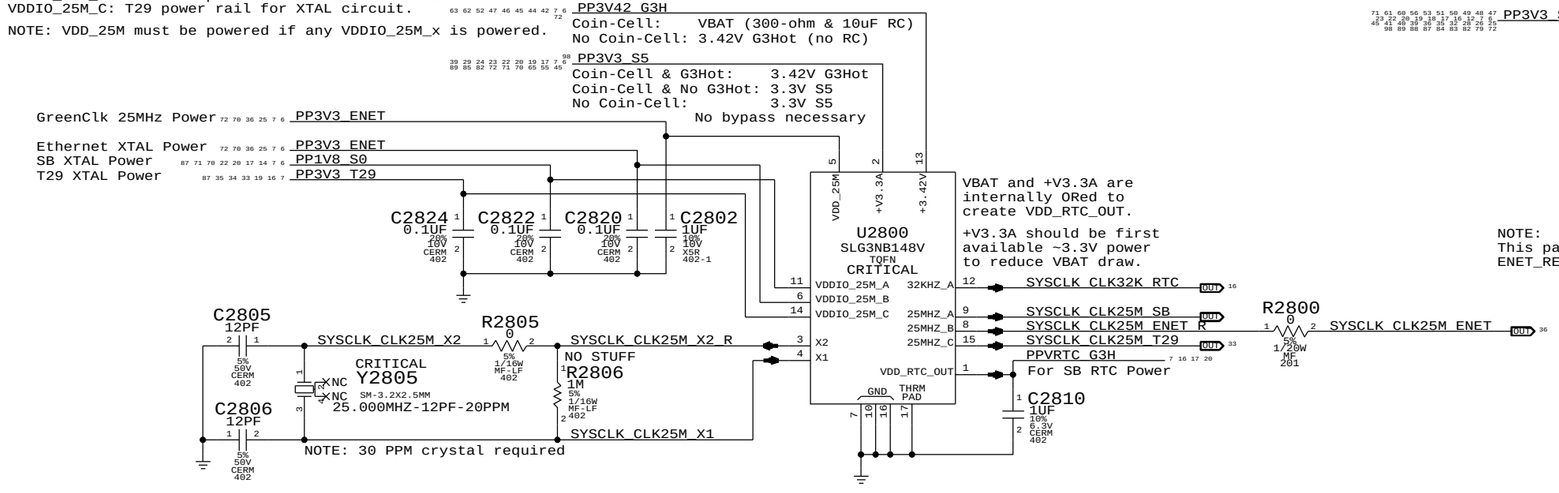
VTT voltage divider on CPU page

NOTE:
This page is different for K92.
ENET_RESET_L hooked up differently on both the projects.

System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.

+V3.3A should be first available ~3.3V power to reduce VBAT draw.

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_A_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

PP1V5_S3

C2910 0.1UF 20% 10V CERM 402
C2911 0.1UF 20% 10V CERM 402
C2912 0.1UF 20% 10V CERM 402
C2913 0.1UF 20% 10V CERM 402
C2914 0.1UF 20% 10V CERM 402
C2915 0.1UF 20% 10V CERM 402
C2916 0.1UF 20% 10V CERM 402
C2917 0.1UF 20% 10V CERM 402
C2918 0.1UF 20% 10V CERM 402
C2919 0.1UF 20% 10V CERM 402
C2920 0.1UF 20% 10V CERM 402
C2921 0.1UF 20% 10V CERM 402
C2922 0.1UF 20% 10V CERM 402
C2923 0.1UF 20% 10V CERM 402

PLACE_NEAR=J2900.75:2.54mm

C2900 10UF 20% 6.3V X6S 603
C2901 10UF 20% 6.3V X6S 603

PLACE_NEAR=J2900.75:2.54mm

PP0V75_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

OMIT_TABLE

J2900 F-RT-THB
DDR3-SODIMM-DUAL-K6 (SYMBOL 2 OF 2)

73	CKE0	CKE1	74	MEM_A_CKE<1>	
75	VDD	VDD	76		
77	NC	A15	78	MEM_A_A<15>	
79	BA2	A14	80	MEM_A_A<14>	
81	VDD	VDD	82		
83	A12/BC*	A11	84	MEM_A_A<11>	
85	A9	A7	86	MEM_A_A<7>	
87	VDD	VDD	88		
89	A8	A6	90	MEM_A_A<6>	
91	A5	A4	92	MEM_A_A<4>	
93	VDD	VDD	94		
95	A3	A2	96	MEM_A_A<2>	
97	A1	A0	98	MEM_A_A<0>	
99	VDD	VDD	100		
101	CK0	CK1	102	MEM_A_CLK_P<1>	
103	CK0*	CK1*	104	MEM_A_CLK_N<1>	
105	VDD	VDD	106		
107	A10/AP	BA1	108	MEM_A_BA<1>	
109	BA0	RAS*	110	MEM_A_RAS_L	
111	VDD	VDD	112		
113	WE*	S0*	114	MEM_A_CS_L<0>	
115	CAS*	ODT0	116	MEM_A_ODT<0>	
117	VDD	VDD	118		
119	A13	ODT1	120	MEM_A_ODT<1>	
121	S1*	NC	122	NC	
123	VDD	VDD	124		
125	TEST	VREFCA	126		
127	VSS	VSS	128		
129	DQ32	DQ36	130	MEM_A_DQ<32>	
131	DQ33	DQ37	132	MEM_A_DQ<37>	
133	VSS	VSS	134		
135	DQS4*	DM4	136		
137	DQS4	VSS	138		
139	VSS	DQ38	140	MEM_A_DQ<38>	
141	DQ34	DQ39	142	MEM_A_DQ<39>	
143	DQ35	VSS	144		
145	VSS	DQ44	146	MEM_A_DQ<44>	
147	DQ40	DQ45	148	MEM_A_DQ<45>	
149	DQ41	VSS	150		
151	VSS	DQS5*	152	MEM_A_DQS_N<5>	
153	DM5	DQS5	154	MEM_A_DQS_P<5>	
155	VSS	VSS	156		
157	DQ42	DQ46	158	MEM_A_DQ<46>	
159	DQ43	DQ47	160	MEM_A_DQ<47>	
161	VSS	VSS	162		
163	DQ48	DQ52	164	MEM_A_DQ<52>	
165	DQ49	DQ53	166	MEM_A_DQ<53>	
167	VSS	VSS	168		
169	DQS6*	DM6	170		
171	DQS6	VSS	172		
173	VSS	DQ54	174	MEM_A_DQ<54>	
175	DQ50	DQ55	176	MEM_A_DQ<55>	
177	DQ51	VSS	178		
179	VSS	DQ60	180	MEM_A_DQ<60>	
181	DQ56	DQ61	182	MEM_A_DQ<61>	
183	DQ57	VSS	184		
185	VSS	DQS7*	186	MEM_A_DQS_N<7>	
187	DM7	DQS7	188	MEM_A_DQS_P<7>	
189	VSS	VSS	190		
191	DQ58	DQ62	192	MEM_A_DQ<62>	
193	DQ59	DQ63	194	MEM_A_DQ<63>	
195	VSS	VSS	196		
197	SA0	EVENT*	198	MEM_EVENT_L	
199	VDDSPD	SDA	200	SMBUS_PCH_DATA	
201	SA1	SCL	202	SMBUS_PCH_CLK	
203	VTT	VTT	204		

NC
NC
NC

J2900 F-RT-THB
DDR3-SODIMM-DUAL-K6 (SYMBOL 1 OF 2)
CRITICAL

1	VREFDQ	VSS	2		
3	VSS	DQ4	4	=MEM_A_DQ<4>	
5	DQ0	DQ5	6	=MEM_A_DQ<5>	
7	DQ1	VSS	8		
9	VSS	DQS0*	10	=MEM_A_DQS_N<0>	
11	DM0	DQS0	12	=MEM_A_DQS_P<0>	
13	VSS	VSS	14		
15	DQ2	DQ6	16	=MEM_A_DQ<6>	
17	DQ3	DQ7	18	=MEM_A_DQ<7>	
19	VSS	VSS	20		
21	DQ8	DQ12	22	=MEM_A_DQ<12>	
23	DQ9	DQ13	24	=MEM_A_DQ<13>	
25	VSS	VSS	26		
27	DQS1*	DM1	28		
29	DQS1	RESET*	30	MEM_RESET_L	
31	VSS	VSS	32		
33	DQ10	DQ14	34	=MEM_A_DQ<14>	
35	DQ11	DQ15	36	=MEM_A_DQ<15>	
37	VSS	VSS	38		
39	DQ16	DQ20	40	=MEM_A_DQ<20>	
41	DQ17	DQ21	42	=MEM_A_DQ<21>	
43	VSS	VSS	44		
45	DQS2*	DM2	46		
47	DQS2	VSS	48		
49	VSS	DQ22	50	=MEM_A_DQ<22>	
51	DQ18	DQ23	52	=MEM_A_DQ<23>	
53	DQ19	VSS	54		
55	VSS	DQ28	56	=MEM_A_DQ<28>	
57	DQ24	DQ29	58	=MEM_A_DQ<29>	
59	DQ25	VSS	60		
61	VSS	DQS3*	62	=MEM_A_DQS_N<3>	
63	DM3	DQS3	64	=MEM_A_DQS_P<3>	
65	VSS	VSS	66		
67	DQ26	DQ30	68	=MEM_A_DQ<30>	
69	DQ27	DQ31	70	=MEM_A_DQ<31>	
71	VSS	VSS	72		

=MEM_A_DQ<0>
=MEM_A_DQ<1>
=MEM_A_DQ<2>
=MEM_A_DQ<3>
=MEM_A_DQ<8>
=MEM_A_DQ<9>
=MEM_A_DQS_N<1>
=MEM_A_DQS_P<1>
=MEM_A_DQ<10>
=MEM_A_DQ<11>
=MEM_A_DQ<16>
=MEM_A_DQ<17>
=MEM_A_DQS_N<2>
=MEM_A_DQS_P<2>
=MEM_A_DQ<18>
=MEM_A_DQ<19>
=MEM_A_DQ<24>
=MEM_A_DQ<25>
=MEM_A_DQ<26>
=MEM_A_DQ<27>

See CSA05 BOM table

PP0V75_S3_MEM_VREFCA_A

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

"Factory" (top) slot

PP3V3_S0

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

516-0229
SPD ADDR=0xA0(WR)/0xA1(RD)

PP0V75_S0_DDRVTT

C2950 1UF 10% 10V X5R 402
C2951 1UF 10% 10V X5R 402
C2952 1UF 10% 10V X5R 402
C2953 1UF 10% 10V X5R 402

SYNC_MASTER=K92_SUMA SYNC_DATE=06/23/2010

PAGE TITLE: DDR3 SO-DIMM Connector A

Apple Inc.

DRAWING NUMBER | SIZE: D
REVISION
BRANCH
PAGE: 29 OF 132
SHEET: 26 OF 101

8	7	6	5	4	3	2	1

CPU CHANNEL A DQS 0 -> DIMM A DQS 0

91 11 6	MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>	26
91 11 6	MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	26
91 11 6	MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	26
91 11 6	MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	26
91 11 6	MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	26
91 11 6	MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	26
91 11 6	MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	26
91 11 6	MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	26
91 11 6	MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	26
91 11 6	MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	26

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

91 11 6	MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	26
91 11 6	MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	26
91 11 6	MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	26
91 11 6	MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	26
91 11 6	MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	26
91 11 6	MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	26
91 11 6	MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	26
91 11 6	MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	26
91 11 6	MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	26
91 11 6	MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	26

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

91 11 6	MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	26
91 11 6	MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	26
91 11 6	MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<23>	26
91 11 6	MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	26
91 11 6	MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	26
91 11 6	MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	26
91 11 6	MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	26
91 11 6	MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	26
91 11 6	MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	26
91 11 6	MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	26

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

91 11 6	MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	26
91 11 6	MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	26
91 11 6	MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	26
91 11 6	MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	26
91 11 6	MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	26
91 11 6	MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	26
91 11 6	MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	26
91 11 6	MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	26
91 11 6	MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	26
91 11 6	MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	26

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

91 11 6	MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	26
91 11 6	MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	26
91 11 6	MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	26
91 11 6	MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<37>	26
91 11 6	MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	26
91 11 6	MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	26
91 11 6	MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	26
91 11 6	MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	26
91 11 6	MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	26
91 27 26 11 6	MEM_A_DQ<32>	MAKE_BASE=TRUE	MEM_A_DQ<32>	6 11 26 27 91

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

91 11 6	MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	26
91 11 6	MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	26
91 11 6	MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	26
91 11 6	MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	26
91 11 6	MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	26
91 11 6	MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	26
91 11 6	MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	26
91 11 6	MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	26
91 11 6	MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	26
91 11 6	MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	26

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

91 27 26 11 6	MEM_A_DQS_N<6>	MAKE_BASE=TRUE	MEM_A_DQS_N<6>	6 11 26 27 91
91 27 26 11 6	MEM_A_DQS_P<6>	MAKE_BASE=TRUE	MEM_A_DQS_P<6>	6 11 26 27 91
91 11 6	MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	26
91 11 6	MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	26
91 11 6	MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	26
91 11 6	MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	26
91 11 6	MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	26
91 11 6	MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	26
91 11 6	MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	26
91 11 6	MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	26

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

91 11 6	MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	26
91 11 6	MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	26
91 11 6	MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	26
91 11 6	MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	26
91 11 6	MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	26
91 11 6	MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	26
91 11 6	MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	26
91 11 6	MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	26
91 11 6	MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	26
91 11 6	MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	26

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

91 11 6	MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>	28
91 11 6	MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>	28
91 11 6	MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	28
91 11 6	MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<3>	28
91 11 6	MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	28
91 11 6	MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	28
91 11 6	MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	28
91 11 6	MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	28
91 11 6	MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	28
91 11 6	MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	28

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

91 11 6	MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>	28
91 11 6	MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	28
91 11 6	MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<15>	28
91 11 6	MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<14>	28
91 11 6	MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<13>	28
91 11 6	MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<12>	28
91 11 6	MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	28
91 11 6	MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<10>	28
91 11 6	MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	28
91 11 6	MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<8>	28

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

91 11 6	MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	28
91 11 6	MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	28
91 11 6	MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<23>	28
91 11 6	MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	28
91 11 6	MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	28
91 11 6	MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	28
91 11 6	MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	28
91 11 6	MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	28
91 11 6	MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<17>	28
91 11 6	MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	28

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

91 11 6	MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	28
91 11 6	MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	28
91 11 6	MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<31>	28
91 11 6	MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	28
91 11 6	MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	28
91 11 6	MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	28
91 11 6	MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	28
91 11 6	MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<26>	28
91 11 6	MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	28
91 11 6	MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	28

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

91 11 6	MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>	28
91 11 6	MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	28
91 11 6	MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<39>	28
91 11 6	MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<38>	28
91 11 6	MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<37>	28
91 11 6	MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<36>	28
91 11 6	MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<35>	28
91 11 6	MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<34>	28
91 11 6	MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	28
27 11 6 91 28	MEM_B_DQ<32>	MAKE_BASE=TRUE	MEM_B_DQ<32>	6 11 27 28 91

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

91 11 6	MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	28
91 11 6	MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	28
91 11 6	MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<47>	28
91 11 6	MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	28
91 11 6	MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	28
91 11 6	MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	28
91 11 6	MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	28
91 11 6	MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	28
91 11 6	MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	28
91 11 6	MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	28

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

27 11 6 91 28	MEM_B_DQS_N<6>	MAKE_BASE=TRUE	MEM_B_DQS_N<6>	6 11 27 28 91
27 11 6 91 28	MEM_B_DQS_P<6>	MAKE_BASE=TRUE	MEM_B_DQS_P<6>	6 11 27 28 91
91 11 6	MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<55>	28
91 11 6	MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	28
91 11 6	MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	28
91 11 6	MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	28
91 11 6	MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	28
91 11 6	MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	28
91 11 6	MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	28
91 11 6	MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	28

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

91 11 6	MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	28
91 11 6	MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	28
91 11 6	MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	28
91 11 6	MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	28
91 11 6	MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	28
91 11 6	MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	28
91 11 6	MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	28
91 11 6	MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	28
91 11 6	MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	28
91 11 6	MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	28

SYNC_MASTER=K92_SUMA SYNC_DATE=05/10/2010

PAGE TITLE

DDR3 Byte/Bit Swaps

Apple Inc.

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

PP1V5_S3

C3100 10UF 20% 6.3V X6S CERM 603
C3101 10UF 20% 6.3V X6S CERM 603
PLACE_NEAR=J3100.75:2.54mm

C3110 C3111 C3112 C3113 C3114 C3115 C3116 C3117 C3118 C3119 C3120 C3121 C3122 C3123
0.1UF 20% 10V CERM 402
PLACE_NEAR=J3100.75:2.54mm
PLACE_NEAR=J3100.75:2.54mm

PP0V75_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

PP0V75_S3_MEM_VREFCA_B

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

PP3V3_S0

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

PP0V75_S0_DDRVTT

C3150 C3151 C3152 C3153
1UF 10% 10V X5R 402

J3100 DDR3-SODIMM (2 OF 2)

OMIT_TABLE

KEY

			CKE0	73	
			VDD	75	
		NC×	NC	77	
		MEM_B_BA<2>	BA2	79	
			VDD	81	
		MEM_B_A<12>	A12/BC*	83	
		MEM_B_A<9>	A9	85	
			VDD	87	
		MEM_B_A<8>	A8	89	
		MEM_B_A<5>	A5	91	
			VDD	93	
		MEM_B_A<3>	A3	95	
		MEM_B_A<1>	A1	97	
			VDD	99	
		MEM_B_CLK_P<0>	CK0	101	
		MEM_B_CLK_N<0>	CK0*	103	
			VDD	105	
		MEM_B_A<10>	A10/AP	107	
		MEM_B_BA<0>	BA0	109	
			VDD	111	
		MEM_B_WE_L	WE*	113	
		MEM_B_CAS_L	CAS*	115	
			VDD	117	
		MEM_B_A<13>	A13	119	
		MEM_B_CS_L<1>	S1*	121	
			VDD	123	
		NC×	TEST	125	
			VSS	127	
		=MEM_B_DQ<32>	DQ32	129	
		=MEM_B_DQ<33>	DQ33	131	
			VSS	133	
		=MEM_B_DQS_N<4>	DQS4*	135	
		=MEM_B_DQS_P<4>	DQS4	137	
			VSS	139	
		=MEM_B_DQ<34>	DQ34	141	
		=MEM_B_DQ<35>	DQ35	143	
			VSS	145	
		=MEM_B_DQ<40>	DQ40	147	
		=MEM_B_DQ<41>	DQ41	149	
			VSS	151	
			DM5	153	
			VSS	155	
		=MEM_B_DQ<42>	DQ42	157	
		=MEM_B_DQ<43>	DQ43	159	
			VSS	161	
		=MEM_B_DQ<48>	DQ48	163	
		=MEM_B_DQ<49>	DQ49	165	
			VSS	167	
		MEM_B_DQS_N<6>	DQS6*	169	
		MEM_B_DQS_P<6>	DQS6	171	
			VSS	173	
		=MEM_B_DQ<50>	DQ50	175	
		=MEM_B_DQ<51>	DQ51	177	
			VSS	179	
		=MEM_B_DQ<56>	DQ56	181	
		=MEM_B_DQ<57>	DQ57	183	
			VSS	185	
			DM7	187	
			VSS	189	
		=MEM_B_DQ<58>	DQ58	191	
		=MEM_B_DQ<59>	DQ59	193	
			VSS	195	
		MEM_B_SA<0>	SA0	197	
PP3V3_S0			VDDSPD	199	
		MEM_B_SA<1>	SA1	201	
			VTT	203	
			MTG PIN	205	
			MTG PIN	207	
			MTG PIN	209	
			MTG PIN	211	

			CKE1	74	
			VDD	76	
		MEM_B_A<15>	A15	78	
		MEM_B_A<14>	A14	80	
			VDD	82	
		MEM_B_A<11>	A11	84	
		MEM_B_A<7>	A7	86	
			VDD	88	
		MEM_B_A<6>	A6	90	
		MEM_B_A<4>	A4	92	
			VDD	94	
		MEM_B_A<2>	A2	96	
		MEM_B_A<0>	A0	98	
			VDD	100	
		MEM_B_CLK_P<1>	CK1	102	
		MEM_B_CLK_N<1>	CK1*	104	
			VDD	106	
		MEM_B_BA<1>	BA1	108	
		MEM_B_RAS_L	RAS*	110	
			VDD	112	
		MEM_B_CS_L<0>	S0*	114	
		MEM_B_ODT<0>	ODT0	116	
			VDD	118	
		MEM_B_ODT<1>	ODT1	120	
		×NC	NC	122	
			VDD	124	
			VREFCA	126	
			VSS	128	
		=MEM_B_DQ<36>	DQ36	130	
		=MEM_B_DQ<37>	DQ37	132	
			VSS	134	
			DM4	136	
			VSS	138	
		=MEM_B_DQ<38>	DQ38	140	
		=MEM_B_DQ<39>	DQ39	142	
			VSS	144	
		=MEM_B_DQ<44>	DQ44	146	
		=MEM_B_DQ<45>	DQ45	148	
			VSS	150	
		=MEM_B_DQS_N<5>	DQS5*	152	
		=MEM_B_DQS_P<5>	DQS5	154	
			VSS	156	
		=MEM_B_DQ<46>	DQ46	158	
		=MEM_B_DQ<47>	DQ47	160	
			VSS	162	
		=MEM_B_DQ<52>	DQ52	164	
		=MEM_B_DQ<53>	DQ53	166	
			VSS	168	
			DM6	170	
			VSS	172	
		=MEM_B_DQ<54>	DQ54	174	
		=MEM_B_DQ<55>	DQ55	176	
			VSS	178	
		=MEM_B_DQ<60>	DQ60	180	
		=MEM_B_DQ<61>	DQ61	182	
			VSS	184	
		=MEM_B_DQS_N<7>	DQS7*	186	
		=MEM_B_DQS_P<7>	DQS7	188	
			VSS	190	
		=MEM_B_DQ<62>	DQ62	192	
		=MEM_B_DQ<63>	DQ63	194	
			VSS	196	
		MEM_EVENT_L	EVENT*	198	
		SMBUS_PCH_DATA	SDA	200	
		SMBUS_PCH_CLK	SCL	202	
PP0V75_S0_DDRVTT			VTT	204	
			MTG PIN	206	
			MTG PIN	208	
			MTG PIN	210	
			MTG PIN	212	

MTG PINS

516S0806
SPD ADDR=0xA4(WR)/0xA5(RD)

J3100 DDR3-SODIMM (1 OF 2)

OMIT_TABLE

CRITICAL

KEY

			VREFDQ	1	
			VSS	3	
		=MEM_B_DQ<0>	DQ0	5	
		=MEM_B_DQ<1>	DQ1	7	
			VSS	9	
			DM0	11	
			VSS	13	
		=MEM_B_DQ<2>	DQ2	15	
		=MEM_B_DQ<3>	DQ3	17	
			VSS	19	
		=MEM_B_DQ<8>	DQ8	21	
		=MEM_B_DQ<9>	DQ9	23	
			VSS	25	
		=MEM_B_DQS_N<1>	DQS1*	27	
		=MEM_B_DQS_P<1>	DQS1	29	
			VSS	31	
		=MEM_B_DQ<10>	DQ10	33	
		=MEM_B_DQ<11>	DQ11	35	
			VSS	37	
		=MEM_B_DQ<16>	DQ16	39	
		=MEM_B_DQ<17>	DQ17	41	
			VSS	43	
		=MEM_B_DQS_N<2>	DQS2*	45	
		=MEM_B_DQS_P<2>	DQS2	47	
			VSS	49	
		=MEM_B_DQ<18>	DQ18	51	
		=MEM_B_DQ<19>	DQ19	53	
			VSS	55	
		=MEM_B_DQ<24>	DQ24	57	
		=MEM_B_DQ<25>	DQ25	59	
			VSS	61	
			DM3	63	
			VSS	65	
		=MEM_B_DQ<26>	DQ26	67	
		=MEM_B_DQ<27>	DQ27	69	
			VSS	71	

			VSS	2	
		=MEM_B_DQ<4>	DQ4	4	
		=MEM_B_DQ<5>	DQ5	6	
			VSS	8	
		=MEM_B_DQS_N<0>	DQS0*	10	
		=MEM_B_DQS_P<0>	DQS0	12	
			VSS	14	
		=MEM_B_DQ<6>	DQ6	16	
		=MEM_B_DQ<7>	DQ7	18	
			VSS	20	
		=MEM_B_DQ<12>	DQ12	22	
		=MEM_B_DQ<13>	DQ13	24	
			VSS	26	
			DM1	28	
		MEM_RESET_L	RESET*	30	
			VSS	32	
		=MEM_B_DQ<14>	DQ14	34	
		=MEM_B_DQ<15>	DQ15	36	
			VSS	38	
		=MEM_B_DQ<20>	DQ20	40	
		=MEM_B_DQ<21>	DQ21	42	
			VSS	44	
			DM2	46	
			VSS	48	
		=MEM_B_DQ<22>	DQ22	50	
		=MEM_B_DQ<23>	DQ23	52	
			VSS	54	
		=MEM_B_DQ<28>	DQ28	56	
		=MEM_B_DQ<29>	DQ29	58	
			VSS	60	
		=MEM_B_DQS_N<3>	DQS3*	62	
		=MEM_B_DQS_P<3>	DQS3	64	
			VSS	66	
		=MEM_B_DQ<30>	DQ30	68	
		=MEM_B_DQ<31>	DQ31	70	
			VSS	72	

516S0806

"Expansion" (bottom) slot

SYNC_MASTER=K92_SUMA SYNC_DATE=06/23/2010

PAGE TITLE
DDR3 SO-DIMM Connector B

Apple Inc.

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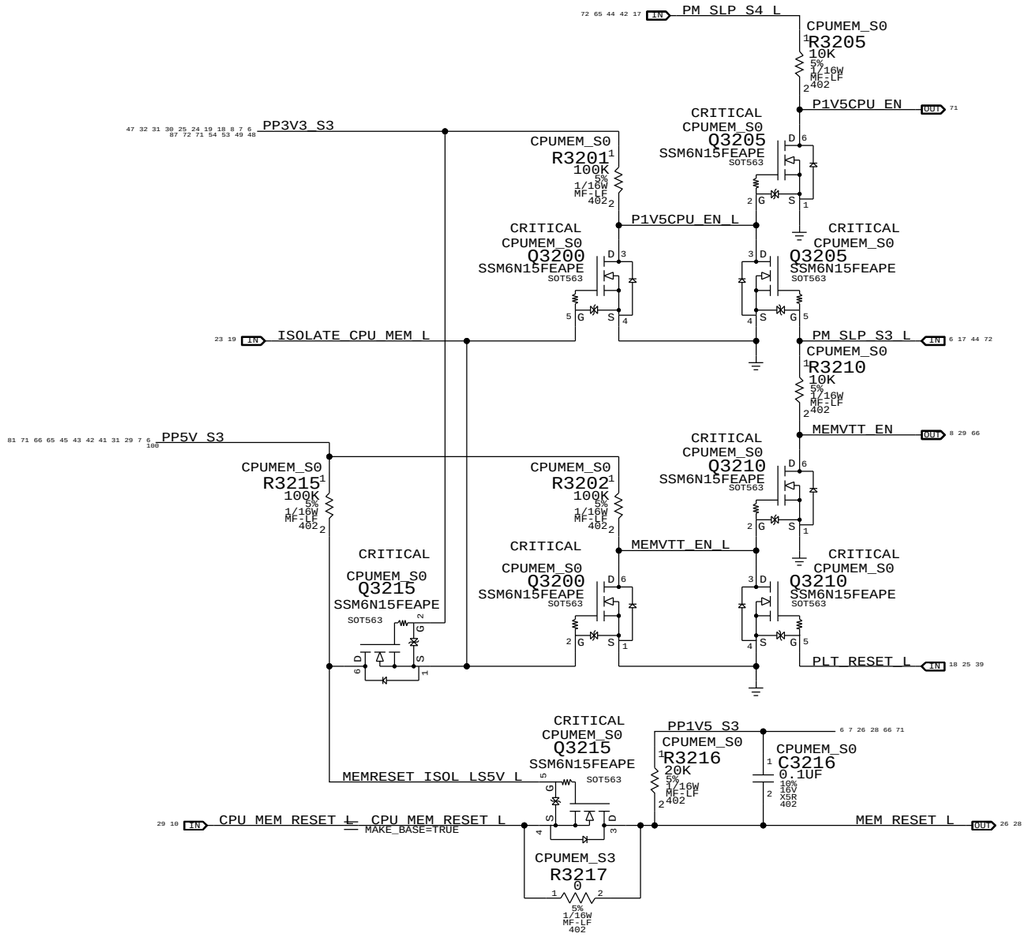
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

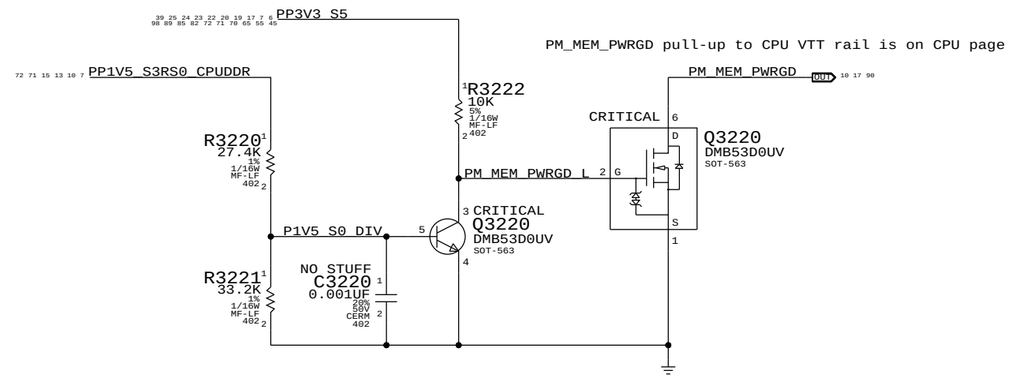


	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
to	4	0	0	1	1	X	1	0	1
S0	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

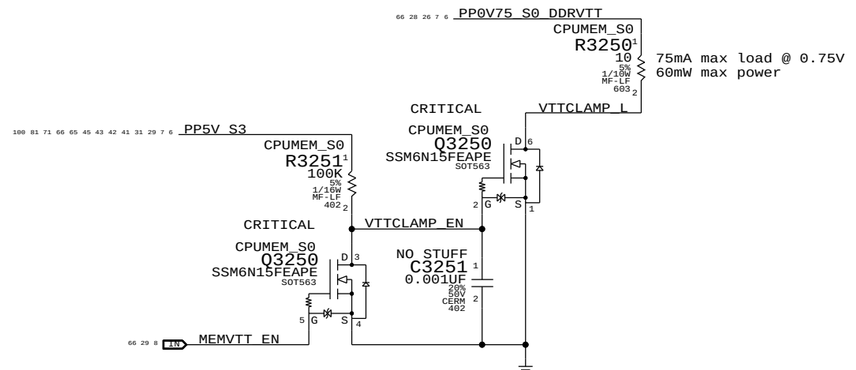
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

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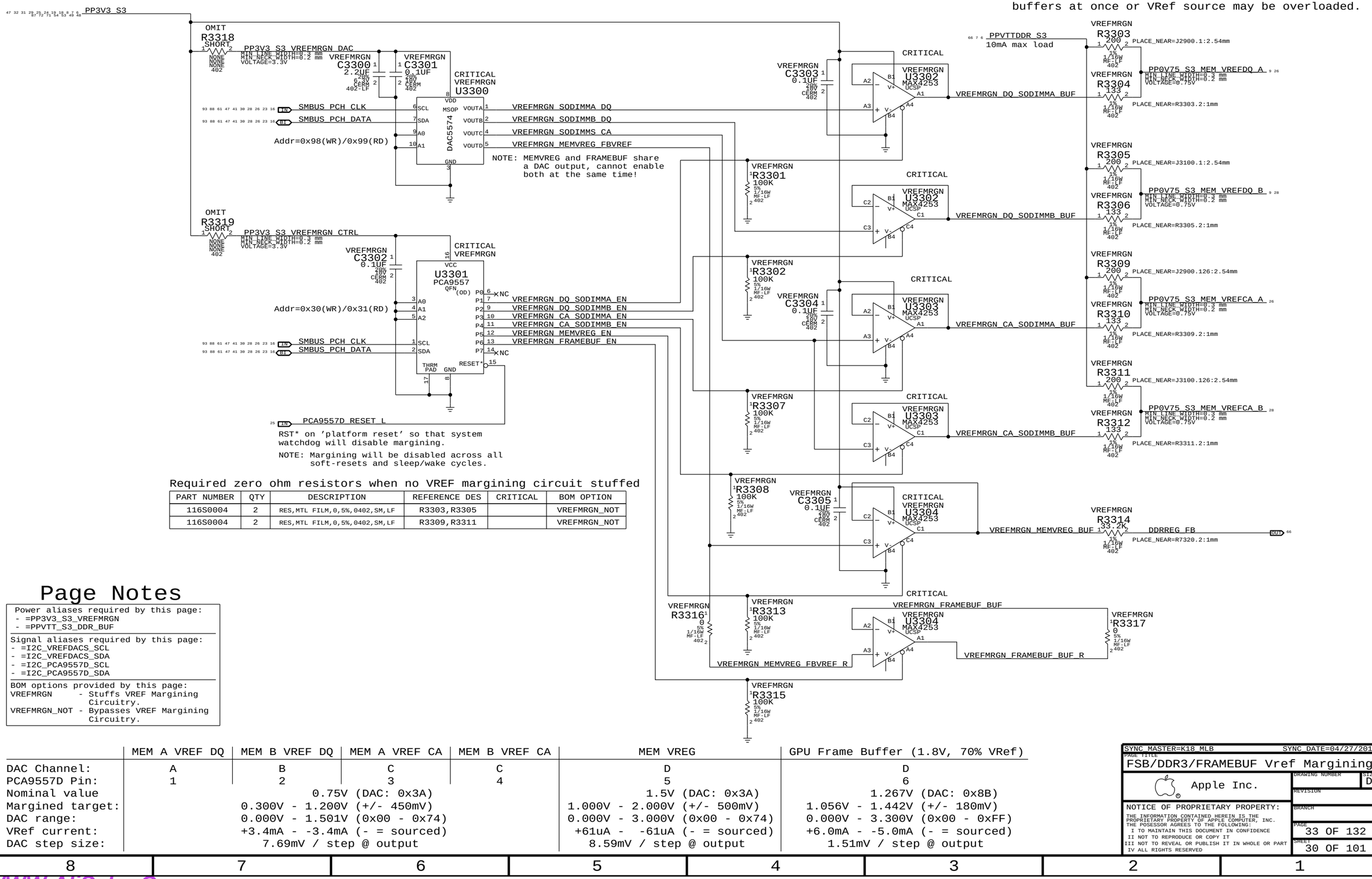

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

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AIRPORT

OMIT_TABLE
L3470
0.6NH+/-0.1NH-0.85A
0201
PCIE_AP_R2D_PI_P
PLACE_NEAR=J3401.15:2.54mm
C3431 0.1UF 10% 16V X5R 402-1
PCIE_AP_R2D_C_P
NOSTUFF C3470 0.1UF 10% 16V X5R-CERM 0201
NOSTUFF C3471 0.1UF 10% 16V X5R-CERM 0201

L3471
0.6NH+/-0.1NH-0.85A
0201
PCIE_AP_R2D_PI_N
C3430 0.1UF 10% 16V X5R 402-1
PCIE_AP_R2D_C_N
NOSTUFF C3472 0.1UF 10% 16V X5R-CERM 0201
OMIT_TABLE
NOSTUFF C3473 0.1UF 10% 16V X5R-CERM 0201
PLACE_NEAR=J3401.17:2.54mm

OMIT_TABLE
L3473
0.6NH+/-0.1NH-0.85A
0201
PCIE_AP_D2R_P
NOSTUFF C3474 0.1UF 10% 16V X5R-CERM 0201
NOSTUFF C3475 0.1UF 10% 16V X5R-CERM 0201

L3474
0.6NH+/-0.1NH-0.85A
0201
PCIE_AP_D2R_N
NOSTUFF C3476 0.1UF 10% 16V X5R-CERM 0201
OMIT_TABLE
NOSTUFF C3477 0.1UF 10% 16V X5R-CERM 0201

SMBUS_SMC_0_S0_SDA
SMBUS_SMC_0_S0_SCL
WIFI_EVENT_L
PCIE_AP_R2D_P
PCIE_AP_R2D_N
PCIE_AP_D2R_PI_P
PCIE_AP_D2R_PI_N

516S0582
CRITICAL
J3401
500913-0302
F-ST-SM

CRITICAL
L3401
90-OHM-100MA
DLP11S
PCIE_CLK100M_AP_P
PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_CONN_N
PCIE_CLK100M_AP_N
PLACE_NEAR=J3401.11:2.54mm

BLUETOOTH

USB_BT_P
USB_BT_N
PP3V3_S3_BT_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
C3432 0.01UF 10% 10V CERM 402
L3406
FERR-120-OHM-1.5A
0402-LF
PLACE_NEAR=J3401.27:2.54mm
PP3V3_S3

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0OHM, 0201	L3470,L3471,L3473,L3474		

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	1 A (EDP)

1A PEAK
155S0367
L3404
FERR-120-OHM-3A
0603
PP3V3_WLAN
PP3V3_WLAN_F
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.4 mm
MIN_LINE_WIDTH=1 mm
C3422 1UF 20% 10V CERM 402
C3421 0.1UF 20% 10V CERM 402
PLACE_NEAR=J3401.29:2.54mm
XW3452 SM
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
PP3V3_WLAN_R

CRITICAL
Q3450
TPCP8102
23V1K-SM
C3450 0.1UF 10% 16V X5R 402-1
P3V3WLAN_SS
C3451 0.033UF 10% 16V X5R 402
R3450 33K 5% 1/16W MF-LF 402
R3451 10K 5% 1/16W MF-LF 402
PP3V3_S3
PM_WLAN_EN_L

Supervisor & CLKFREG # Isolation
Delay = 60 ms +/- 20%

AP_RESET_CONN_L
AP_CLKREQ_Q_L
PCIE_WAKE_L

PP3V3_WLAN_F
PP3V3_S3
R3453 100K 1% 1/10W MF-LF 402
R3454 232K 1% 1/10W MF-LF 402
P3V3WLAN_VMON
R3455 100K 1% 1/10W MF-LF 402
CRITICAL
U3440
SLG4AP016V
TDFN
VDD
SENSE
0.7V
KDLY
RESET*
MR*
EN
IN
OUT
THRM PAD
GND
C3440 0.1UF 20% 10V CERM 402
AP_RESET_L
AP_PWR_EN
AP_CLKREQ_L

518S0816
CRITICAL
J3402
CCR20-6K710S
F-RT-SM
PP5V_S3_ALSCAMERA_F
SMBUS_SMC_A_S3_SCL
SMBUS_SMC_A_S3_SDA
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm

ALS CAMERA

CRITICAL
L3407
90-OHM
DLP0NS
USB_CAMERA_P
USB_CAMERA_N
PLACE_NEAR=J3402.3:2.54mm

275 mA peak
206 mA nominal max
PLACE_NEAR=J3402.6:2.54mm
L3408
FERR-120-OHM-1.5A
0402-LF
PP5V_S3
C3452 0.1uF 20% 10V CERM 402

SYNC_MASTER=K91_MARY SYNC_DATE=10/08/2010
PAGE TITLE
X19/ALS/CAMERA CONNECTOR
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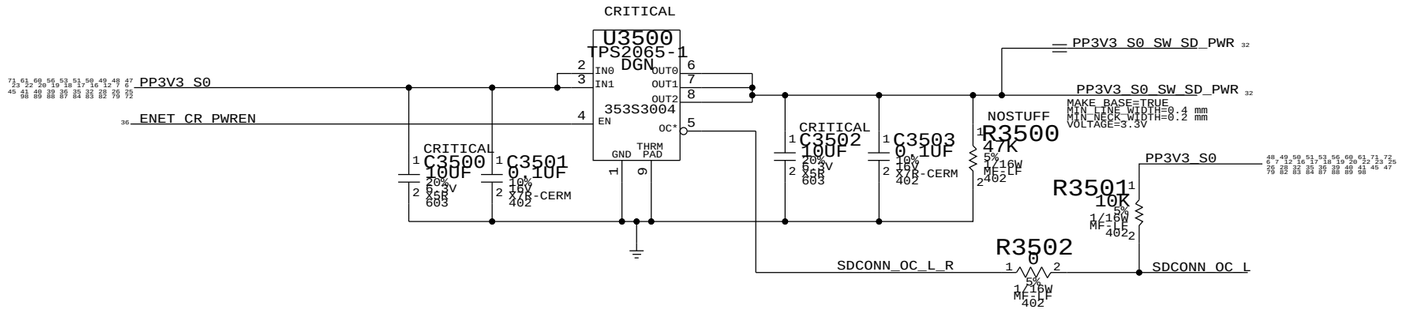
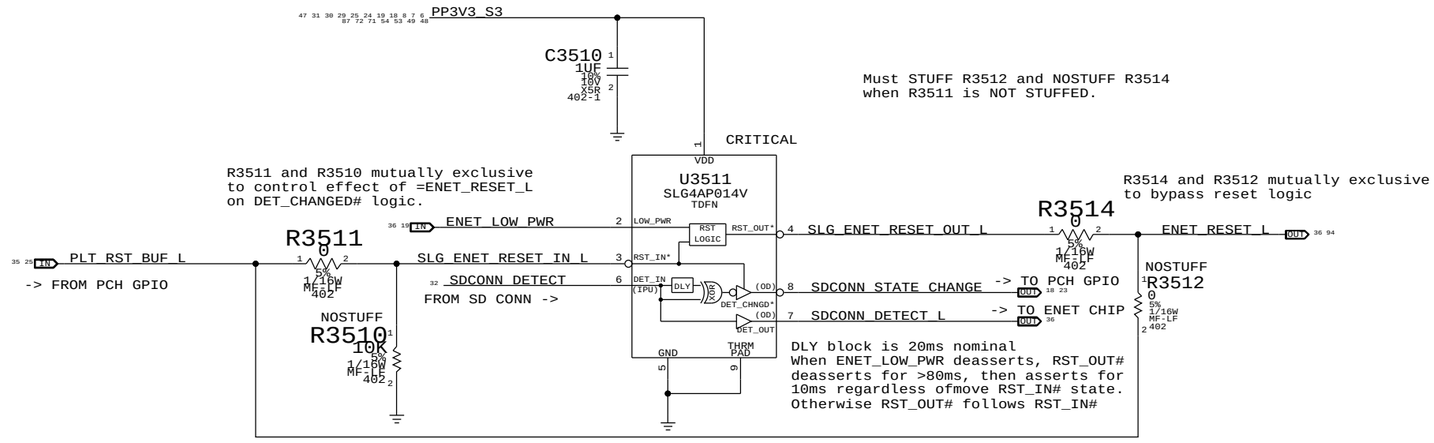
SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

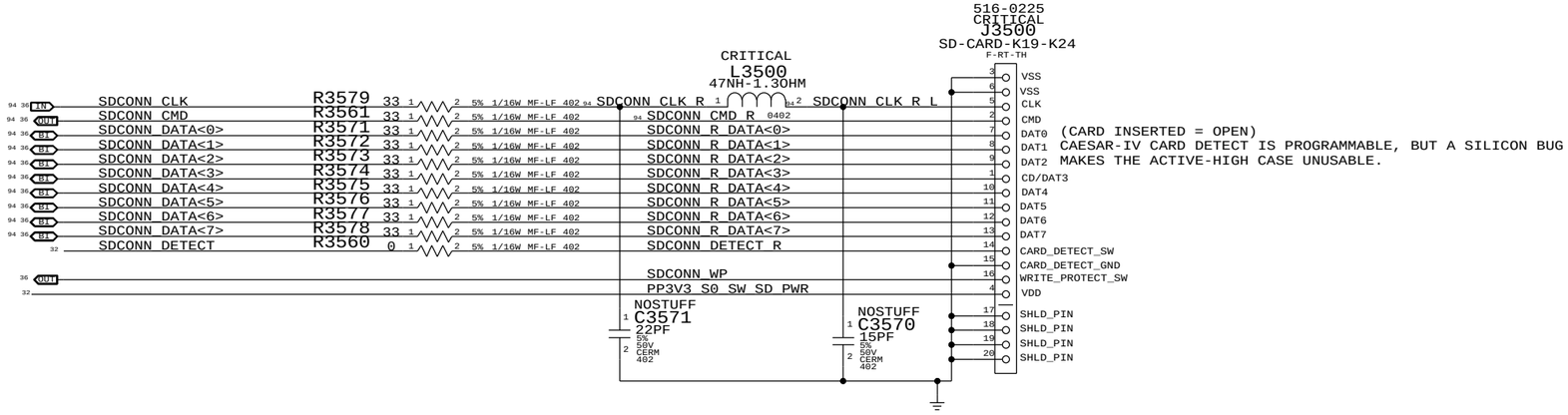
TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.



SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO LATCH CIRCUIT



SD CARD CONNECTOR



SYNC MASTER=K91_ERIC SYNC DATE=10/08/2010

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SD READER CONNECTOR

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CRITICAL

OMIT_TABLE

U3600

T29

FCBGA

(SYM 1 OF 2)

PCIE GEN2

RECEIVE

PCIE T29 R2D C P<0> C3600 0.1uF PCIE T29 R2D P<0> V19 PER_0_P
PCIE T29 R2D C N<0> C3601 0.1uF PCIE T29 R2D N<0> T19 PER_0_N
PCIE T29 R2D C P<1> C3602 0.1uF PCIE T29 R2D P<1> P19 PER_1_P
PCIE T29 R2D C N<1> C3603 0.1uF PCIE T29 R2D N<1> M19 PER_1_N
PCIE T29 R2D C P<2> C3604 0.1uF PCIE T29 R2D P<2> K19 PER_2_P
PCIE T29 R2D C N<2> C3605 0.1uF PCIE T29 R2D N<2> H19 PER_2_N
PCIE T29 R2D C P<3> C3606 0.1uF PCIE T29 R2D P<3> F19 PER_3_P
PCIE T29 R2D C N<3> C3607 0.1uF PCIE T29 R2D N<3> D19 PER_3_N

TRANSMIT

PET_0_P V21 PCIE T29 D2R C P<0> C3640 0.1uF PCIE T29 D2R P<0>
PET_0_N T21 PCIE T29 D2R C N<0> C3641 0.1uF PCIE T29 D2R N<0>
PET_1_P P21 PCIE T29 D2R C P<1> C3642 0.1uF PCIE T29 D2R P<1>
PET_1_N M21 PCIE T29 D2R C N<1> C3643 0.1uF PCIE T29 D2R N<1>
PET_2_P K21 PCIE T29 D2R C P<2> C3644 0.1uF PCIE T29 D2R P<2>
PET_2_N H21 PCIE T29 D2R C N<2> C3645 0.1uF PCIE T29 D2R N<2>
PET_3_P F21 PCIE T29 D2R C P<3> C3646 0.1uF PCIE T29 D2R P<3>
PET_3_N D21 PCIE T29 D2R C N<3> C3647 0.1uF PCIE T29 D2R N<3>

TP T29_MONDC0 R3610 0 NO STUFF T29_MONDC0 B21 MONDC0
DEBUG: For monitoring current/voltage
TP T29_MONDC1 R3611 0 NO STUFF T29_MONDC1 A20 MONDC1
TP T29_MONOBSP C3615 0.1uF T29_MONOBSP K17 MONOBSP
DEBUG: For monitoring clock
TP T29_MONOBSN C3616 0.1uF T29_MONOBSN M17 MONOBSN

PP3V3_T29

WAKE* F1 T29_PCIE_WAKE_L R3651 10K PP3V3_T29
PERST* E6 T29_RESET_L
RSENSE E14 T29_RSENSE R3655 1.0K
RBIAS E16 T29_RBIAS

MISC

CLK REQUEST

CLKREQ_ISOL_L P3 PCIE_CLKREQ_0*
T29_GPIO<1> N4 PCIE_CLKREQ_1*
T29_GPIO<2> M3 PCIE_CLKREQ_2*
T29_RSVD L4 PCIE_CLKREQ_3*

EEPROM

T29_SPI_MOSI P1 EE_DI
T29_SPI_MISO M1 EE_DO
T29_SPI_CS_L N2 EE_CS*
T29_SPI_CLK L2 EE_CLK

R3690 3.3K R3691 3.3K C3690 1UF 10V CERM 402
CRITICAL
OMIT_TABLE
U3690 M95160 2KX8-1.8V MLP
(T29_SPI_MOSI) (T29_SPI_CLK) (T29_SPI_CS_L) T29ROM_WP_L T29ROM_HOLD_L (T29_SPI_MISO)
R3692 3.3K R3693 3.3K R3623 10K R3622 10K R3621 10K

THERM_DP

T29_THERMD_P A2
Use B1 GND ball for THERM_DN

TEST PORT

T29_TEST_EN E4 TEST_EN
TP T29_TEST_POINT_0 P5 TEST_POINT_0
TP T29_TEST_POINT_1 N6 TEST_POINT_1
TP T29_TEST_POINT_2 M5 TEST_POINT_2
T29_TEST_POINT_3 L6 TEST_POINT_3

R3625 0

R3629 0

POWER ON RESET

PCIE_RST_0* K1 TP_T29_PCIE_RESET0_L
PCIE_RST_1* J2 TP_T29_PCIE_RESET1_L
PCIE_RST_2* K3 TP_T29_PCIE_RESET2_L
PCIE_RST_3* J4 TP_T29_PCIE_RESET3_L

Not used in host mode.

JTAG

TDI T3 JTAG_ISP_TDI
TMS R4 JTAG_T29_TMS
TCK R2 JTAG_ISP_TCK
TDO T1 JTAG_ISP_TDO

PP3V3_T29

R3698 10K R3695 806 SYSCLK_CLK25M_T29 R3696 1K

CLOCKS

REFCLK_100_IN_P H17 PCIE_CLK100M_T29_P
REFCLK_100_IN_N G16 PCIE_CLK100M_T29_N
XTAL_25_IN P17 SYSCLK_CLK25M_T29_R
XTAL_25_OUT R16 TP_T29_XTAL25OUT
TMU_CLK_OUT U2 T29_TMU_CLK_OUT
TMU_CLK_IN E2 T29_TMU_CLK_IN

NO STUFF R3699 10K

DISPLAY

SINK PORT 0

DP_T29SNK0_ML_P<3> AA4 DPSNK0_ML_LANE_3P
DP_T29SNK0_ML_N<3> Y3 DPSNK0_ML_LANE_3N
DP_T29SNK0_ML_P<2> AA6 DPSNK0_ML_LANE_2P
DP_T29SNK0_ML_N<2> Y5 DPSNK0_ML_LANE_2N
DP_T29SNK0_ML_P<1> AA8 DPSNK0_ML_LANE_1P
DP_T29SNK0_ML_N<1> Y7 DPSNK0_ML_LANE_1N
DP_T29SNK0_ML_P<0> AA10 DPSNK0_ML_LANE_0P
DP_T29SNK0_ML_N<0> Y9 DPSNK0_ML_LANE_0N
DP_T29SNK0_AUXCH_P V1 DPSNK0_AUX_CHP
DP_T29SNK0_AUXCH_N W2 DPSNK0_AUX_CHN
DP_T29SNK0_HPD V5 DPSNK0_HOT_PLUG_DET

SINK PORT 1

DP_T29SNK1_ML_P<3> V9 DPSNK1_ML_LANE_3P
DP_T29SNK1_ML_N<3> U8 DPSNK1_ML_LANE_3N
DP_T29SNK1_ML_P<2> V11 DPSNK1_ML_LANE_2P
DP_T29SNK1_ML_N<2> U10 DPSNK1_ML_LANE_2N
DP_T29SNK1_ML_P<1> V13 DPSNK1_ML_LANE_1P
DP_T29SNK1_ML_N<1> U12 DPSNK1_ML_LANE_1N
DP_T29SNK1_ML_P<0> V15 DPSNK1_ML_LANE_0P
DP_T29SNK1_ML_N<0> U14 DPSNK1_ML_LANE_0N
DP_T29SNK1_AUXCH_P V7 DPSNK1_AUX_CHP
DP_T29SNK1_AUXCH_N U6 DPSNK1_AUX_CHN
DP_T29SNK1_HPD U4 DPSNK1_HOT_PLUG_DET

R3630 100K R3631 100K

SOURCE PORT 0

DPSRC0_ML_LANE_3P AA18 TP_DP_T29SRC_ML_CP<3>
DPSRC0_ML_LANE_3N Y17 TP_DP_T29SRC_ML_CN<3>
DPSRC0_ML_LANE_2P AA16 TP_DP_T29SRC_ML_CP<2>
DPSRC0_ML_LANE_2N Y15 TP_DP_T29SRC_ML_CN<2>
DPSRC0_ML_LANE_1P AA14 TP_DP_T29SRC_ML_CP<1>
DPSRC0_ML_LANE_1N Y13 TP_DP_T29SRC_ML_CN<1>
DPSRC0_ML_LANE_0P AA12 TP_DP_T29SRC_ML_CP<0>
DPSRC0_ML_LANE_0N Y11 TP_DP_T29SRC_ML_CN<0>
DPSRC0_AUX_CHP W16 TP_DP_T29SRC_AUXCH_CP
DPSRC0_AUX_CHN U16 TP_DP_T29SRC_AUXCH_CN
DPSRC0_HOT_PLUG_DET V3 DP_T29SRC_HPD

100pF SRF > 40MHz
BYPASS=U3600.Y19::2mm
BYPASS=U3600.Y19::5.08mm

DP_ATEST Y19 T29_DP_ATEST
DP_RES_0 Y21
DP_RES_1 AA20 T29_DP_RES

R3685 14.0K R3632 100K C3685 100PF C3686 0.01UF

PORTS

PORT0

T29_R2D_C_P<0> A6 PRT0_T29T_P
T29_R2D_C_N<0> A4 PRT0_T29T_N
T29_D2R_P<0> C4 PRT0_T29R_P
T29_D2R_N<0> C2 PRT0_T29R_N
T29_LSEO<0> J6 T29_0_LSEO
T29_LSOE<0> K5 T29_0_LSOE

PORT1

T29_R2D_C_P<1> A10 PRT1_T29T_P
T29_R2D_C_N<1> A8 PRT1_T29T_N
T29_D2R_P<1> C8 PRT1_T29R_P
T29_D2R_N<1> C6 PRT1_T29R_N
T29_LSEO<1> G6 T29_1_LSEO
T29_LSOE<1> H5 T29_1_LSOE

I2C_T29_SDA F3 T29_SDA
I2C_T29_SCL F5 T29_SCL

PORT2

PRT2_T29T_P A14 NC_T29_R2D_CP<2>
PRT2_T29T_N A12 NC_T29_R2D_CN<2>
PRT2_T29R_P C12 NC_T29_D2RP<2>
PRT2_T29R_N C10 NC_T29_D2RN<2>
T29_2_LSEO G4 T29_LSEO_LSOE2
T29_2_LSOE H3 T29_LSEO_LSOE2

PORT3

PRT3_T29T_P A18 NC_T29_R2D_CP<3>
PRT3_T29T_N A16 NC_T29_R2D_CN<3>
PRT3_T29R_P C16 NC_T29_D2RP<3>
PRT3_T29R_N C14 NC_T29_D2RN<3>
T29_3_LSEO G2 T29_LSEO_LSOE3
T29_3_LSOE H1 T29_LSEO_LSOE3

NOTE: All unused LSOE/EO pairs should be aliased together. Other signals okay to float (TP/NC).

SNK0 AC Coupling

DP_T29SNK0_ML_C_P<0> C3620 0.1uF DP_T29SNK0_ML_P<0>
DP_T29SNK0_ML_C_N<0> C3621 0.1uF DP_T29SNK0_ML_N<0>
DP_T29SNK0_ML_C_P<1> C3622 0.1uF DP_T29SNK0_ML_P<1>
DP_T29SNK0_ML_C_N<1> C3623 0.1uF DP_T29SNK0_ML_N<1>
DP_T29SNK0_ML_C_P<2> C3624 0.1uF DP_T29SNK0_ML_P<2>
DP_T29SNK0_ML_C_N<2> C3625 0.1uF DP_T29SNK0_ML_N<2>
DP_T29SNK0_ML_C_P<3> C3626 0.1uF DP_T29SNK0_ML_P<3>
DP_T29SNK0_ML_C_N<3> C3627 0.1uF DP_T29SNK0_ML_N<3>
DP_T29SNK0_AUXCH_C_P C3628 0.1uF DP_T29SNK0_AUXCH_P
DP_T29SNK0_AUXCH_C_N C3629 0.1uF DP_T29SNK0_AUXCH_N

SNK1 AC Coupling

DP_T29SNK1_ML_C_P<0> C3630 0.1uF DP_T29SNK1_ML_P<0>
DP_T29SNK1_ML_C_N<0> C3631 0.1uF DP_T29SNK1_ML_N<0>
DP_T29SNK1_ML_C_P<1> C3632 0.1uF DP_T29SNK1_ML_P<1>
DP_T29SNK1_ML_C_N<1> C3633 0.1uF DP_T29SNK1_ML_N<1>
DP_T29SNK1_ML_C_P<2> C3634 0.1uF DP_T29SNK1_ML_P<2>
DP_T29SNK1_ML_C_N<2> C3635 0.1uF DP_T29SNK1_ML_N<2>
DP_T29SNK1_ML_C_P<3> C3636 0.1uF DP_T29SNK1_ML_P<3>
DP_T29SNK1_ML_C_N<3> C3637 0.1uF DP_T29SNK1_ML_N<3>
DP_T29SNK1_AUXCH_C_P C3638 0.1uF DP_T29SNK1_AUXCH_P
DP_T29SNK1_AUXCH_C_N C3639 0.1uF DP_T29SNK1_AUXCH_N

SYNC_MASTER=T29_REF SYNC_DATE=10/12/2010

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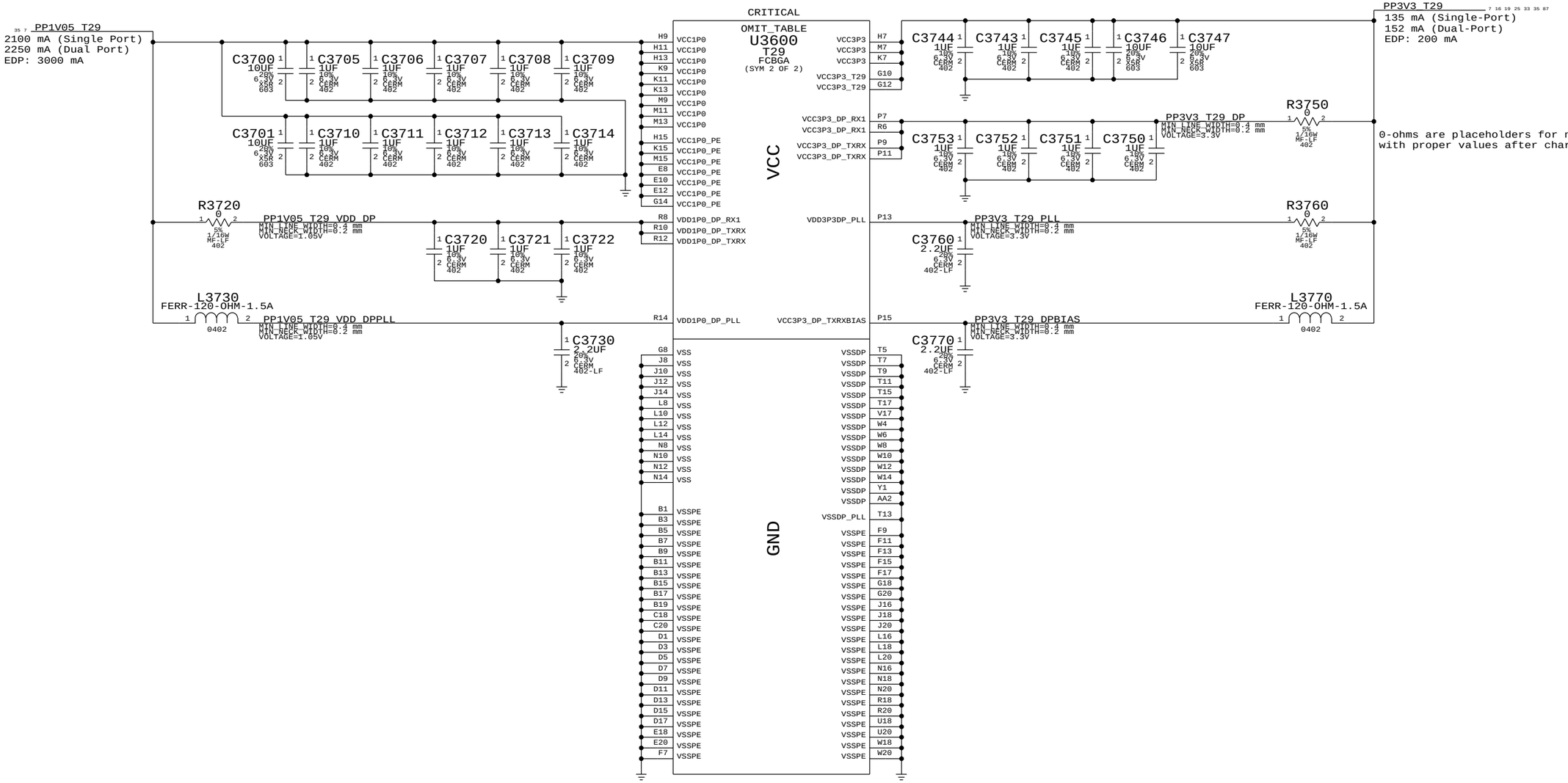

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=T29_REF SYNC_DATE=10/12/2010

PAGE TITLE: T29 Host (2 of 2)

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

T29 15V Boost Regulator

PPBUS_G3H
8-13V Input
Changes required for 2S.

CRITICAL T29BST:Y Q3880 SI8409DB 8A

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_SW_T29BST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

CRITICAL T29BST:Y L3895 10UH-4A-68-MOHM PCMB063T-100MS

T29BST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL T29BST:Y U3890 LT3957 QFN

T29BST_SNS1
T29BST_SNS2
T29BST_VSNS
T29BST_INTVCC
T29BST_VC
T29BST_RT
T29BST_SS
T29BST_FBX
T29BST_EN_UVLO
T29BST_VC_RC
GND_T29BST_SGND
SGND

CRITICAL T29BST:Y D3895 POWERDI-123 DFLS230L

XW3895 SM PLACE_NEAR=C3895.1:2 mm

NO STUFF C3889 100PF

PP15V_T29
Vout = 15V
Max Current = 0.8A
Freq = 300KHz

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

SGND shorted to GND inside package, no XW necessary.

Vout = 1.6V * (1 + Ra / Rb)

T29 A HV EN

Max Vgs: 10V

T29BST_SHDN_DIV

SMC_DELAYED_PWRGD

Supervisor & CLKREQ# Isolation

PP3V3_S0

Platform (PCIe) Reset
PLT_RST_BUF_L

CRITICAL U3800 SLG4AP016V TDFN

PP3V3_T29
PP1V05_T29

Open-Drain GPIO
T29_SW_RESET_L
T29_RESET_L
DLY = 60 ms +/- 20%

T29_CLKREQ_L
Pull-up provided by SB page.

T29_CLKREQ_ISOL_L
MAKE_BASE=TRUE

3.3V T29 Switch

U3810 TPS22924 CSP CRITICAL

PP3V3_S0
PP3V3_T29
Max Current = 1.7A (85C)

U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

1.05V T29 Switch

U3815 TPS22924 CSP CRITICAL

PP1V05_S0
PP1V05_T29
Max Current = 3.4A (85C)

U3816 TPS22924 CSP CRITICAL

T29_PWR_EN
Pull-up provided by SB page.

U3816.A2: PLACE_NEAR=U3815.B2:3 mm

SYNC_MASTER=T29_REF
SYNC_DATE=10/12/2016

PAGE TITLE: T29 Power Support

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

PP3V3_ENET
281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
PP3V3R1V8_ENET_LR_OUT_REG

CRITICAL L3900 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_XTALVDDH — C3900 0.1UF
CRITICAL L3905 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_BIASVDDH — C3905 0.1UF
CRITICAL L3910 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_AVDDH — R3910 4.7K, C3910 0.1UF, C3911 0.1UF

R3940 4.7K, R3941 4.7K
C3915 4.7UF, C3916 0.1UF

ENET_SR_LX
PP1V2_ENET

Internal 1.2V Switching Regulator pins.

CRITICAL L3920 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_AVDDL — C3921 0.1UF, C3920 4.7UF
CRITICAL L3925 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_PCIEPLL — C3926 0.1UF, C3925 4.7UF
CRITICAL L3930 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_GPHYPLL — C3931 0.1UF, C3930 4.7UF
C3936 0.1UF, CRITICAL C3935 10UF

PP1V2_ENET
???mA (1000base-T, Caesar V)

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

PP3V3_S0
R3942 1K Current Limiting Resistor
C3950 0.1uF, C3951 0.1uF, C3955 0.1uF, C3956 0.1uF
R3943 0

OMIT
U3900
BCM57765B0
QFN-8X8

PCIE_ENET_D2R_N	PCIE_TXD_N	
PCIE_ENET_D2R_P	PCIE_TXD_P	
PCIE_ENET_R2D_C_P	PCIE_RXD_P	
PCIE_ENET_R2D_C_N	PCIE_RXD_N	
ENET_WAKE_L (See note)	PCIE_REFCLK_P	
	PCIE_REFCLK_N	
ENET_VMAIN_PRSNT	VMAIN_PRSNT(IPD)	
ENET_RESET_L	PERST* (IPD)	
ENET_CLKREQ_L	CLKREQ* (OD)	
ENET_WAKE_R_L	WAKE* (OD)	
ENET_LOW_PWR	LOW_PWR (IPD)	
BCM57765_SMB_CLK	SMB_CLK	
BCM57765_SMB_DATA	SMD_DATA (IPD)	
BCM57765_SCLK	SCLK	
BCM57765_MISO	SI/LINKLED*	
BCM57765_MOSI	SO	
BCM57765_CS_L	CS*	
TP_BCM57765_SPD100LED_L	SPD100LED*/SERIAL_DO (OD)	
TP_BCM57765_TRAFFICLED_L	TRAFFICLED*/SERIAL_DI (OD)	
SYSCLK_CLK25M_ENET	XTALI	
NC	XTALO	
BCM57765_RDAC	RDAC	
	THRM_PAD	

	ENET_MDI_P<0>	
	ENET_MDI_N<0>	
	ENET_MDI_P<1>	
	ENET_MDI_N<1>	
	ENET_MDI_P<2>	
	ENET_MDI_N<2>	
	ENET_MDI_P<3>	
	ENET_MDI_N<3>	
GPIO_0	NC	
GPIO_1/CR_BUS_PWR	ENET_MEDIA_SENSE	
RE*/GPIO_2	SDCONN_DETECT_L	
(IPU) DETECT/WE*	SDCONN_CMD	
(IPU) CR_CMD/CLE	SDCONN_CLK	
CR_CLK/RY_BY*	SDCONN_DATA<0>	
CR_DATA0	SDCONN_DATA<1>	
CR_DATA1	SDCONN_DATA<2>	
CR_DATA2	SDCONN_DATA<3>	
CR_DATA3	SDCONN_DATA<4>	
CR_DATA4	SDCONN_DATA<5>	
CR_DATA5	SDCONN_DATA<6>	
CR_DATA6	SDCONN_DATA<7>	
CR_DATA7		
CE*/MS_INS*	TP_CE_L_MS_INS_L	
CR_LED/ALE	ENET_CR_PWREN	
CR_WP*/XD_WP*	SDCONN_WP	
XD_DETECT	BDM57765_SR_DISABLE	

NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.

R3965 1.24K

BCM57765 supports both active-levels for WP.

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

R3980 1K

SR_DISABLE must be pulled down to use internal SR. IPD has a race condition.

PP3V3R1V8_ENET_LR_OUT_REG
PP3V3R1V8_ENET_LR_OUT_REG
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C3970 4.7UF, C3971 0.1UF, C3972 0.1UF

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Required for proper PHY operation.
(Required ROM size TBD)

PP3V3_ENET
C3990 0.1UF
U3990 AT45DB011D SOIC-8S1 OMIT
BCM57765_SCLK, BCM57765_CS_L, BCM57765_MOSI, BCM57765_MISO
NOSTUFF R3990 4.7K, R3997 4.7K

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=K91_ERIC SYNC_DATE=10/11/2010
PAGE TITLE
ETHERNET PHY (CAESAR IV)

Apple Inc.

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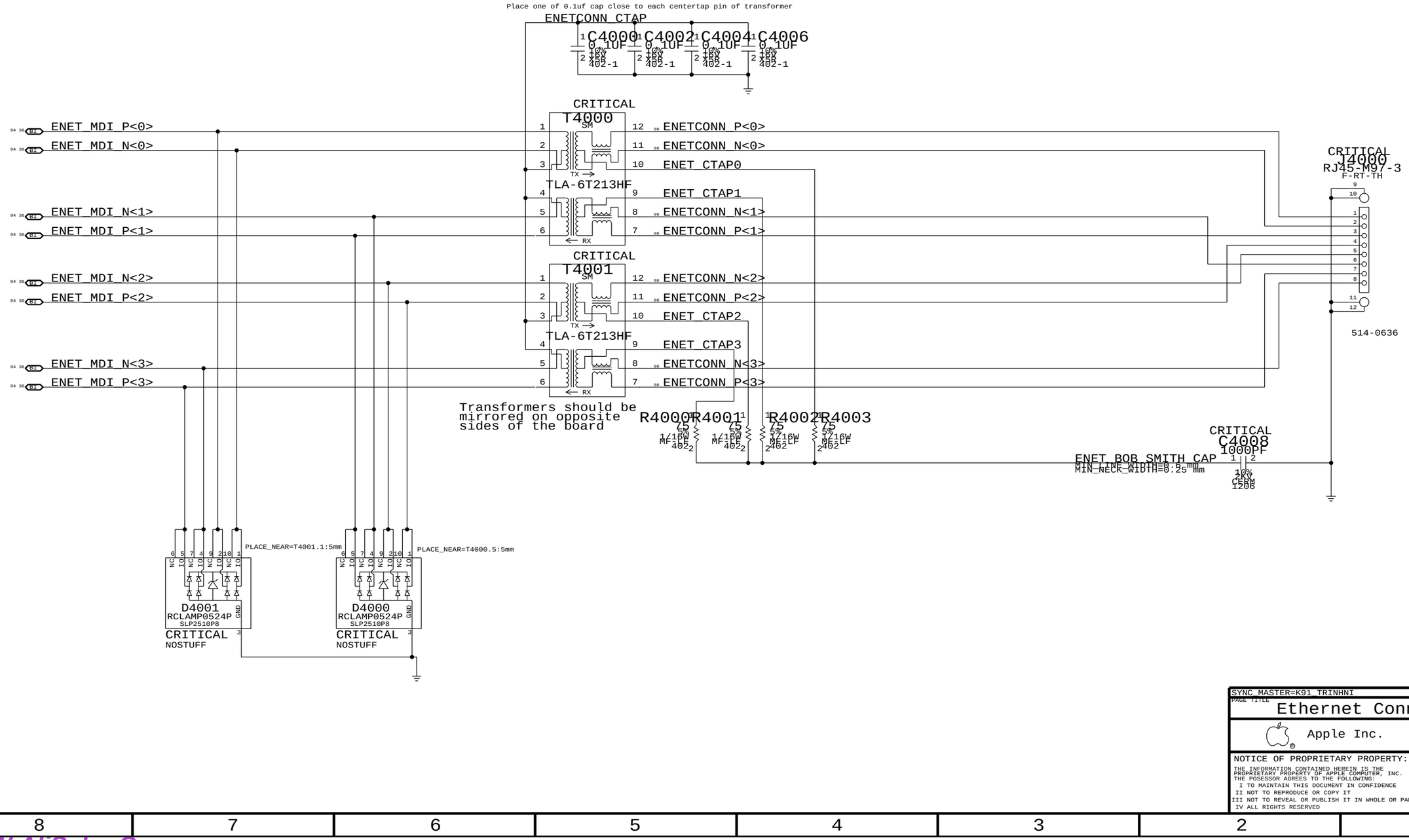
Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K91_TRINHNI SYNC_DATE=05/26/2010

PAGE TITLE
Ethernet Connector

Apple Inc.

DRAWING NUMBER
SIZE D

REVISION

BRANCH

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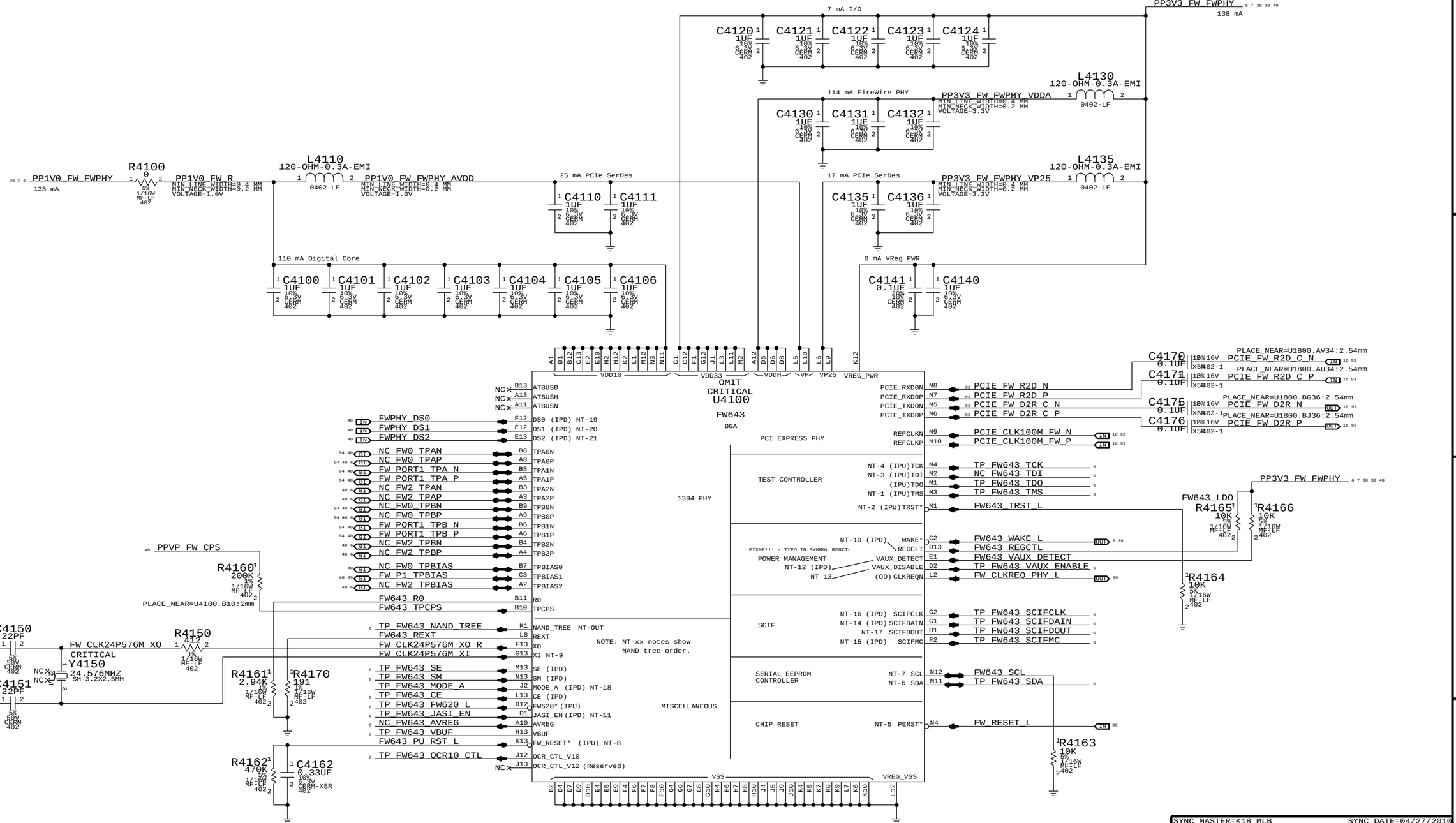


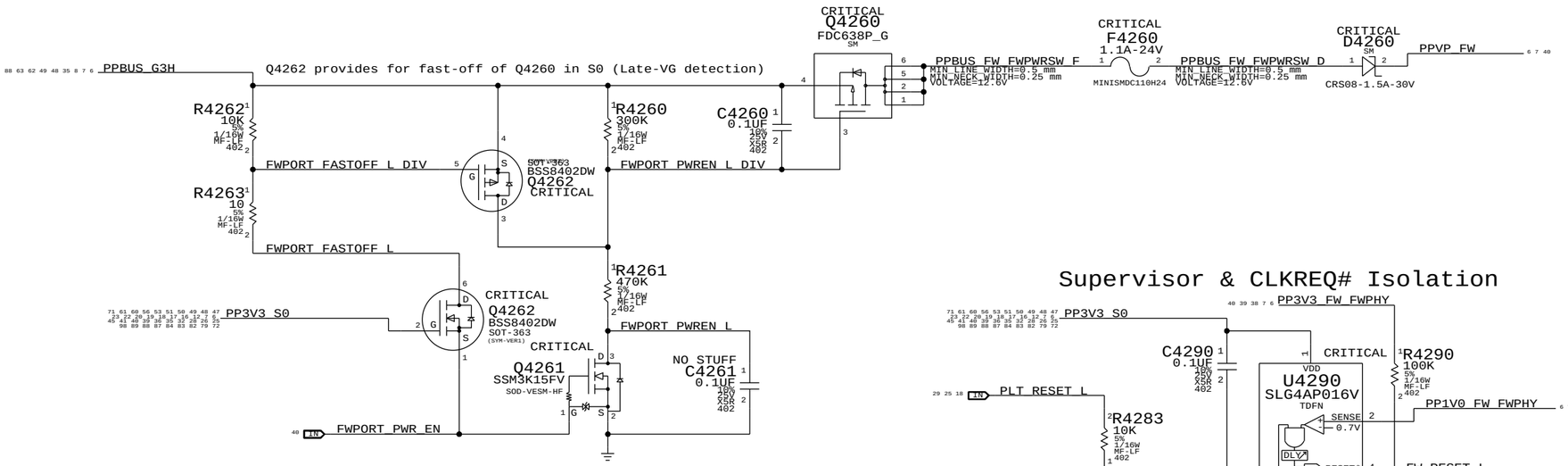
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:
(NONE)

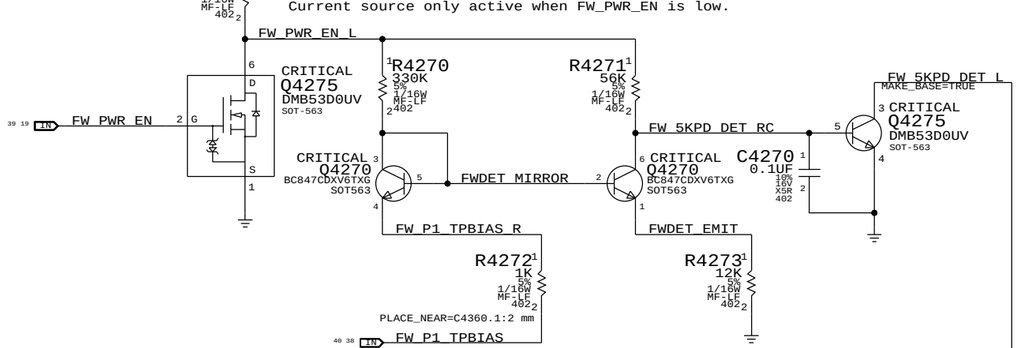
FireWire Port Power Switch



Supervisor & CLKREQ# Isolation

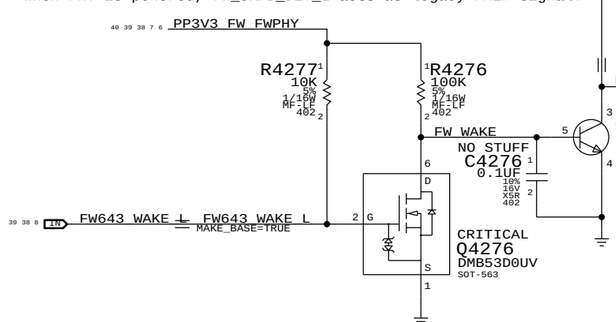
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.



FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

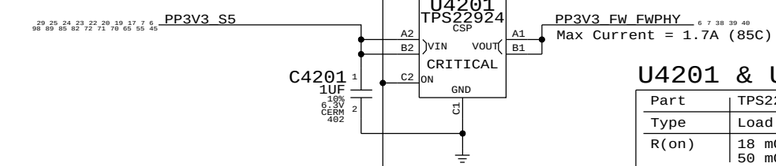


Dual-purpose output:

1) 5K Pull-down Detect when FW_PWR_EN is low.
2) FW643 WAKE# (PME#) when PHY is powered.

FW_PLUG_DET_L
Pull-up provided on another page.

3.3V FW Switch

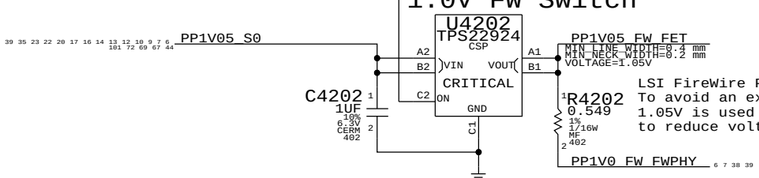


U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



LSI FireWire PHY requires 1.0V.
To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.

SYNC_MASTER=T27_REF SYNC_DATE=06/10/2010

PAGE TITLE
FireWire Port & PHY Power

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

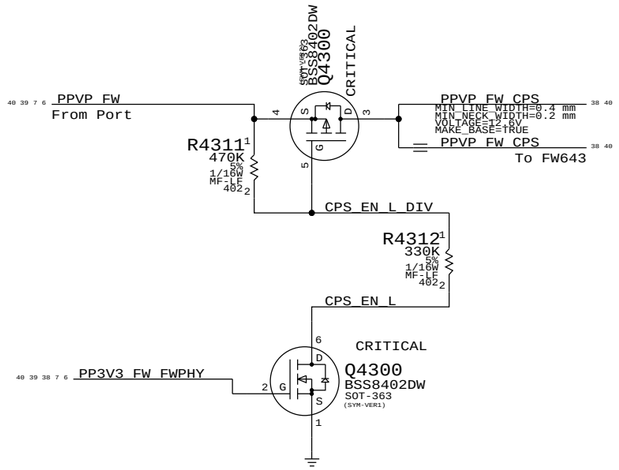
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

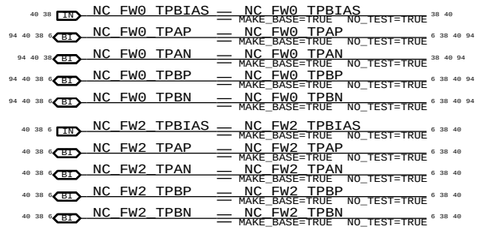
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



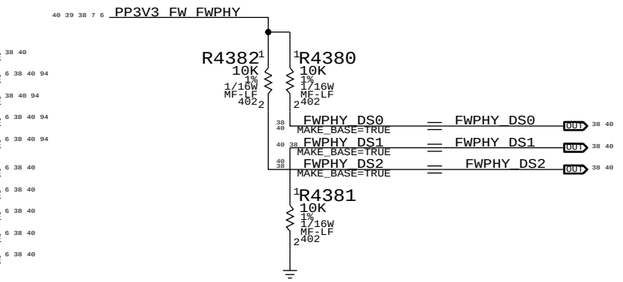
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



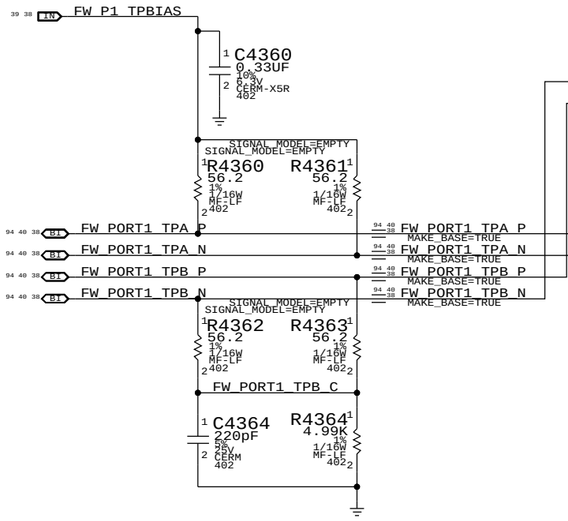
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

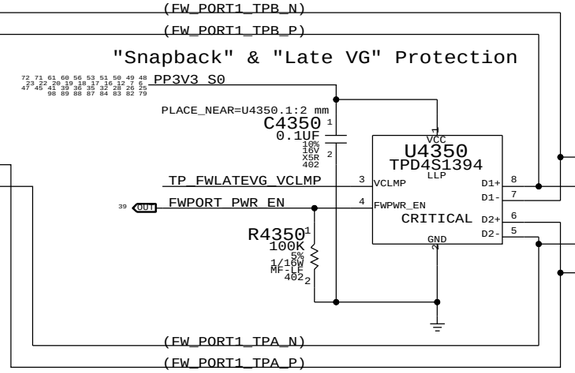


Termination

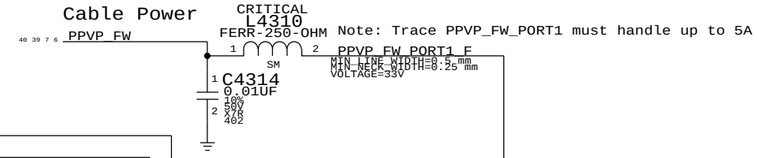
Place close to FireWire PHY



"Snapback" & "Late VG" Protection



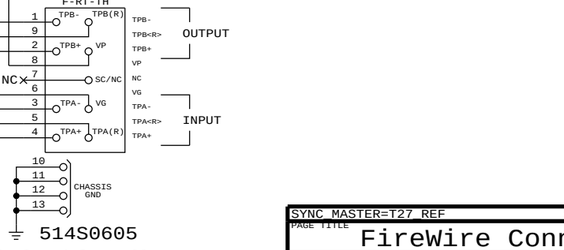
Cable Power

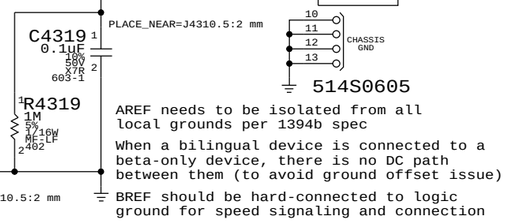


Note: Trace PPVP_FW_PORT1 must handle up to 5A

PORT 1

BILINGUAL





AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

SYNC_MASTER=T27_REF	SYNC_DATE=06/10/2010
PAGE TITLE	FireWire Connector
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ODD Power Control

PP5V_S3

R4596 100K 5% 1/16W MF-LF 402

C4595 0.068UF 10% 16V CERM 402

CRITICAL Q4590 TPCP8102 23V1K-SM

PP5V_SW_ODD_R

C4596 0.01UF 10% 16V CERM 402

NOTE: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.

ODD_PWR_EN_LS5V_L

R4595 100K 5% 1/10W MF-LF 402

ODD_PWR_SS

PP3V3_S0

R4597 100K 5% 1/16W MF-LF 402

CRITICAL Q4596 SSM6N15FEAPE SOT563

ODD_PWR_EN

CRITICAL Q4596 SSM6N15FEAPE SOT563

ODD_PWR_EN_L

XW4598 SM

PP5V_SW_ODD_R — MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.4mm VOLTAGE=5V

PP5V_SW_ODD — MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.4mm VOLTAGE=5V

SATA ODD Connector

CRITICAL J4500 54722-0164 F-ST-SM

516S0616

PP5V_SW_ODD

PP3V3_S0

R4590 33K 5% 1/16W MF-LF 402

SMC_ODD_DETECT

Indicates disc presence

SATA_ODD_R2D_P

SATA_ODD_R2D_N

SATA_ODD_D2R_UF_N

SATA_ODD_D2R_UF_P

CRITICAL FL4520 90-OHM-100MA DLP11S

SATA_ODD_R2D_UF_P — C4521 0.01UF — SATA_ODD_R2D_C_P

SATA_ODD_R2D_UF_N — C4520 0.01UF — SATA_ODD_R2D_C_N

CRITICAL FL4525 90-OHM-100MA DLP11S

SATA_ODD_D2R_C_N — C4526 0.01UF — SATA_ODD_D2R_N

SATA_ODD_D2R_C_P — C4525 0.01UF — SATA_ODD_D2R_P

SATA HDD / IR / SIL Connector

PP5V_S3

R4532 0 5% 1/16W MF-LF 402

PP5V_S3_IR_R — MIN_LINE_WIDTH=0.5mm MIN_NECK_WIDTH=0.2mm VOLTAGE=5V

C4532 0.1UF 10% 16V X7R-CERM 402

PP5V_S0_HDD_FLT — MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.4mm VOLTAGE=5V

CRITICAL L4500 FERR-70-OHM-4A 0603

C4501 0.1UF 20% 10V CERM 402

C4502 0.1UF 20% 10V CERM 402

PP5V_S0_HDD_R — MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.4mm VOLTAGE=5V

XW4599 SM

PP5V_S0

CRITICAL J4501 54722-0224 F-ST-SM

516S0687

IR_RX_OUT

SYS_LED_ANODE_R

R4531 4.7 5% 1/16W MF-LF 402

SYS_LED_ANODE

C4531 0.001UF 10% 50V CERM 402

GND_VOID=TRUE

PP1V5_S0

NO STUFF R4510 4.7K 5% 1/16W MF-LF 402

C4514 0.1UF 20% 10V CERM 402

C4519 0.01UF 20% 10V CERM 402

PLACE_NEAR=U4510.16:2 mm

PLACE_NEAR=U4510.6:2 mm

U4510 PS8521A TQFN CRITICAL

338S0907

SATA_HDD_D2R_C_P — C4516 0.01UF — SATA_HDD_D2R_RDRVR_IN_P

SATA_HDD_D2R_C_N — C4515 0.01UF — SATA_HDD_D2R_RDRVR_IN_N

SATA_HDD_D2R_RDRVR_OUT_P

SATA_HDD_D2R_RDRVR_OUT_N

SATARDRVR_EN

SATARDRVR_I2C_ADDR0

SATARDRVR_I2C_ADDR1

SATARDRVR_I2C_EN_L

SATARDRVR_TEST

SATARDRVR_REXT

R4511 0 5% 1/16W MF-LF 402

R4512 4.99K 1% 1/16W MF-LF 402

SATA_HDD_D2R_RDRVR_OUT_P — C4518 0.01UF — SATA_HDD_D2R_P

SATA_HDD_D2R_RDRVR_OUT_N — C4517 0.01UF — SATA_HDD_D2R_N

SATA_HDD_R2D_RDRVR_IN_N — C4513 0.01UF — SATA_HDD_R2D_C_N

SATA_HDD_R2D_RDRVR_IN_P — C4512 0.01UF — SATA_HDD_R2D_C_P

GND_VOID=TRUE

SMBUS_PCH_CLK

SMBUS_PCH_DATA

D2R values for 4.5dB de-emphasis

R4536 68.1 1% 1/16W MF-LF 402 — C4536 5PF 0.25PCERM 50V 402

R4535 68.1 1% 1/16W MF-LF 402 — C4535 5PF 0.25PCERM 50V 402

R2D values for 3dB de-emphasis

R4534 41.2 1% 1/16W MF-LF 402 — C4534 15PF 5% 50V CERM 402

R4533 41.2 1% 1/16W MF-LF 402 — C4533 15PF 5% 50V CERM 402

CRITICAL FL4501 12-OHM-100MA-5.5GHZ TCM0806-4SM

SATA_HDD_R2D_UF_N

SATA_HDD_R2D_UF_P

SATA_HDD_R2D_RC_UF_N

SATA_HDD_R2D_RC_UF_P

C4511 0.01UF — GND_VOID=TRUE

C4510 0.01UF — GND_VOID=TRUE

Internally PD ~150K
Write:0xB6 Read:0xB7

ADDR1	ADD0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

SATARDRVR_I2C_ADDR0

SATARDRVR_I2C_ADDR1

SYNC_MASTER=K91_ERIC SYNC_DATE=11/08/2010

PAGE TITLE: SATA/IR/SIL Connectors

Apple Inc.

DRAWING NUMBER — SIZE: D

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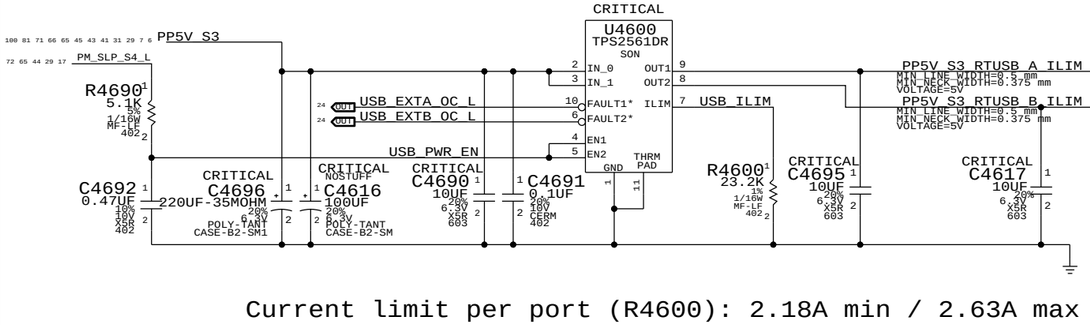
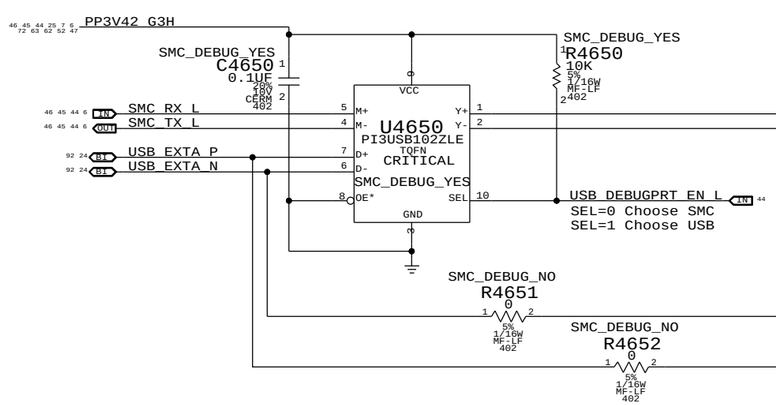
USB Port Power Switch

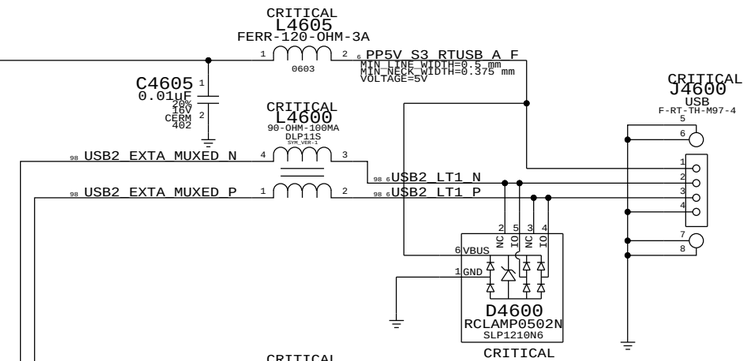


Current limit per port (R4600): 2.18A min / 2.63A max

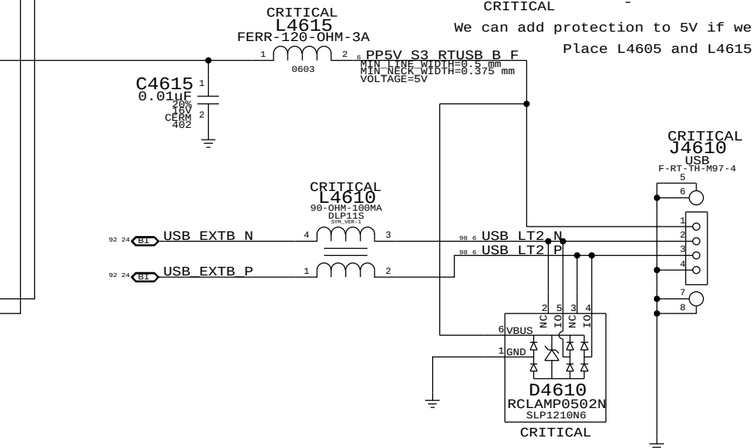
USB/SMC Debug Mux



Left USB Port A



We can add protection to 5V if we want, but leaving NC for now
Place L4605 and L4615 at connector pin



Left USB Port B

SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE: External USB Connectors

Apple Inc.

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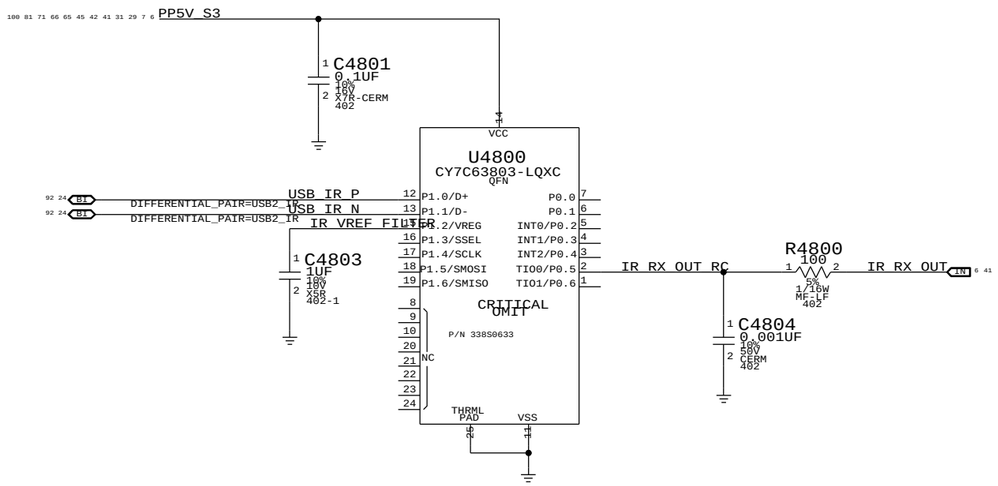
IR SUPPORT



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: Front Flex Support

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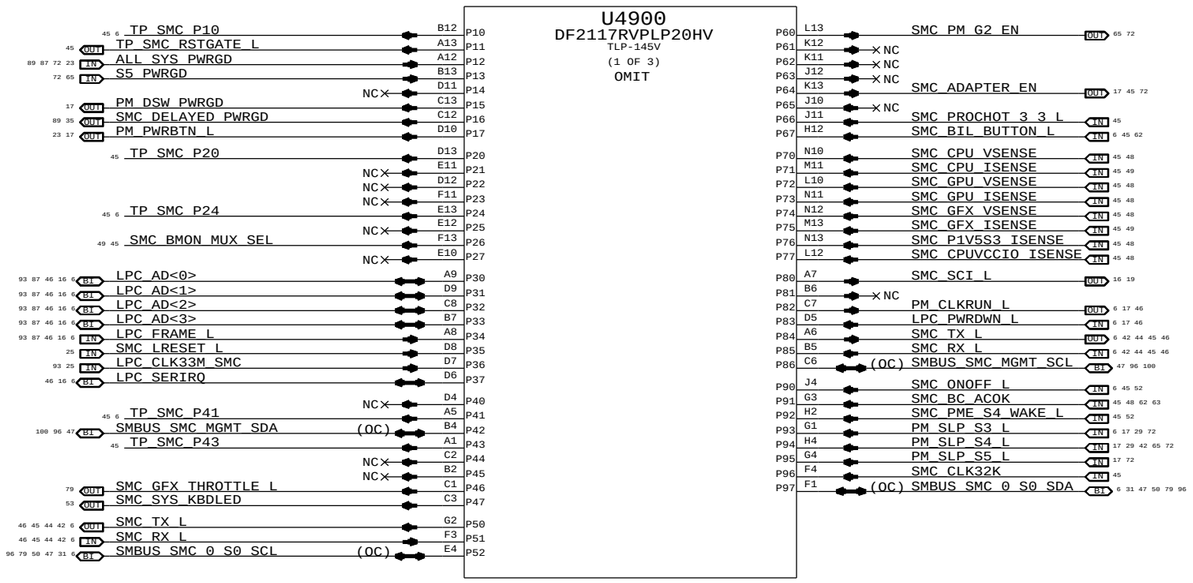
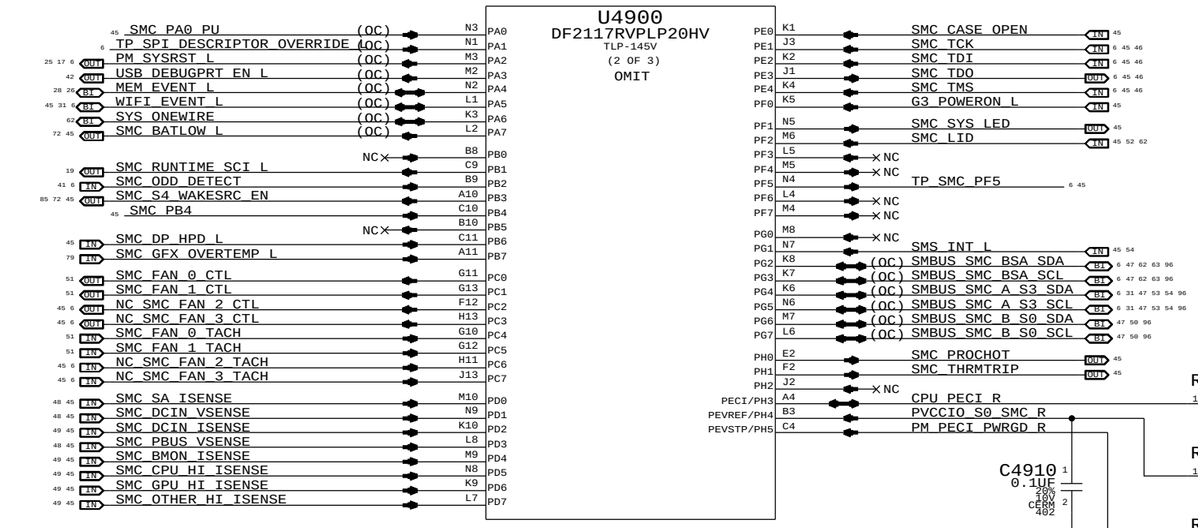
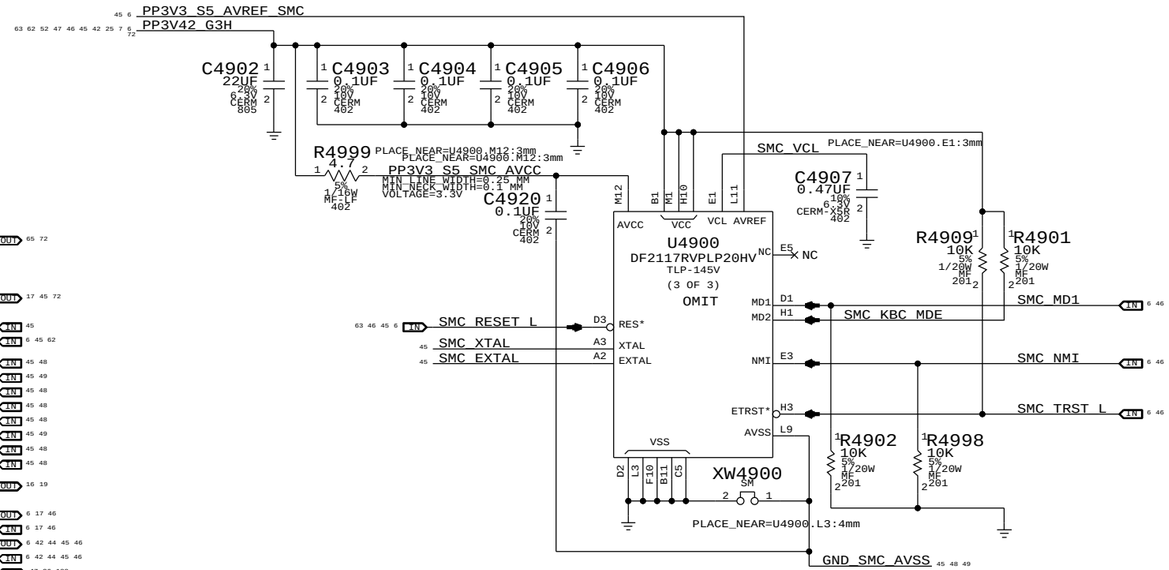
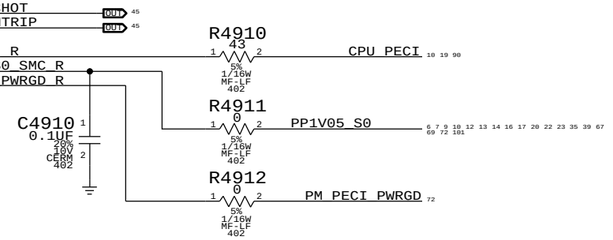
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.







NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SYNC_MASTER=K91_BEN SYNC_DATE=07/12/2010

PAGE TITLE: SMC

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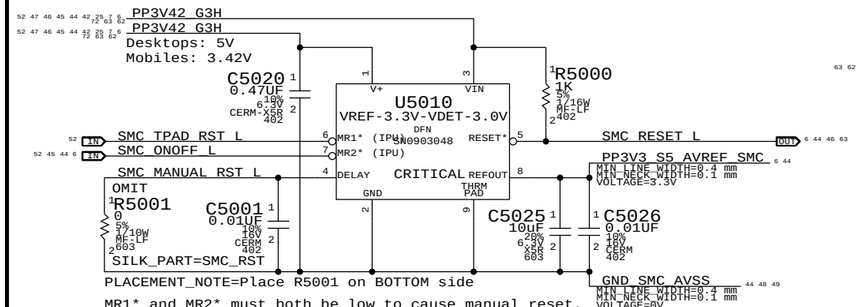
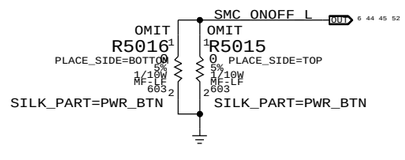
SMC Reset "Button", Supervisor & AVREF Supply



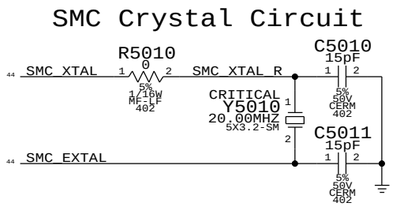
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

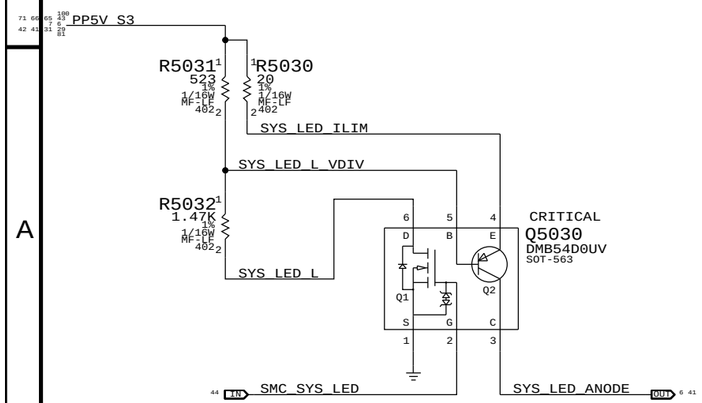
Debug Power "Buttons"



SMC Crystal Circuit

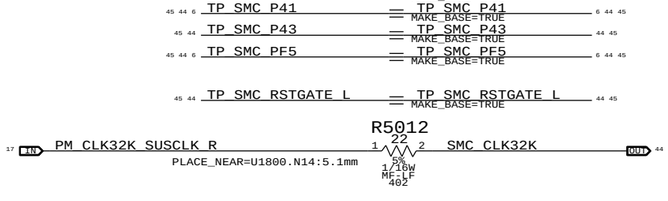


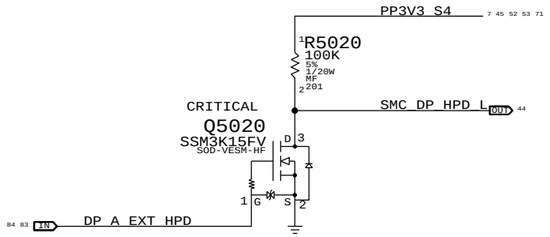
System (Sleep) LED Circuit

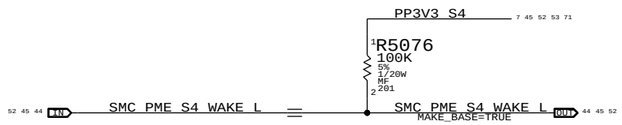


SMC Signal Connections

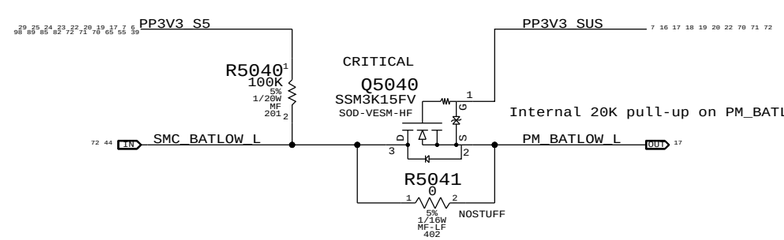
NC_SMC_FAN_2_CTL	= NC_SMC_FAN_2_CTL	MAKE_BASE=TRUE
NC_SMC_FAN_2_TACH	= NC_SMC_FAN_2_TACH	MAKE_BASE=TRUE
NC_SMC_FAN_3_CTL	= NC_SMC_FAN_3_CTL	MAKE_BASE=TRUE
NC_SMC_FAN_3_TACH	= NC_SMC_FAN_3_TACH	MAKE_BASE=TRUE
SMC_BC_ACOK	= SMC_BC_ACOK	MAKE_BASE=TRUE
SMS_INT_L	= SMS_INT_L	MAKE_BASE=TRUE
SMC_CPU_VSENSE	= SMC_CPU_VSENSE	MAKE_BASE=TRUE
SMC_CPU_ISENSE	= SMC_CPU_ISENSE	MAKE_BASE=TRUE
SMC_GPU_VSENSE	= SMC_GPU_VSENSE	MAKE_BASE=TRUE
SMC_GPU_ISENSE	= SMC_GPU_ISENSE	MAKE_BASE=TRUE
SMC_GFX_VSENSE	= SMC_GFX_VSENSE	MAKE_BASE=TRUE
SMC_GFX_ISENSE	= SMC_GFX_ISENSE	MAKE_BASE=TRUE
SMC_P1V5S3_ISENSE	= SMC_P1V5S3_ISENSE	MAKE_BASE=TRUE
SMC_CPUVCCIO_ISENSE	= SMC_CPUVCCIO_ISENSE	MAKE_BASE=TRUE
SMC_SA_ISENSE	= SMC_SA_ISENSE	MAKE_BASE=TRUE
SMC_DCIN_VSENSE	= SMC_DCIN_VSENSE	MAKE_BASE=TRUE
SMC_DCIN_ISENSE	= SMC_DCIN_ISENSE	MAKE_BASE=TRUE
SMC_PBUS_VSENSE	= SMC_PBUS_VSENSE	MAKE_BASE=TRUE
SMC_BMON_ISENSE	= SMC_BMON_ISENSE	MAKE_BASE=TRUE
SMC_CPU_HI_ISENSE	= SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE
SMC_GPU_HI_ISENSE	= SMC_GPU_HI_ISENSE	MAKE_BASE=TRUE
SMC_OTHER_HI_ISENSE	= SMC_OTHER_HI_ISENSE	MAKE_BASE=TRUE
TP_SMC_P10	= TP_SMC_P10	MAKE_BASE=TRUE
TP_SMC_P20	= TP_SMC_P20	MAKE_BASE=TRUE
TP_SMC_P24	= TP_SMC_P24	MAKE_BASE=TRUE
SMC_BMON_MUX_SEL	= SMC_BMON_MUX_SEL	MAKE_BASE=TRUE
TP_SMC_P41	= TP_SMC_P41	MAKE_BASE=TRUE
TP_SMC_P43	= TP_SMC_P43	MAKE_BASE=TRUE
TP_SMC_PF5	= TP_SMC_PF5	MAKE_BASE=TRUE
TP_SMC_RSTGATE_L	= TP_SMC_RSTGATE_L	MAKE_BASE=TRUE



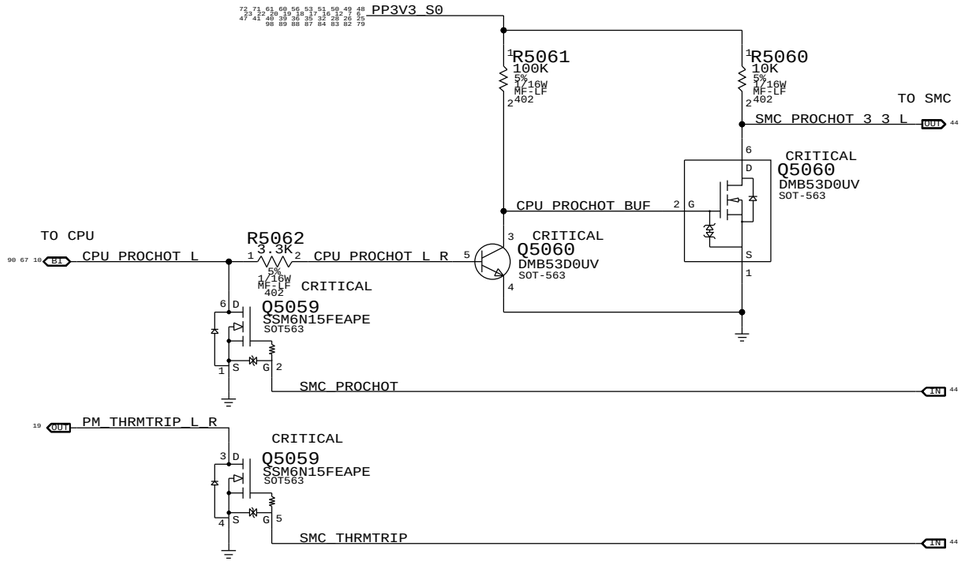


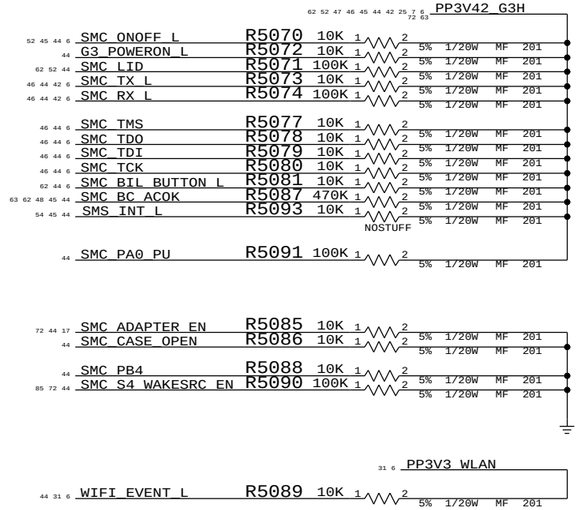


BATLOW# Isolation



SMC FSB to 3.3V Level Shifting





SYNC_MASTER=K91_BEN SYNC_DATE=07/12/2010

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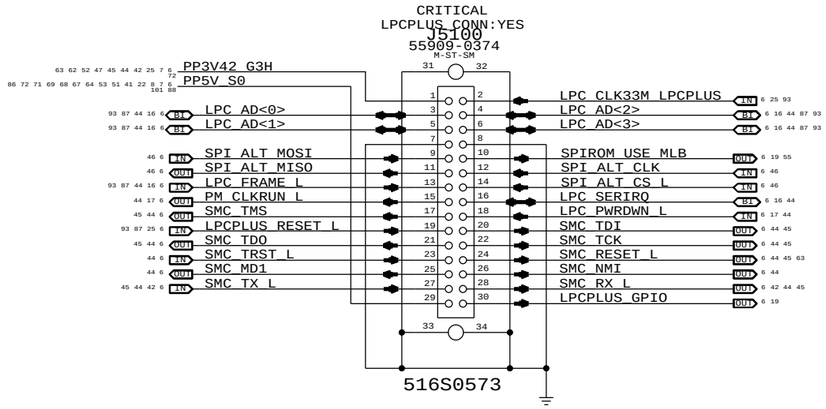
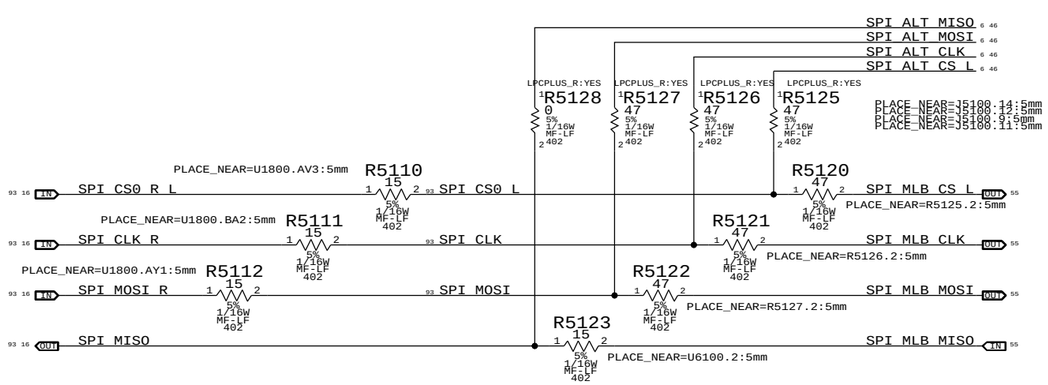
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: LPC+SPI Debug Connector

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PCH SMBus "0" Connections

PP3V3_S0

Cougar Point
U1800
(MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA
MAKE_BASE=TRUE

R5200 1K 5% 1/16W MF-LF 402
R5201 1K 5% 1/16W MF-LF 402

SO-DIMM "A"
J2900
(Write: 0xA0 Read: 0xA1)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

VRef DACs
U3300
(Write: 0x98 Read: 0x99)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SO-DIMM "B"
J3100
(Write: 0xA4 Read: 0xA5)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Margin Control
U3301
(Write: 0x30 Read: 0x31)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SATA Redriver
U4510
(Write: 0xB6 Read: 0xB7)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

LED BACKLIGHT
U9701
(WRITE: 0x58 READ: 0x59)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

XDP Connectors
J2500 & J2550
(MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Mikey
U6880
(Write: 0x72 Read: 0x73)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SDRVI2C:SB
R5237 0 5% 1/16W MF-LF 402

SDRVI2C:SB
R5236 0 5% 1/16W MF-LF 402

DP SDRV "A"
U9310
(Write: 0x94 Read: 0x95)
- I2C_DPSDRVA_SCL
- I2C_DPSDRVA_SDA
MAKE_BASE=TRUE

PCH "SMLink 0" Connections

PP3V3_S0

Cougar Point
U1800
(MASTER)
- SML_PCH_0_CLK
- SML_PCH_0_DATA
MAKE_BASE=TRUE

R5210 8.2K 5% 1/16W MF-LF 402
R5211 8.2K 5% 1/16W MF-LF 402

PCH "SMLink 1" Connections

PP3V3_S0

Cougar Point
U1800
(Write: 0x88 Read: 0x89)
- SML_PCH_1_CLK
- SML_PCH_1_DATA
MAKE_BASE=TRUE

NO STUFF
R5220 8.2K 5% 1/16W MF-LF 402

NO STUFF
R5221 8.2K 5% 1/16W MF-LF 402

R5223 0 5% 1/16W MF-LF 402

R5222 0 5% 1/16W MF-LF 402

SMLink 1 is slave port to
access PCH & CPU via PECI.

SMC "0" SMBus Connections

PP3V3_S0

SMC
U4900
(MASTER)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA
MAKE_BASE=TRUE

R5250 4.7K 5% 1/16W MF-LF 402
R5251 4.7K 5% 1/16W MF-LF 402

GPU Temp (Ext)
EMC1414-A: U5550
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

GPU Temp (Int)
Whistler: U8000
(Write: 0x82 Read: 0x83)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

X19
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

PP3V3_S3

SMC
U4900
(MASTER)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA
MAKE_BASE=TRUE

R5270 1K 5% 1/16W MF-LF 402
R5271 1K 5% 1/16W MF-LF 402

Trackpad
J5800
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

J3401
ALS
(Write: 0x72 Read: 0x73)
Lid Angle Detect
(Write: 0x32 Read: 0x33)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

Digital SMS
LIS331DLH: U5920
(Write: 0x30 Read: 0x31)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

SMC "B" SMBus Connections

PP3V3_S0

SMC
U4900
(MASTER)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA
MAKE_BASE=TRUE

R5260 4.7K 5% 1/16W MF-LF 402
R5261 4.7K 5% 1/16W MF-LF 402

CPU Temp
EMC1414-A: U5570
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

T29 Temp
EMC1412-A: U5520
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

SMC "Battery A" SMBus Connections

PP3V42_G3H

SMC
U4900
(MASTER)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA
MAKE_BASE=TRUE

R5280 2.0K 5% 1/16W MF-LF 402
R5281 2.0K 5% 1/16W MF-LF 402

Battery Charger
ISL6258 - U7000
(Write: 0x12 Read: 0x13)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery
J6955
(See Table)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery
Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x92 Read: 0x93)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

PP3V3_S3

SMC
U4900
(MASTER)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA
MAKE_BASE=TRUE

R5290 4.7K 5% 1/16W MF-LF 402
R5291 4.7K 5% 1/16W MF-LF 402

Sensor ADC A
U5930
(Write: 0x10 Read: 0x11)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA

T29 SMBus Connections

PP3V3_S0

T29 IC
U3600
(MASTER)
- I2C_T29_SCL
- I2C_T29_SDA
MAKE_BASE=TRUE

R5230 4.7K 5% 1/16W MF-LF 402
R5231 4.7K 5% 1/16W MF-LF 402

T29 Port A MCU
J9330
(Write: 0x26 Read: 0x27)
- I2C_T29_SCL
- I2C_T29_SDA

SDRVI2C:MCU
R5234 0 5% 1/16W MF-LF 402

SDRVI2C:MCU
R5235 0 5% 1/16W MF-LF 402

DP SDRV "A"
U9310
(Write: 0x94 Read: 0x95)
- I2C_DPSDRVA_SCL
- I2C_DPSDRVA_SDA
MAKE_BASE=TRUE

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

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SMBus Connections

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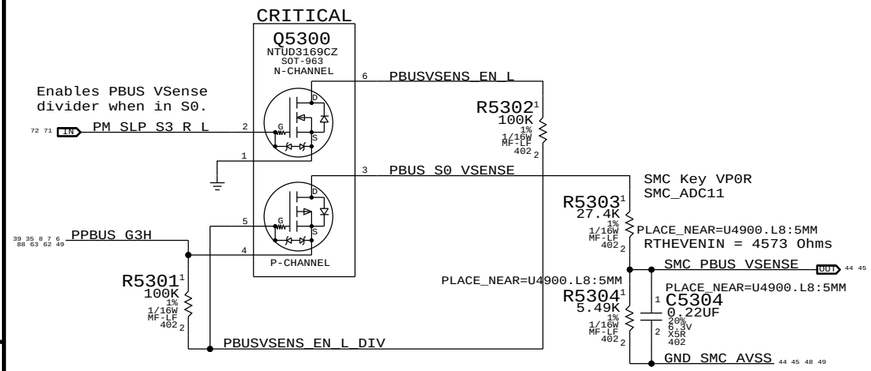
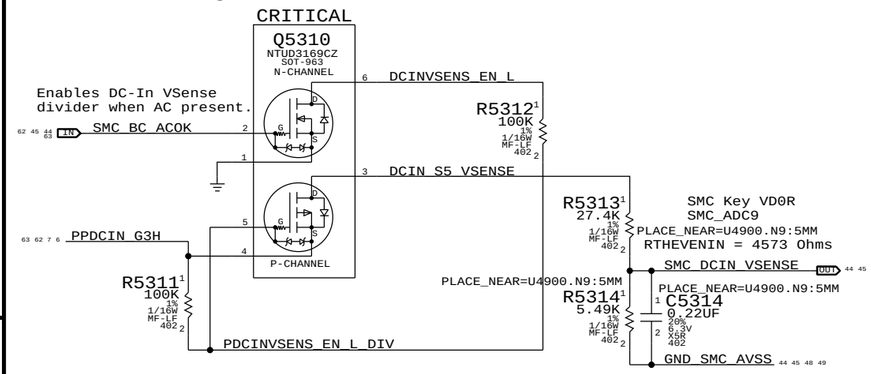
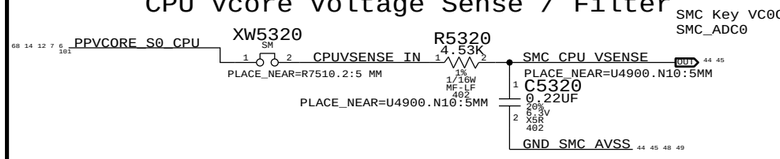
PBUS Voltage Sense Enable & Filter



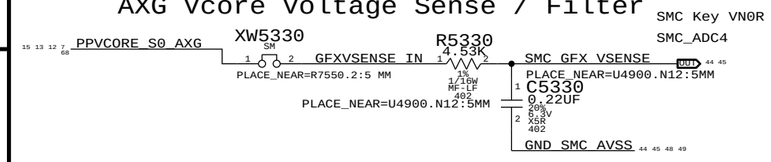
DC-In Voltage Sense Enable & Filter



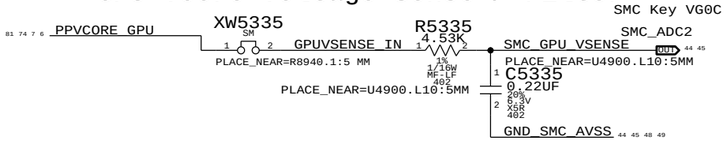
CPU Vcore Voltage Sense / Filter



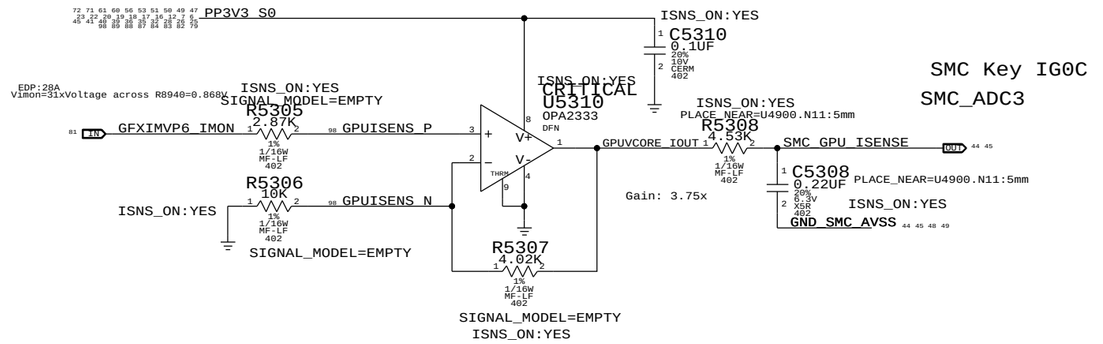
AXG Vcore Voltage Sense / Filter



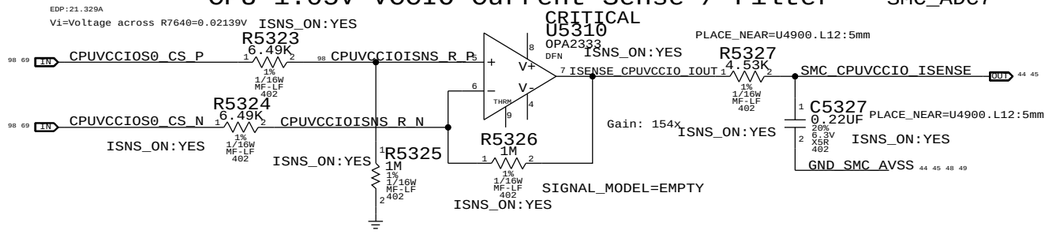
GPU Vcore Voltage Sense / Filter



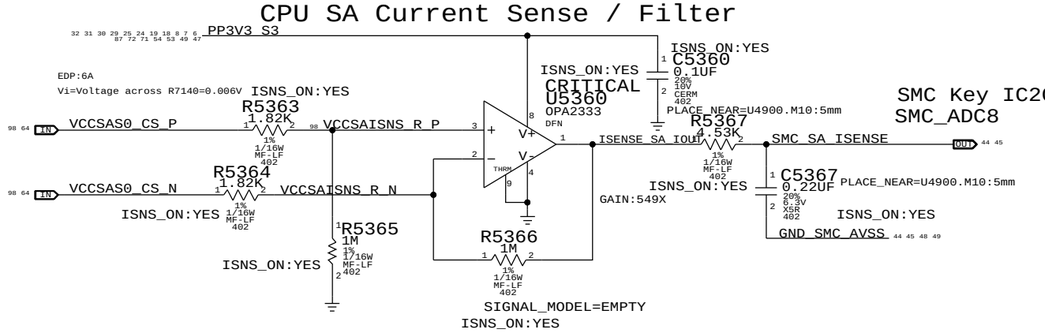
GPU VCore Load Side Current Sense / Filter



CPU 1.05V VCCIO Current Sense / Filter

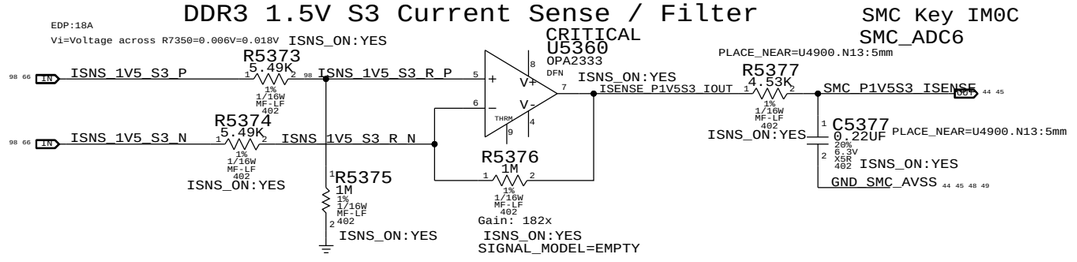


CPU SA Current Sense / Filter



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0090	4	RES, 00HM, 0402	C5308,C5327,C5367,C5377		ISNS_ON:NO

DDR3 1.5V S3 Current Sense / Filter



SYNC_MASTER=K91_DINESH SYNC_DATE=08/16/2010

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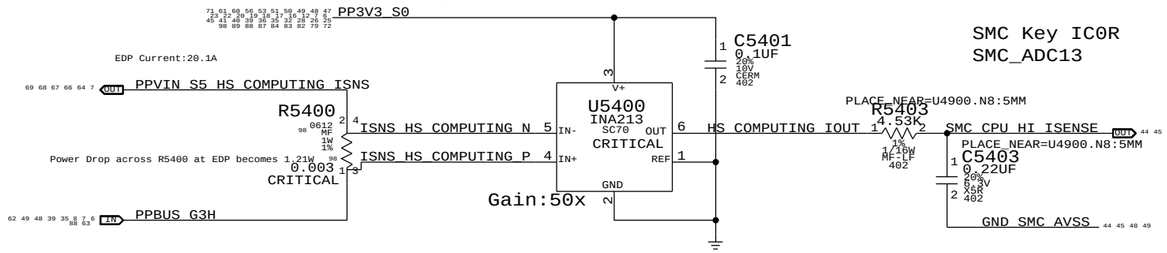
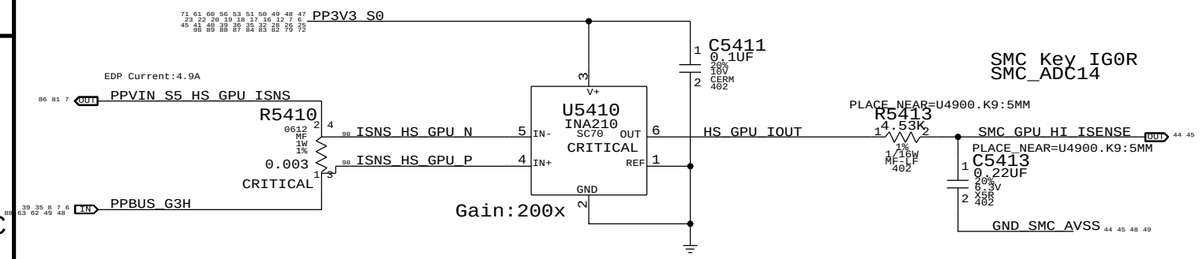
COMPUTING High Side Current Sense / Filter



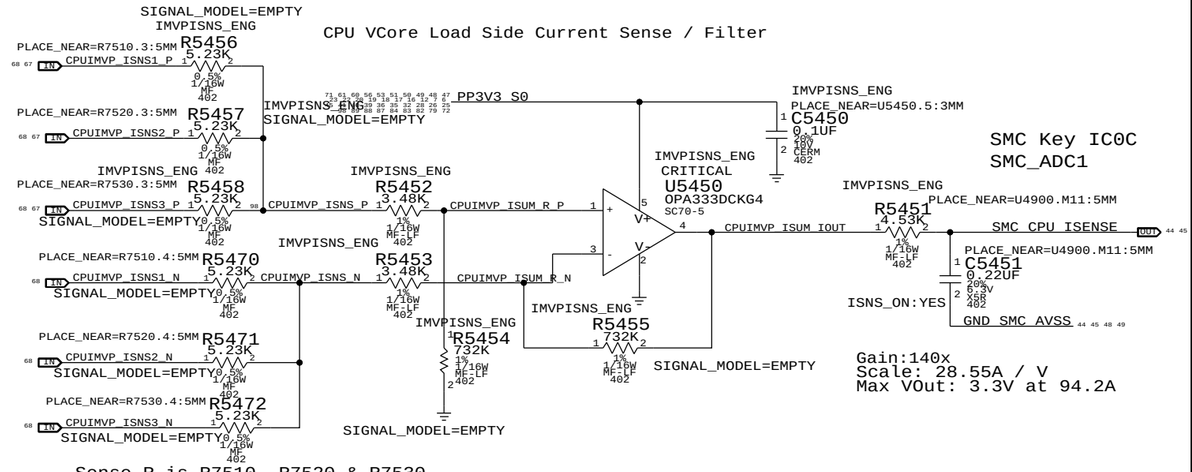
SMC Key IC0R
SMC_ADC13

GRAPHICS High Side Current Sense / Filter



SMC Key IG0R
SMC_ADC14

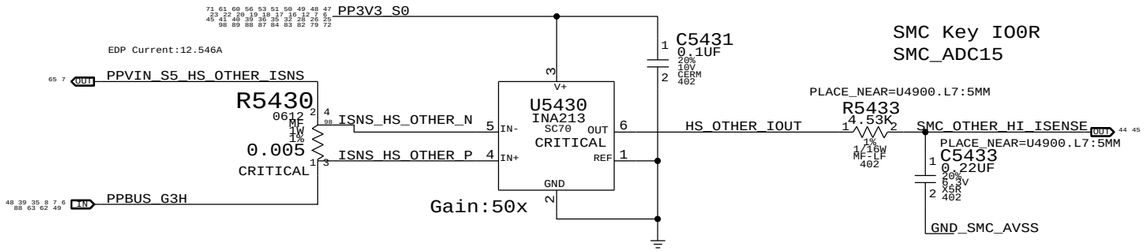
CPU VCore Load Side Current Sense / Filter



SMC Key IC0C
SMC_ADC1

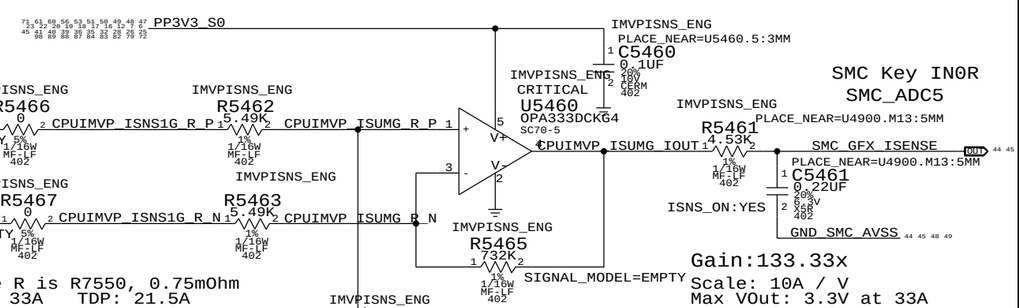
Sense R is R7510, R7520 & R7530
Individual Sense R is 0.75mOhm
EDP: 94A TDP :45A
(Effective Sense R is 0.25mOhm due to summing of the 3 phases)

OTHER High Side Current Sense / Filter



SMC Key IO0R
SMC_ADC15

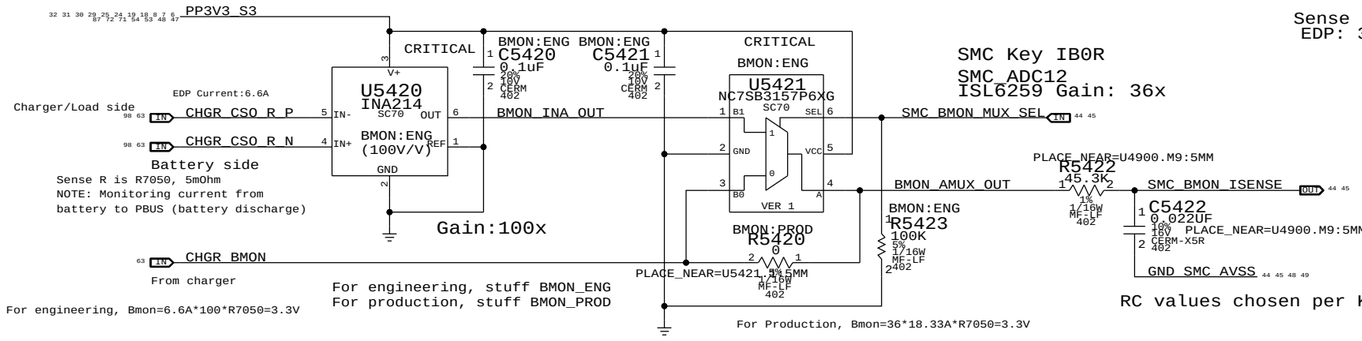
GFX/IG VCore Load Side Current Sense / Filter



SMC Key IN0R
SMC_ADC5

Sense R is R7550, 0.75mOhm
EDP: 33A TDP: 21.5A

CHARGER BMON High Side (BATTERY DISCHARGE) Current Sense, MUX & Filter

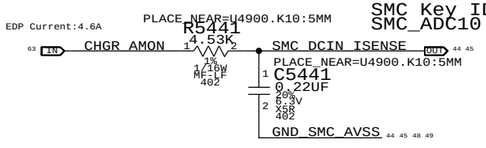


SMC Key IB0R
SMC_ADC12
ISL6259 Gain: 36x

RC values chosen per K17 Radar 7337775

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0090	2	RES, 0OHM, 0402	C5451,C5461		ISNS_ON:NO

DC-IN (AMON) Current Sense Filter



SMC Key ID0R
SMC_ADC10

SYNC_MASTER=K91_DINESH SYNC_DATE=10/29/2016

PAGE TITLE: High Side and CPU/AXG Current Sensing

Apple Inc.

DRAWING NUMBER: D | SIZE

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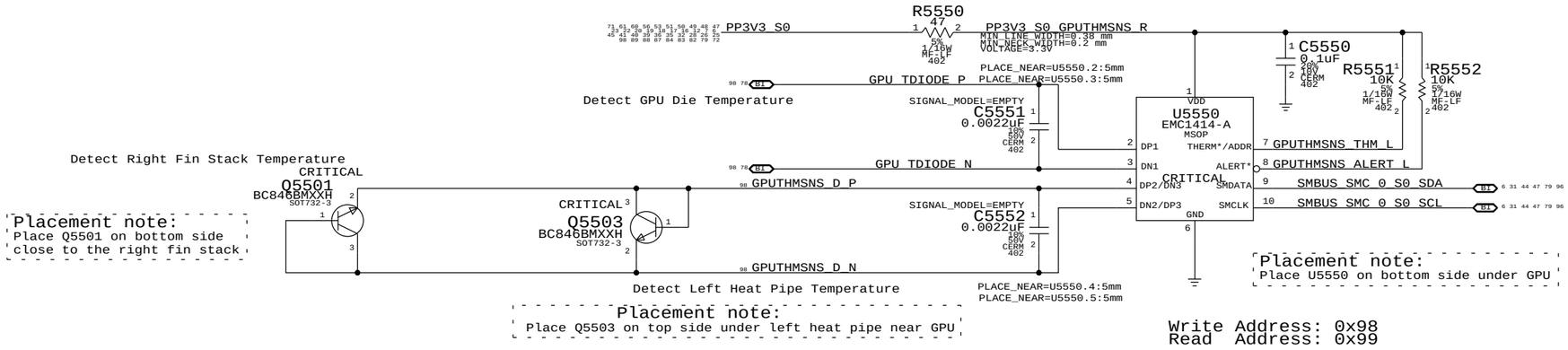
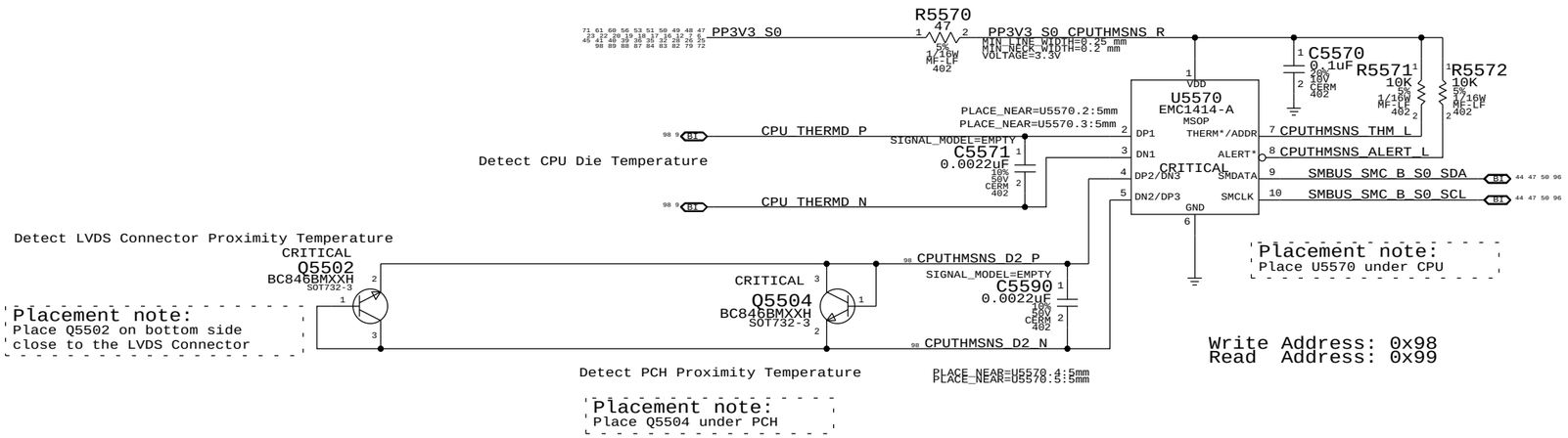
GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack

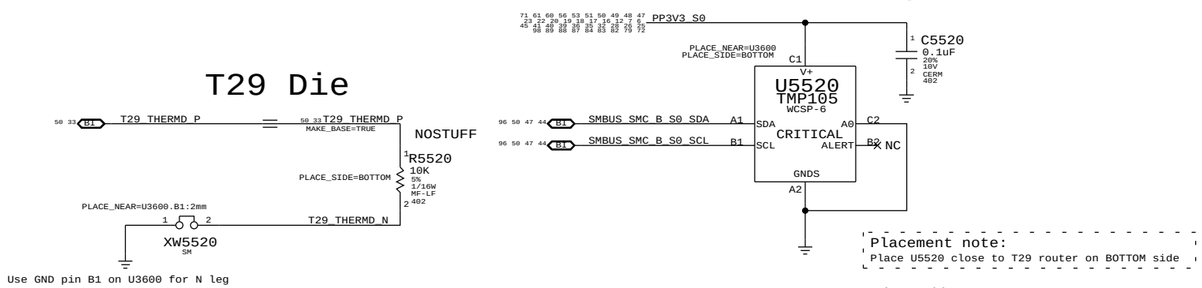


CPU Proximity/CPU Die/PCH Proximity/LVDS Connector Proximity



Note: EMC1414 can perform Beta
Compensation for External Diode 1 only

T29 Proximity



SYNC_MASTER=K91_DINESH SYNC_DATE=09/22/2010

PAGE TITLE
Thermal Sensors

Apple Inc.

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SIZE D

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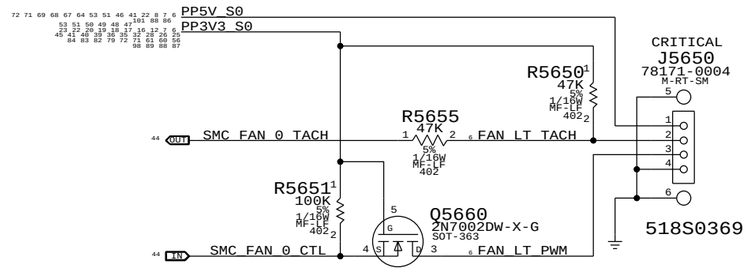
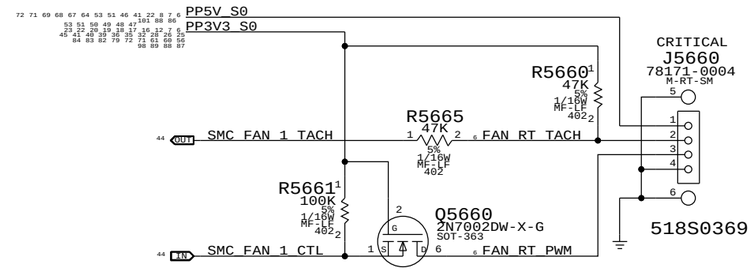
Left Fan



Right Fan



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: Fan Connectors

Apple Inc.

DRAWING NUMBER | SIZE: D

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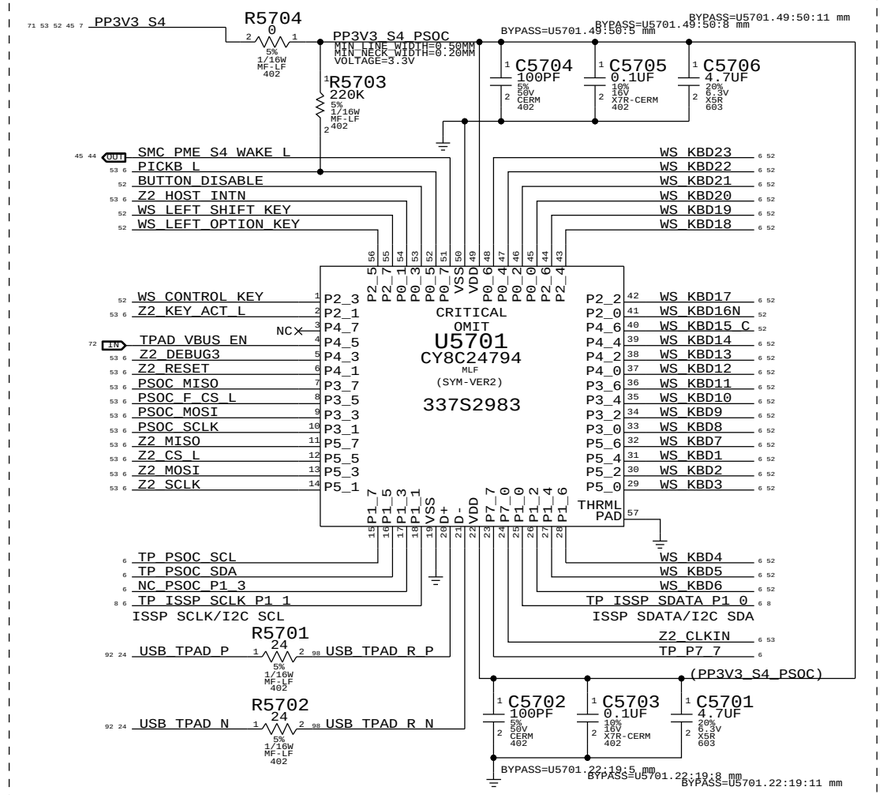
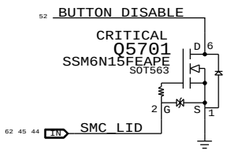
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



TPAD Buttons Disable

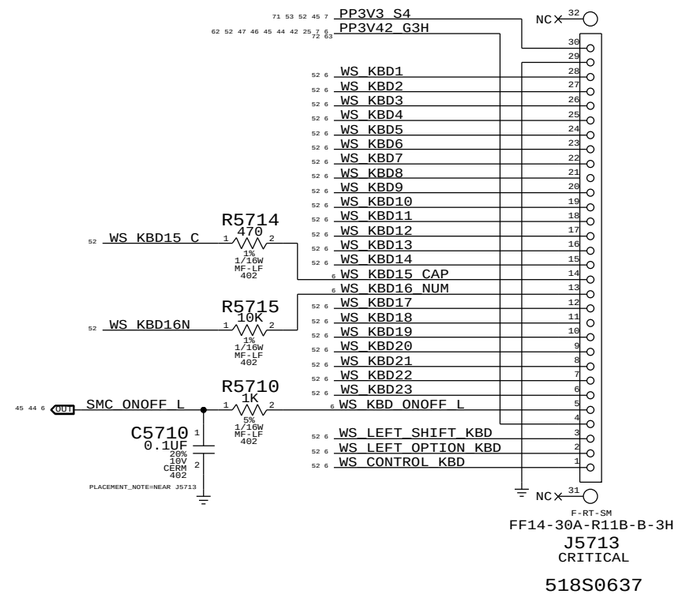


PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

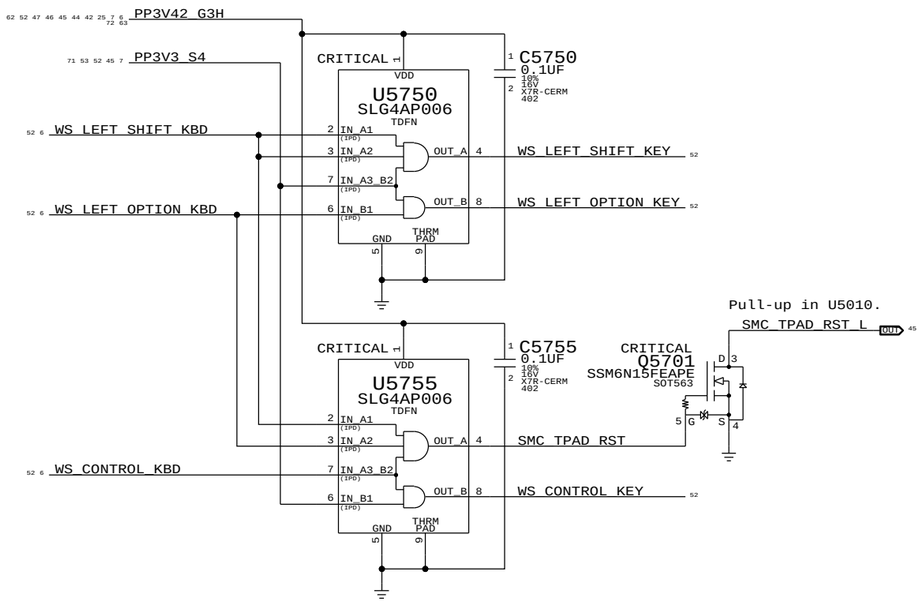
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector



SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.



SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE: WELLSPRING 1

Apple Inc.

DRAWING NUMBER | SIZE: D

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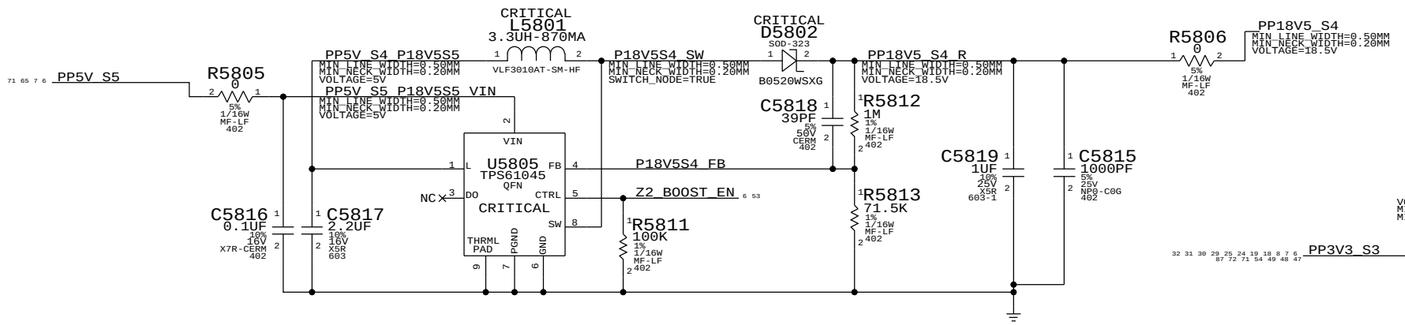
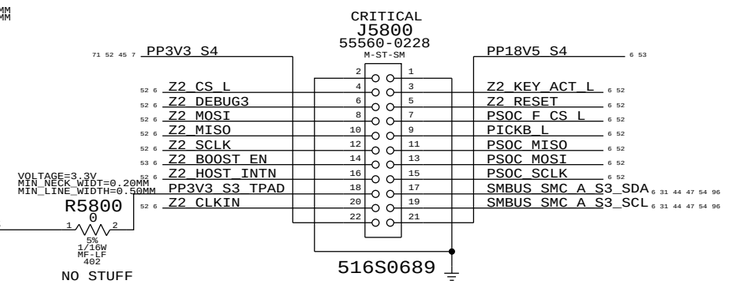
BOOSTER +18.5VDC FOR SENSORS

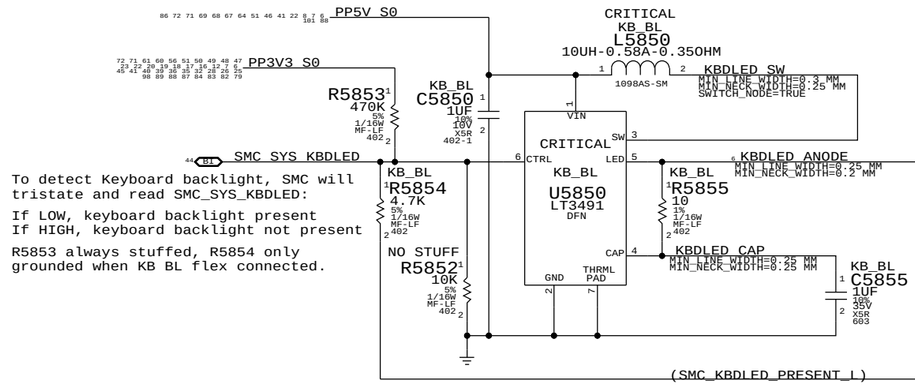
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector



Keyboard Backlight Driver & Detection

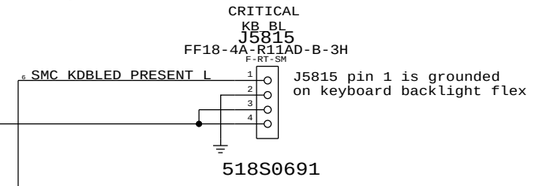


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



SYNC_MASTER=K91_ERIC SYNC_DATE=07/14/2010

PAGE TITLE: WELLSPRING 2

Apple Inc.

DRAWING NUMBER | SIZE: D

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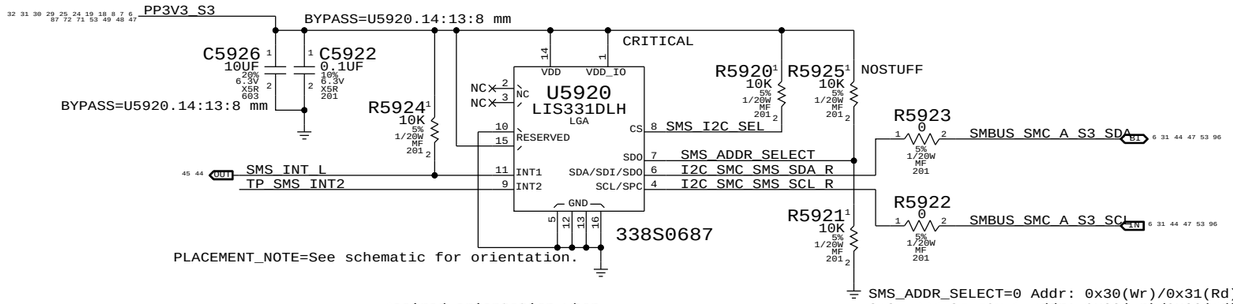

SYNC_MASTER=K91_DINESH SYNC_DATE=08/06/2010

PAGE TITLE
Digital Accelerometer

Apple Inc.

DRAWING NUMBER | SIZE D

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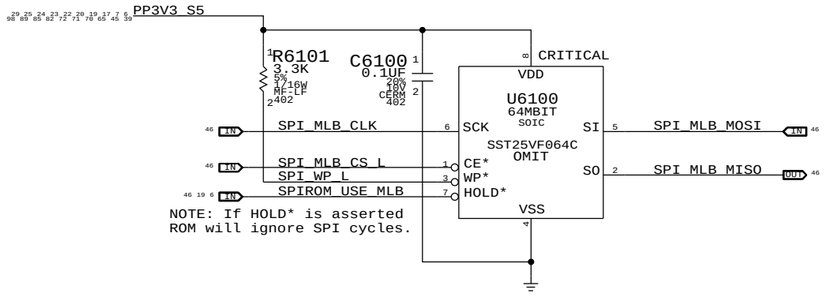

SYNC_MASTER=K91_BEN SYNC_DATE=06/08/2010

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER

SIZE D

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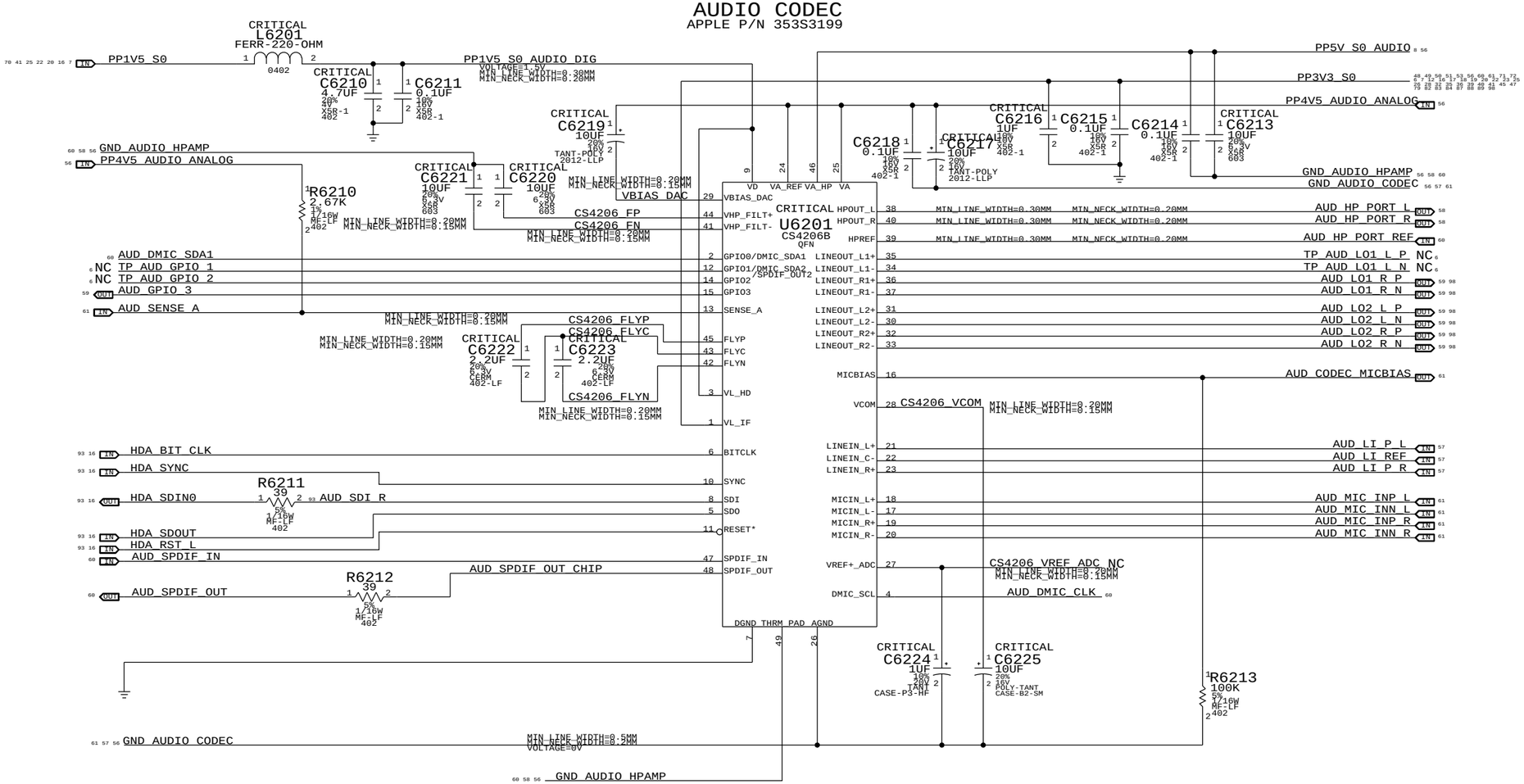
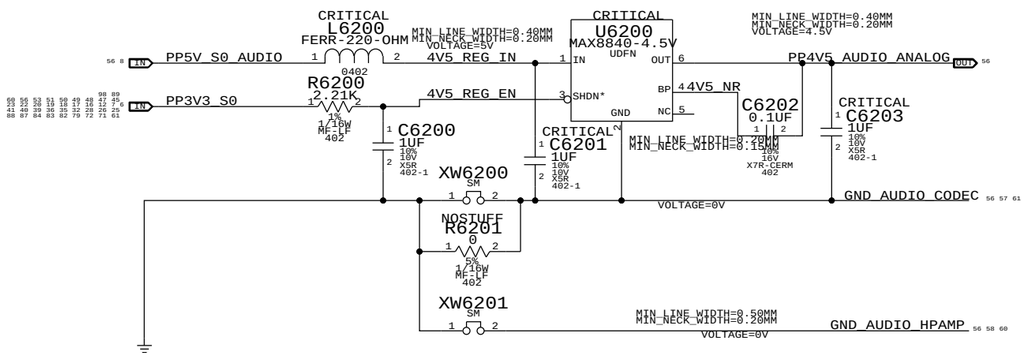
AUDIO CODEC
APPLE P/N 353S3199



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2234



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=K91_AUDIO SYNC_DATE=09/30/2010

PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

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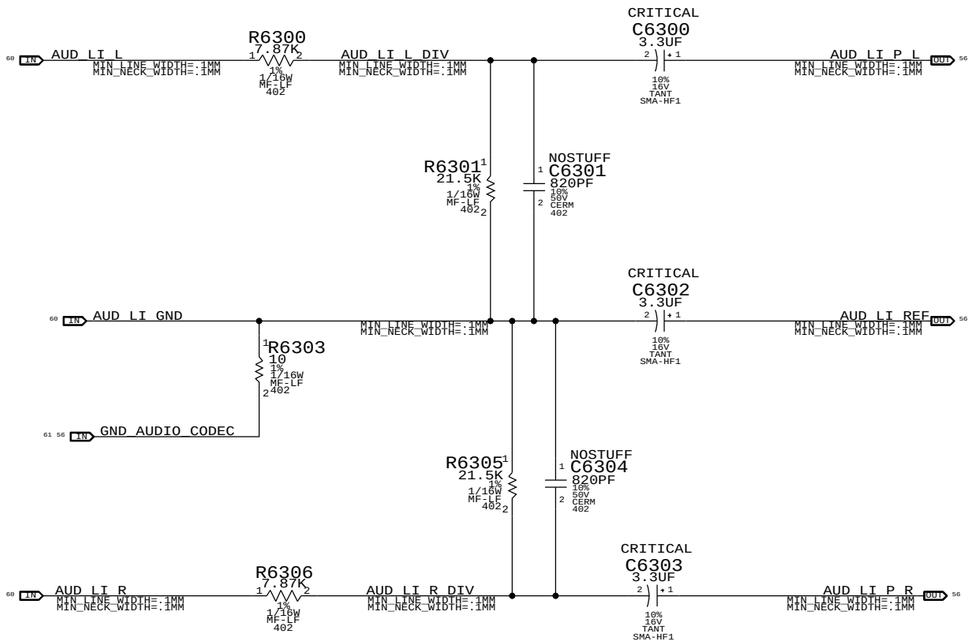
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 18K OHMS
FC = 8 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



SYNC_MASTER=K91_AUDIO SYNC_DATE=07/12/2010

PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

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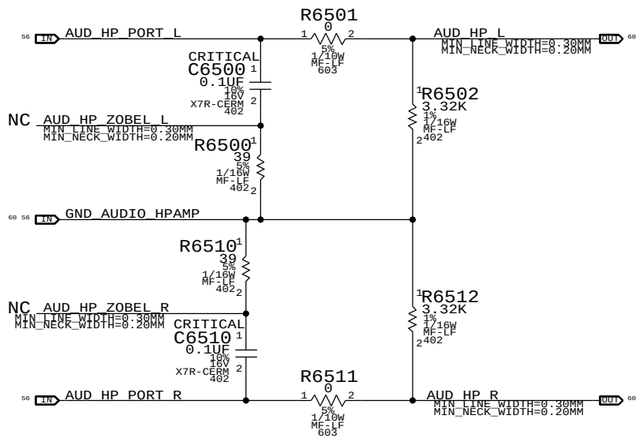
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=K91_AUDIO SYNC_DATE=07/12/2010

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

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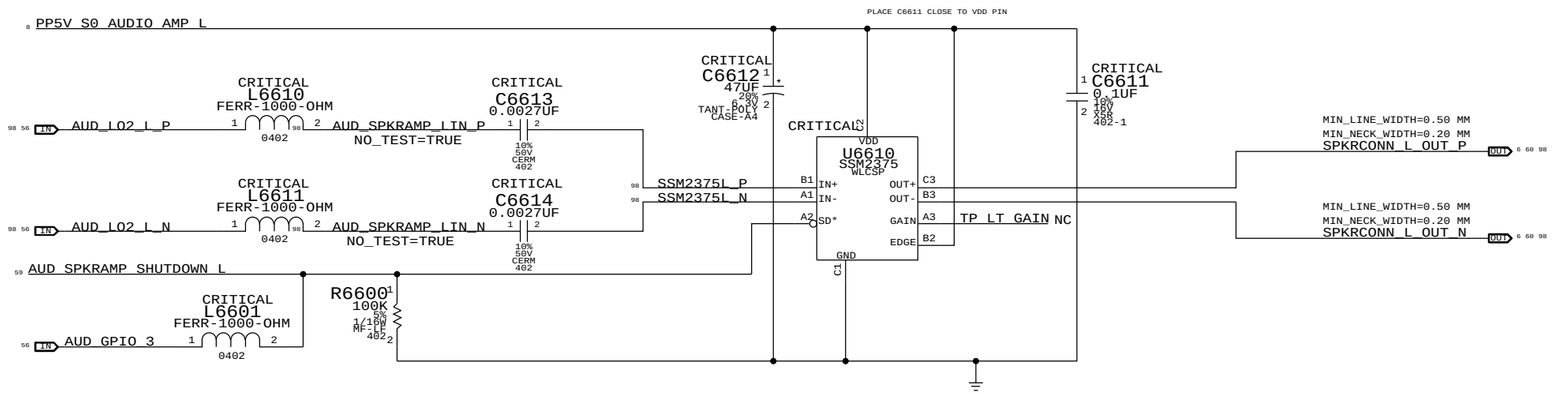
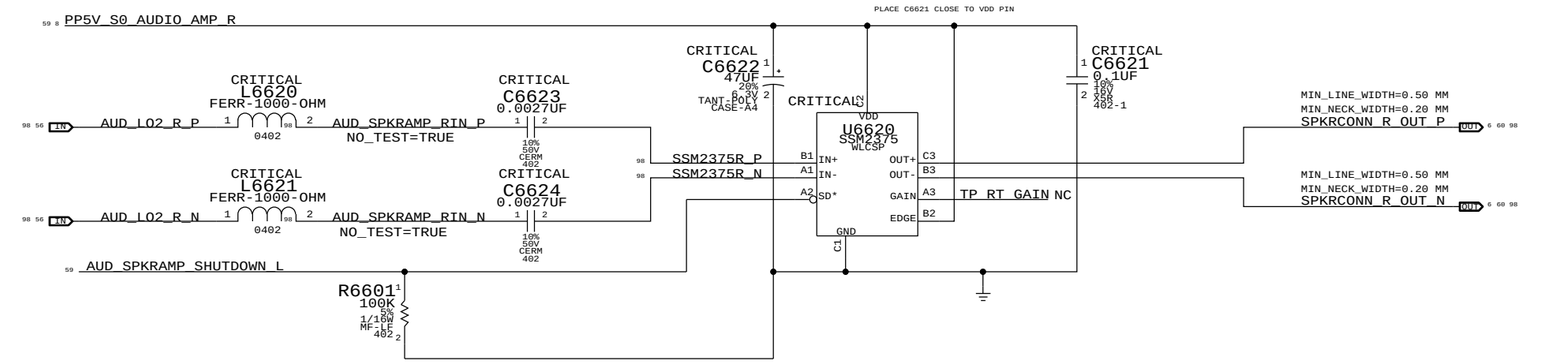
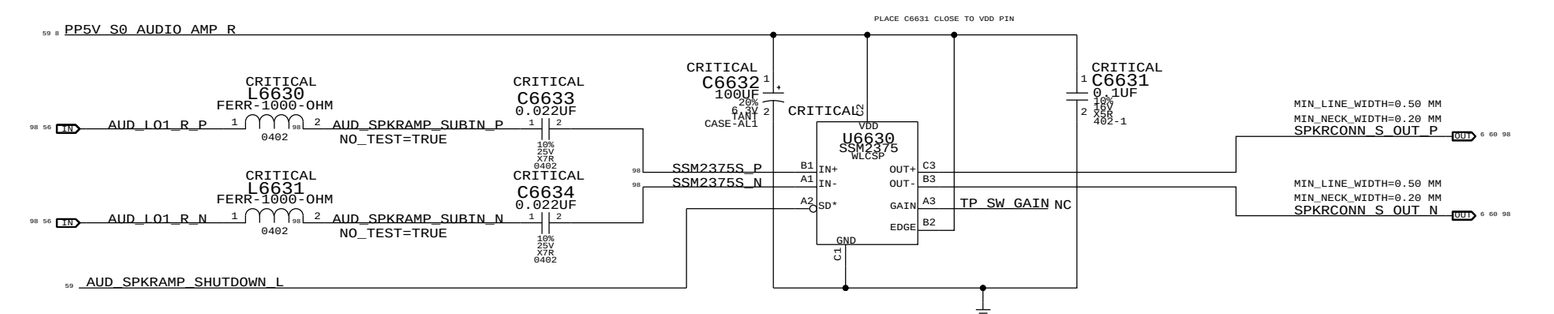
3X MONO SPEAKER AMPLIFIERS (SSM2375)
APN: 353S2958

GAIN = +3 DB
1ST ORDER FC (L&R) = ~737 HZ
1ST ORDER FC (SUB) = ~90 HZ







SYNC_MASTER=K91_AUDIO SYNC_DATE=07/12/2010

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER
SIZE D
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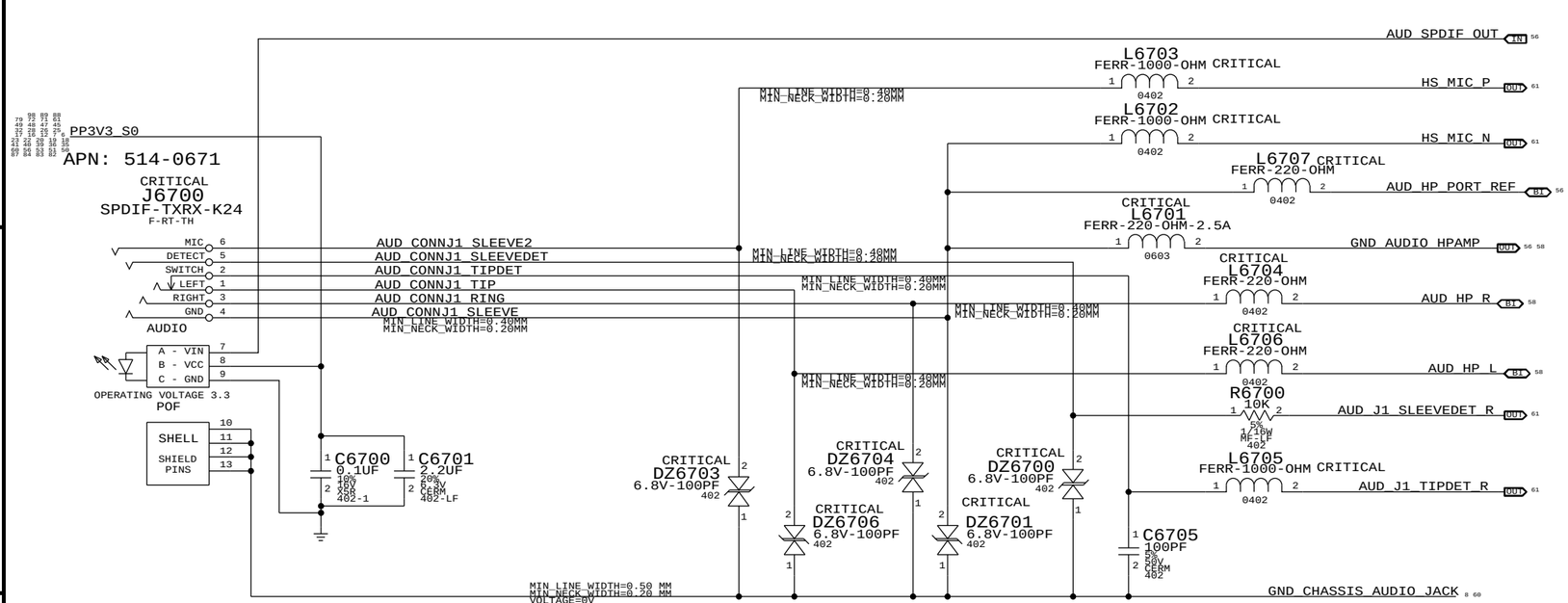
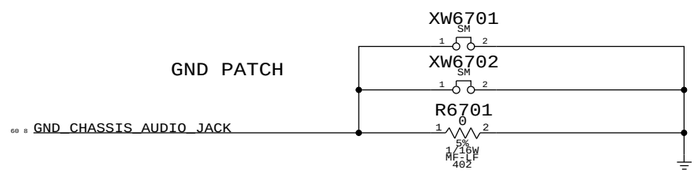
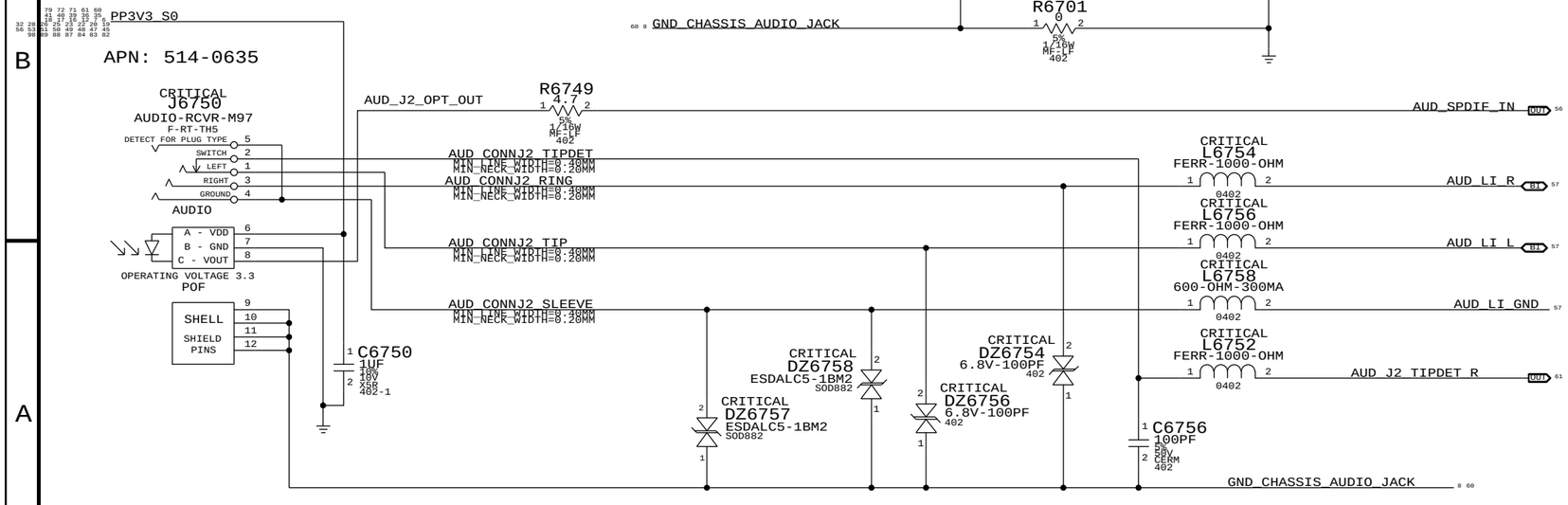
AUDIO JACK 1 LO/HP JACK, SPDIF TX



GND PATCH

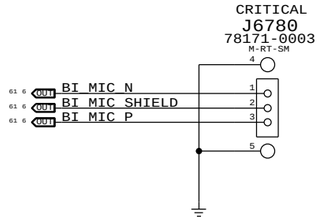


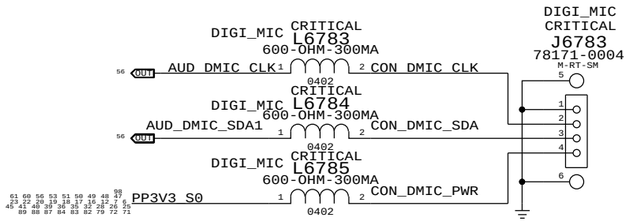
AUDIO JACK 2 LINE IN JACK, SPDIF RX



MIC CONNECTOR
Dual DMIC removed.Added single analog mic like K18.
Sept 21st 2010

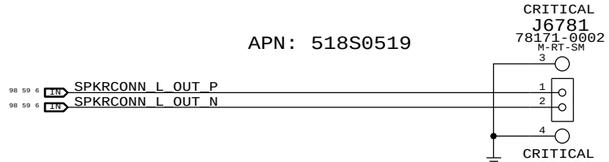
Place this in place of DMIC connector J6780



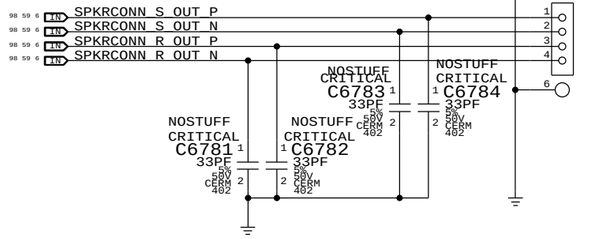


SPEAKER CONNECTOR

APN: 518S0519



APN: 518S0521



SYNC_MASTER=K91_AUDIO SYNC_DATE=09/30/2010

PAGE TITLE: AUDIO: JACKS

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ

PP3V3_S0 — CRITICAL L6880 FERR-1000-OHM 0402 — PP3V3_S0_HS_RX
MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM VOLTAGE=3.3V
R6886 10K 5% 1/16W MF-LF 402
CRITICAL C6880 10UF 20% 6.3V X5R 603
CRITICAL C6887 0.1UF 10% 16V X5R 402
CSP MIKEY APN:353S2640
CRITICAL U6880 CD3282A1 WCSP (AVDD, DGND, AGND)
PULLUPS ON MCP PAGE
R6882 0 5% 1/16W MF-LF 402 — SMBUS_PCH_CLK
R6883 0 5% 1/16W MF-LF 402 — SMBUS_PCH_DATA
R6884 0 5% 1/16W MF-LF 402 — AUD_I2C_INT_L
R6885 0 5% 1/16W MF-LF 402 — AUD_IPHS_SWITCH_EN
R6887 100K 5% 1/16W MF-LF 402
HS_SCL, HS_SDA, HS_INT_L, HS_ENABLE, TIPDET_UNFILT
MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM
HS_MIC_BIAS, HS_SW_DET, HS_RX_BP
CRITICAL C6882 2.2UF 20% 6.3V X5R 402
C6881 0.01UF 10% 16V CERM 402
GND_AUDIO_CODEC
R6880 1K 1% 1/16W MF-LF 402
R6881 2.2K 1% 1/16W MF-LF 402

PORT A DETECT (HEADPHONES) PORT B DETECT(SPDIF DELEGATE)

AUD_SENSE_A
PP3V3_S0_AUDIO_F
R6801 220K 5% 1/16W MF-LF 402
APN:376S0613
AUD_OUTJACK_INSERT_L
R6806 39.2K 1% 1/16W MF-LF 402 — AUD_PORTA_DET_L NC
R6805 20.0K 1% 1/16W MF-LF 402 — AUD_PORTB_DET_L NC
Q6800 SSM6N15FEAPE SOT563
Q6801 SSM6N15FEAPE SOT563
Q6801 SSM6N15FEAPE SOT563
R6802 47K 5% 1/16W MF-LF 402 — AUD_J1_TIPDET_R — AUD_J1_DET_RC
C6801 0.1UF 20% 10V CERM 402
GND_AUDIO_CODEC
R6803 220K 5% 1/16W MF-LF 402 — PP3V3_S0_AUDIO_F — AUD_J1_SLEEVEDET_INV
R6804 220K 5% 1/16W MF-LF 402
Q6800 SSM6N15FEAPE SOT563
AUD_J1_SLEEVEDET_R
C6802 0.01UF 10% 16V CERM 402
GND_AUDIO_CODEC
AUD_J1_SLEEVEDET_R

PORT B DETECT(SPDIF DELEGATE)

CRITICAL C6883 0.1UF 10% 25V X5R 402
R6890 2.2K 5% 1/16W MF-LF 402
AUD_MIC_INP_L — HS_MIC_HI_RC — HS_MIC_P
CRITICAL C6886 0.1UF 10% 25V X5R 402
AUD_MIC_INN_L
R6888 100K 5% 1/16W MF-LF 402
C6884 0.0082UF 10% 25V X7R 402 CRITICAL
XW6880 SM
C6885 27PF 5% 50V CERM 402 CRITICAL
GND_AUDIO_CODEC — HS_MIC_N

PORT B RIGHT(BUILT-IN MIC)

AUD_CODEC_MICBIAS
R6850 100 1% 1/16W MF-LF 402 — MIC_BIAS_FILT
R6851 2.4K 1% 1/16W MF 402-1
CRITICAL C6852 2.2UF 20% 6.3V X5R 402
GND_AUDIO_CODEC
CRITICAL C6850 0.1UF 10% 25V X5R 402 — AUD_MIC_INP_R — BI_MIC_HI_F
L6850 FERR-1000-OHM 0402 — BI_MIC_P
R6852 100K 5% 1/16W MF-LF 402
CRITICAL C6853 0.001UF 10% 50V X7R 402 CERM
CRITICAL C6851 0.1UF 10% 25V X5R 402 — AUD_MIC_INN_R — BI_MIC_LO_F
L6851 FERR-1000-OHM 0402 — BI_MIC_N
R6853 2.4K 1% 1/16W MF 402-1
GND_AUDIO_CODEC
XW6851 SM BI_MIC_SHIELD
HP=80HZ
Place this next to the connector

EXTRACTION NOTIFICATION

CRITICAL L6862 FERR-1000-OHM 0402 — PP3V3_S0 — PP3V3_S0_AUDIO_F
MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM VOLTAGE=3.3V
C6861 0.1UF 10% 25V X5R 402 CERM
GND_AUDIO_CODEC
R6865 100K 5% 1/16W MF-LF 402 — AUD_PERPH_DET_R
R6867 0 5% 1/16W MF-LF 402 — AUD_IP_PERIPHERAL_DET
R6864 220K 5% 1/16W MF-LF 402 — AUD_J1_TIPDET_INV
R6866 0 5% 1/16W MF-LF 402 — TIPDET_UNFILT
Q6803 SSM6N15FEAPE SOT563
Q6803 SSM6N15FEAPE SOT563
R6860 15K 5% 1/16W MF-LF 402 — AUD_J1_TIPDET_R — TIPDET_FILT
C6860 0.1UF 20% 10V CERM 402
GND_AUDIO_CODEC

PORT C DETECT (LINE-IN)

AUD_SENSE_A
PP3V3_S0_AUDIO_F
R6813 10K 1% 1/16W MF-LF 402
R6811 270K 5% 1/16W MF-LF 402
AUD_INJACK_INSERT_L NC
Q6802 SSM3K15FV SOD-VESM-HF
APN:376S0612
R6812 47K 5% 1/16W MF-LF 402 — AUD_J2_TIPDET_R — AUD_J2_DET_RC
C6811 0.1UF 20% 10V CERM 402
GND_AUDIO_CODEC

SYNC_MASTER=K91_AUDIO SYNC_DATE=09/21/2010
PAGE TITLE: AUDIO: JACK TRANSLATORS
Apple Inc.
DRAWING NUMBER: SIZE D
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PAGE: 68 OF 132
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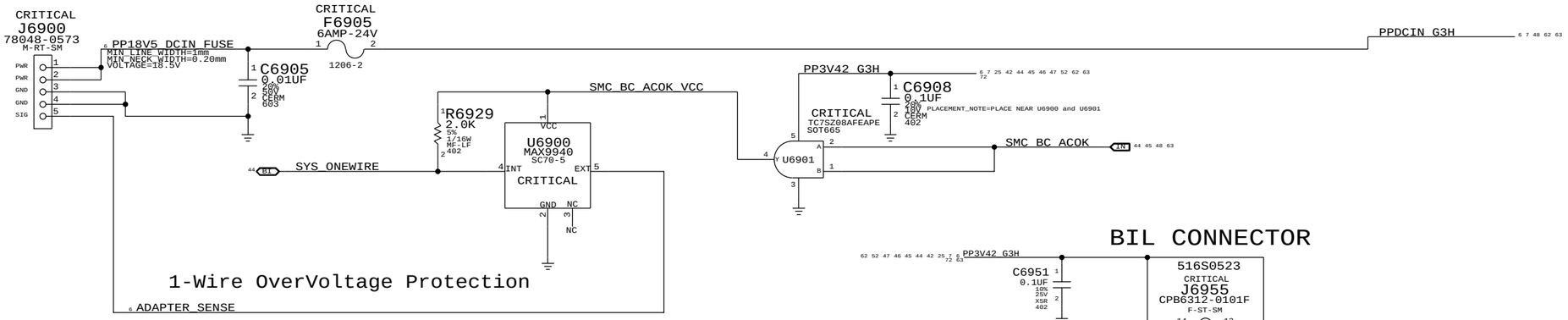
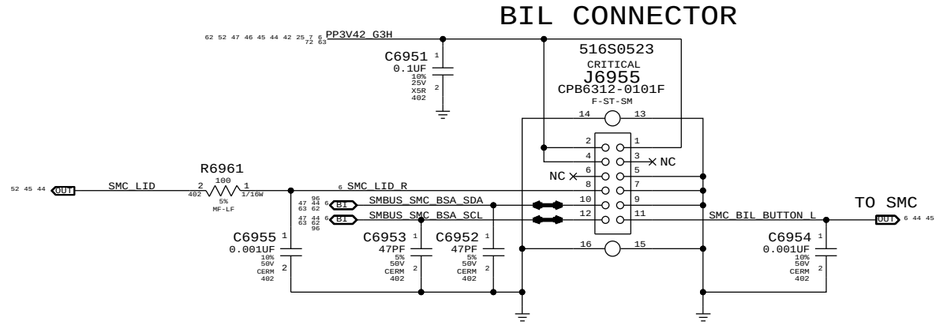
MagSafe DC Power Jack



1-Wire OverVoltage Protection

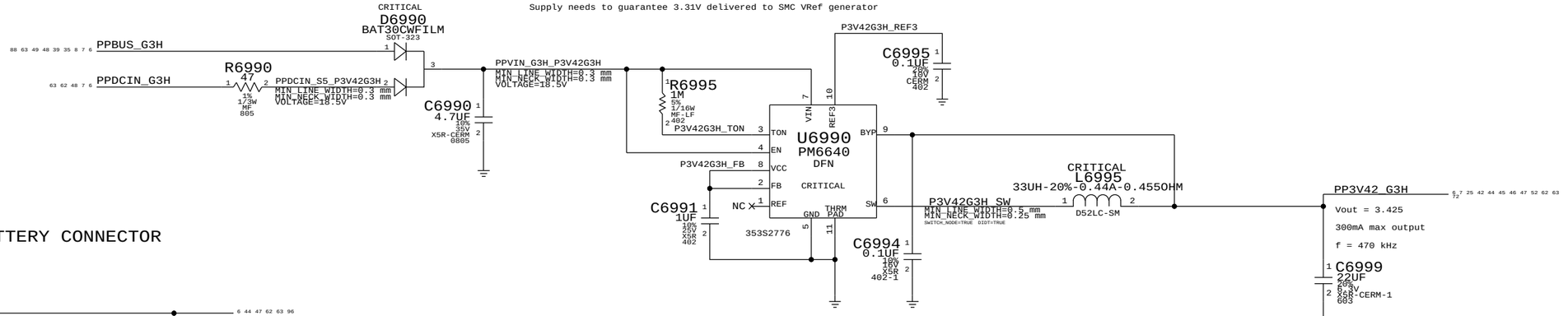
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

BIL CONNECTOR

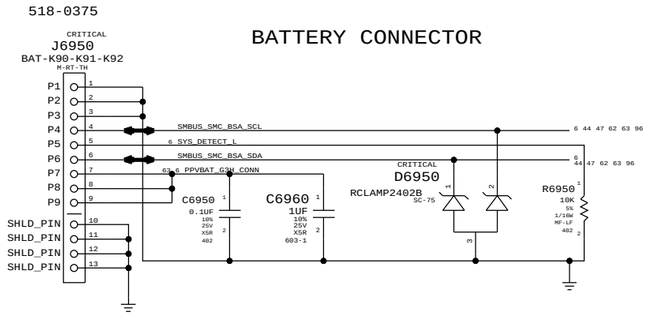


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE: DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER | SIZE: D

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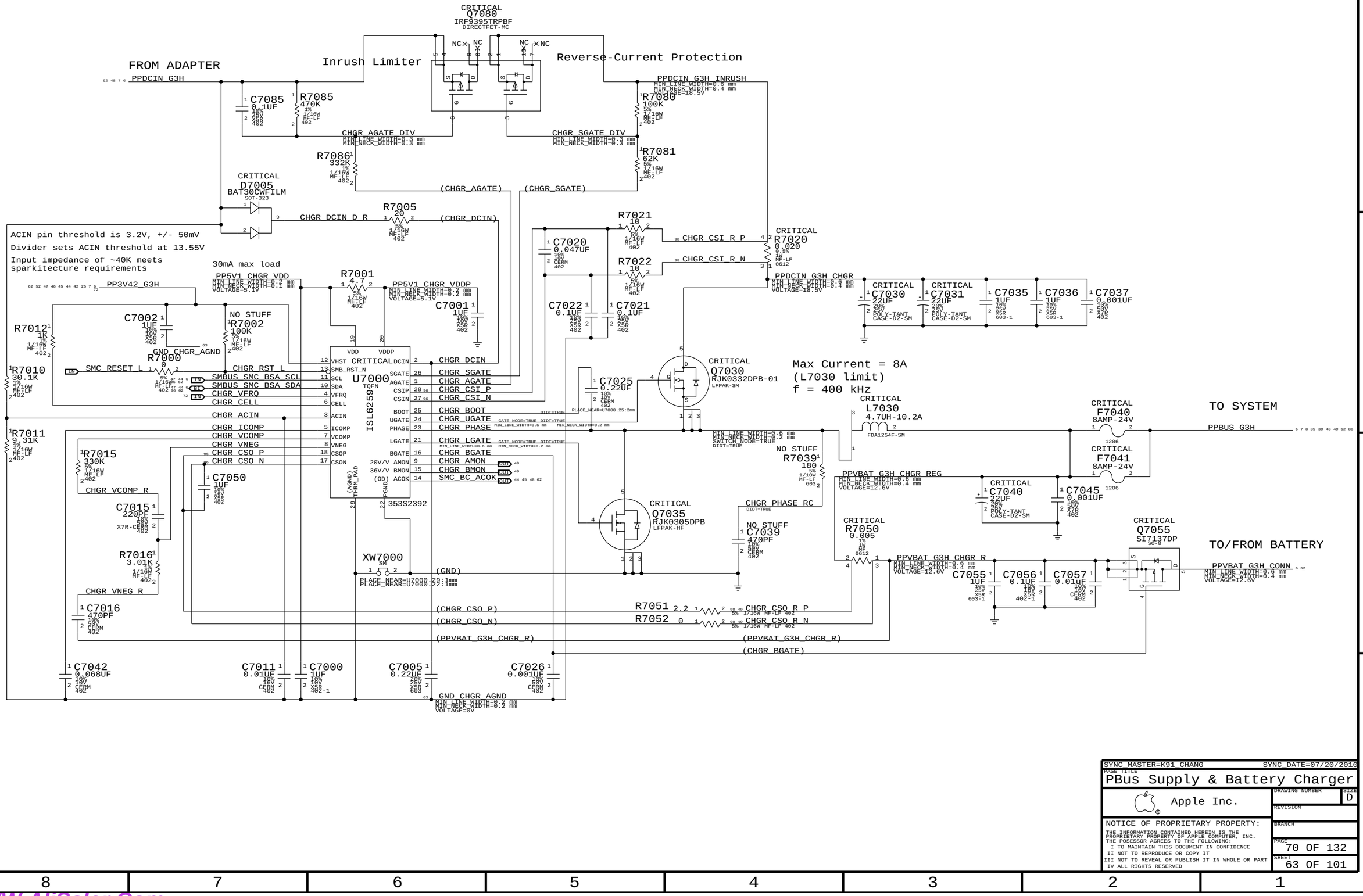

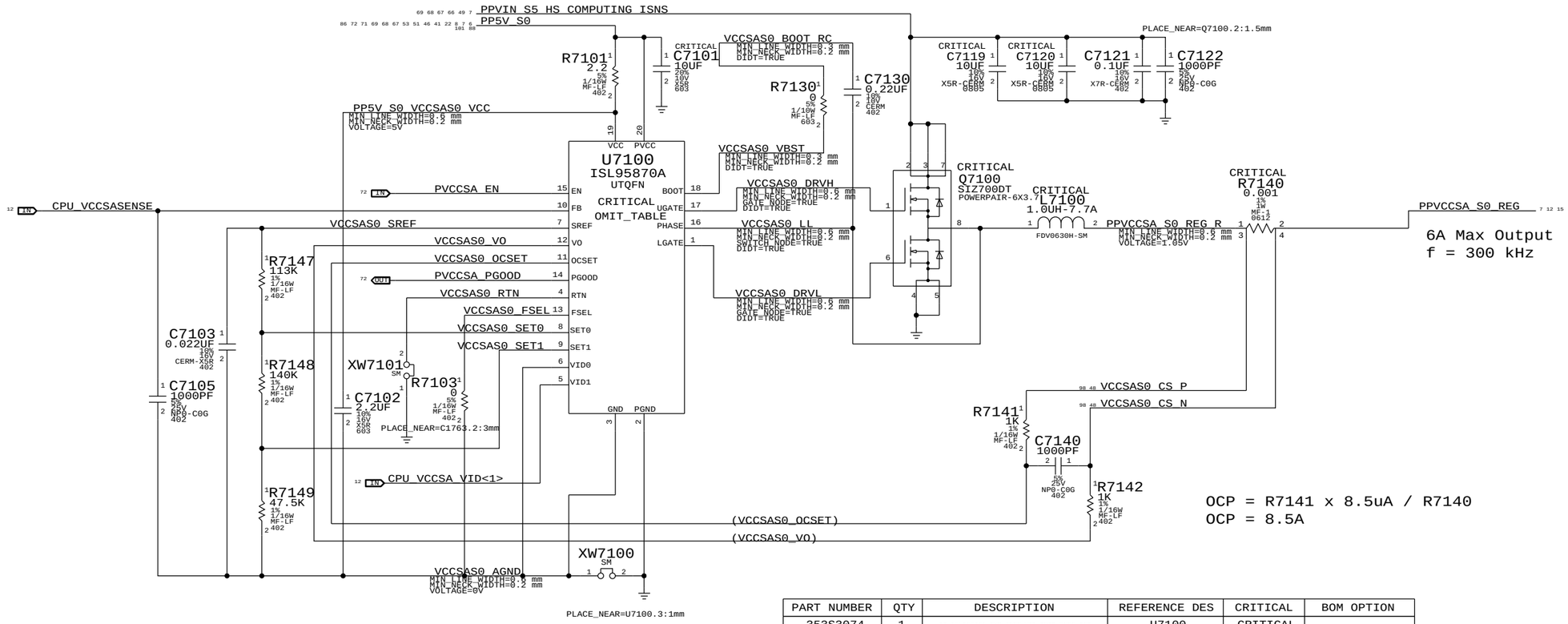

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3074	1	IC,ISL95870A,PWM,2BIT-VID,RMOT-SNSE,20P	U7100	CRITICAL	

SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE: System Agent Supply

Apple Inc.

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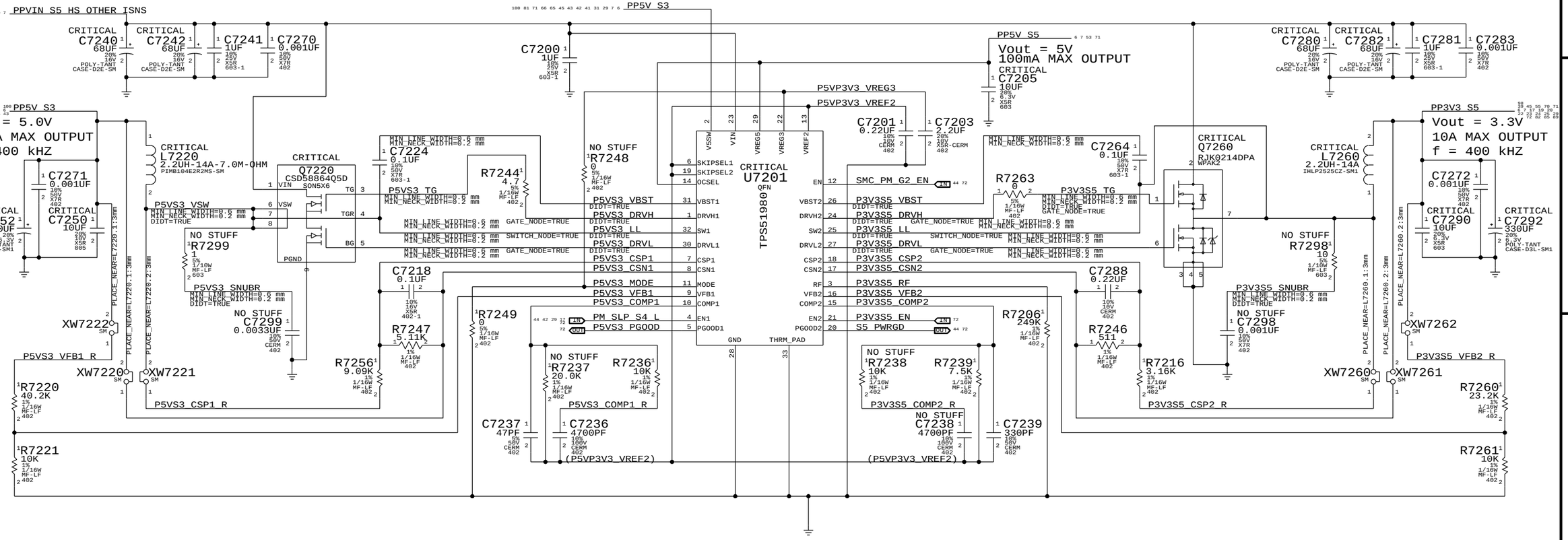

SYNC_MASTER=K91_ERIC	SYNC_DATE=10/08/2010
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER · SIZE D
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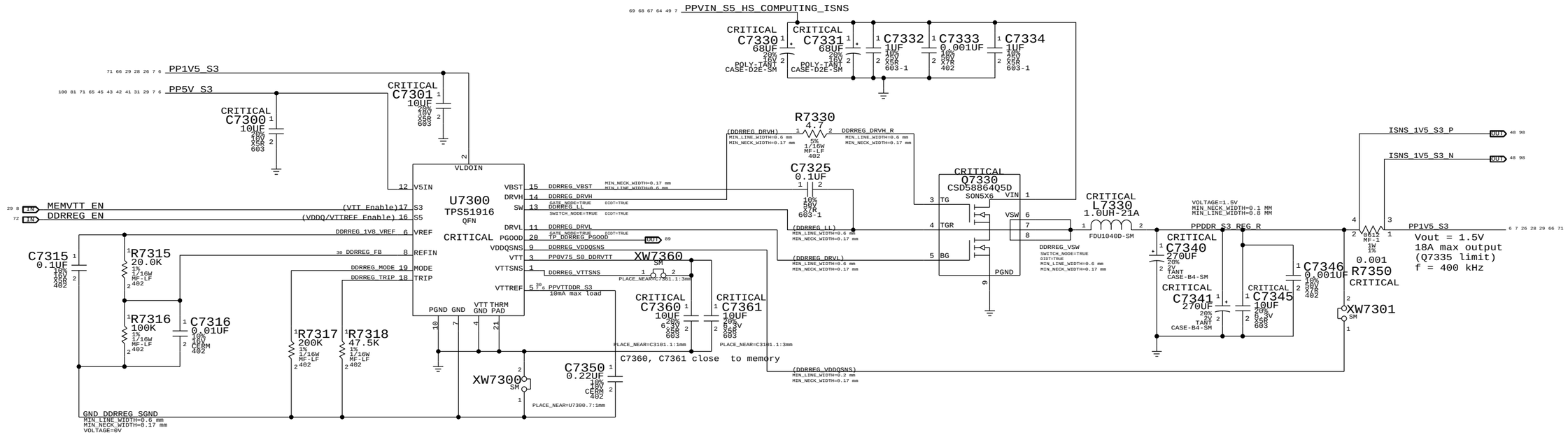

SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE: 1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER | SIZE: D

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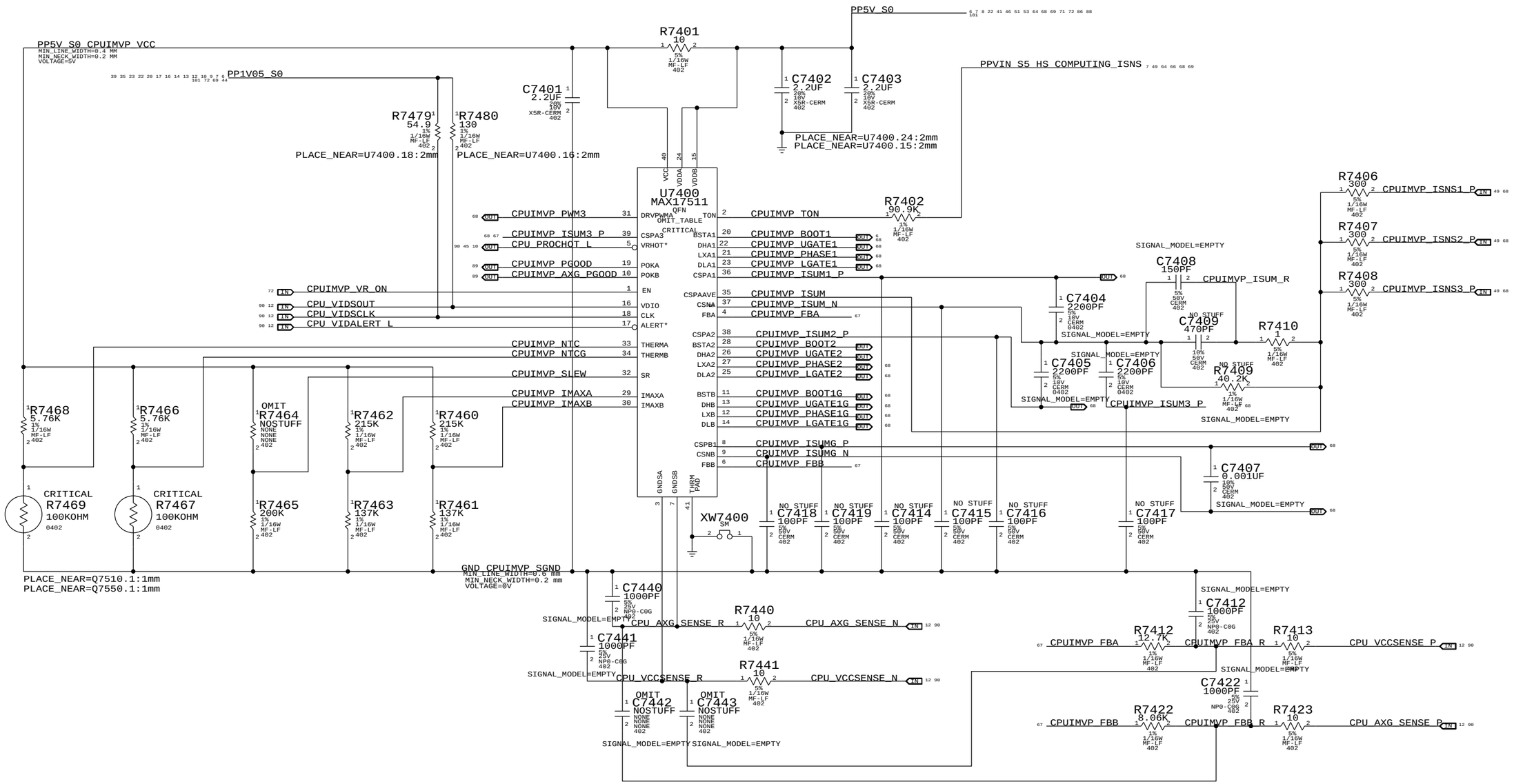
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3259	1	IC,MAX15092,3+1PH CPU REG,IMVP7,5X5QFN40	U7400	CRITICAL	



SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

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PHASE 1

PPVIN_S5_HS_COMPUTING_ISNS

376S0872

CRITICAL Q7510 IRF6723M2DPBF DIRECTFET-MA

CRITICAL L7510 0.36UH-20%-40A-0.000750HM PIMA104E-SM 152S1019

CRITICAL R7510 0.00075 1% 1W MF 0612

THESE TWO CAPS ARE FOR EMC

CRITICAL C7513 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7514 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7515 10UF 10% 16V X5R-CERM 0805

CRITICAL C7516 10UF 10% 16V X5R-CERM 0805

CRITICAL C7517 1UF 10% 16V X5R 402

CRITICAL C7518 0.001UF 10% 50V X7R 402

C7519 0.001UF 10% 50V X7R 402

CPUIMVP_BOOT1_RC MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE

R7511 0 5% 1/16W MF-LF 402

C7511 0.22UF 10% 16V CERM 402

CPUIMVP_BOOT1 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE

CPUIMVP_UGATE1 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_PHASE1 MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE SWITCH_NODE=TRUE

CPUIMVP_LGATE1 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CRITICAL Q7515 IRF6798MTRPBF DIRECTFET-MX

376S0930

NOSTUFF R7512 2.2 5% 1/10W MF-LF 603

CPUIMVP_PH1_SNUB DIDT=TRUE

NOSTUFF C7512 0.001UF 10% 50V X7R 402

CPUIMVP_ISNS1_P

CPUIMVP_ISNS1_N

R7513 46.4 1% 1/16W MF-LF 402

R7514 10.2 1% 1/16W MF-LF 402

CPUIMVP_ISUM_N

NOSTUFF C7571 330PF 10% 50V CERM 402

CPUIMVP_ISUM1_P

PPVCORE_S0_CPU_PH1_L

PPVCORE_S0_CPU_PH1

PPVCORE_S0_CPU

PHASE 2

376S0872

CRITICAL Q7510 IRF6723M2DPBF DIRECTFET-MA

CRITICAL L7520 0.36UH-20%-40A-0.000750HM PIMA104E-SM 152S1019

CRITICAL R7520 0.00075 1% 1W MF 0612

THESE TWO CAPS ARE FOR EMC

CRITICAL C7523 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7524 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7525 10UF 10% 16V X5R-CERM 0805

CRITICAL C7526 10UF 10% 16V X5R-CERM 0805

CRITICAL C7527 1UF 10% 16V X5R 402

CRITICAL C7528 0.001UF 10% 50V X7R 402

C7529 0.001UF 10% 50V X7R 402

CPUIMVP_BOOT2_RC MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE

R7521 0 5% 1/16W MF-LF 402

C7521 0.22UF 10% 16V CERM 402

CPUIMVP_BOOT2 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE

CPUIMVP_UGATE2 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_PHASE2 MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE SWITCH_NODE=TRUE

CPUIMVP_LGATE2 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CRITICAL Q7525 IRF6798MTRPBF DIRECTFET-MX

376S0930

NOSTUFF R7522 2.2 5% 1/10W MF-LF 603

CPUIMVP_PH2_SNUB DIDT=TRUE

NOSTUFF C7522 0.001UF 10% 50V X7R 402

CPUIMVP_ISNS2_P

CPUIMVP_ISNS2_N

R7523 46.4 1% 1/16W MF-LF 402

R7524 10.2 1% 1/16W MF-LF 402

CPUIMVP_ISUM_N

NOSTUFF C7572 330PF 10% 50V CERM 402

CPUIMVP_ISUM2_P

PPVCORE_S0_CPU_PH2_L

PPVCORE_S0_CPU_PH2

PPVCORE_S0_CPU

PHASE 3

376S0772

CRITICAL Q7530 IRF6710 S1

CRITICAL L7530 0.36UH-20%-40A-0.000750HM PIMA104E-SM 152S1019

CRITICAL R7530 0.00075 1% 1W MF 0612

THESE TWO CAPS ARE FOR EMC

CRITICAL C7533 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7534 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7535 10UF 10% 16V X5R-CERM 0805

CRITICAL C7536 10UF 10% 16V X5R-CERM 0805

CRITICAL C7537 1UF 10% 16V X5R 402

CRITICAL C7538 0.001UF 10% 50V X7R 402

C7539 0.001UF 10% 50V X7R 402

CPUIMVP_BOOT3_RC MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE

R7531 0 5% 1/16W MF-LF 402

C7531 0.22UF 10% 16V CERM 402

PP5V_S0

R7547 10K 5% 1/16W MF-LF 402

C7541 1UF 10% 16V X5R 402

U7541 MAX17491 TQFN CRITICAL

VDD PWN SKIP* BST DH LX DL GND THRM PAD

CPUIMVP_PWM3

CPUIMVP_SKIP

CPUIMVP_BOOT3 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE

CPUIMVP_UGATE3 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_PHASE3 MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE SWITCH_NODE=TRUE

CPUIMVP_LGATE3 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CRITICAL Q7535 IRF6798MTRPBF DIRECTFET-MX

376S0930

NOSTUFF R7532 2.2 5% 1/10W MF-LF 603

CPUIMVP_PH3_SNUB DIDT=TRUE

NOSTUFF C7532 0.001UF 10% 50V X7R 402

CPUIMVP_ISNS3_P

CPUIMVP_ISNS3_N

R7533 46.4 1% 1/16W MF-LF 402

R7534 10.2 1% 1/16W MF-LF 402

CPUIMVP_ISUM_N

NOSTUFF C7573 330PF 10% 50V CERM 402

CPUIMVP_ISUM3_P

SWITCH_NODE=TRUE

PPVCORE_S0_CPU_PH3_L

PPVCORE_S0_CPU_PH3

PPVCORE_S0_CPU

Additonal Input Bulk Caps

CRITICAL C7561 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7562 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7563 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7564 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7565 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7566 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7567 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7568 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7569 68UF 20% 16V POLY-TANT CASE-D2E-SM

AXG PHASE

PPVIN_S5_HS_COMPUTING_ISNS

THESE TWO CAPS ARE FOR EMC

CRITICAL C7553 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7554 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7555 10UF 10% 16V X5R-CERM 0805

CRITICAL C7556 10UF 10% 16V X5R-CERM 0805

CRITICAL C7557 1UF 10% 16V X5R 402

CRITICAL C7558 0.001UF 10% 50V X7R 402

C7559 0.001UF 10% 50V X7R 402

CRITICAL Q7550 CSD58864Q5D SON5X6

CRITICAL L7550 0.36UH-20%-40A-0.000750HM PIMA104E-SM 152S1019

CRITICAL R7550 0.00075 1% 1W MF 0612

CPUIMVP_BOOT1G_R MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE

CPUIMVP_BOOT1G MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE

C7551 0.22UF 10% 16V CERM 402

R7555 4.7 5% 1/10W MF-LF 402

CPUIMVP_UGATE1G_R MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_UGATE1G MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_PHASE1G MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE SWITCH_NODE=TRUE

CPUIMVP_LGATE1G MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

376S0906

CPUIMVP_VSWG MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM SWITCH_NODE=TRUE

NOSTUFF R7552 2.2 5% 1/10W MF-LF 603

CPUIMVP_AXG_SNUB DIDT=TRUE

NOSTUFF C7552 0.001UF 10% 50V X7R 402

CPUIMVP_ISNS1G_P

CPUIMVP_ISNS1G_N

R7553 46.4 1% 1/16W MF-LF 402

R7554 10.2 1% 1/16W MF-LF 402

CPUIMVP_ISUMG_N

NOSTUFF C7574 330PF 10% 50V CERM 402

CPUIMVP_ISUMG_P

PPVCORE_S0_AXG_L

PPVCORE_S0_AXG

SYNC_MASTER=K91_ERIC	SYNC_DATE=09/22/2010
PAGE TITLE	CPU IMVP7 & AXG VCore Output
Apple Inc.	DRAWING NUMBER: D; SIZE
	REVISION
	BRANCH
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	SHEET: 68 OF 101

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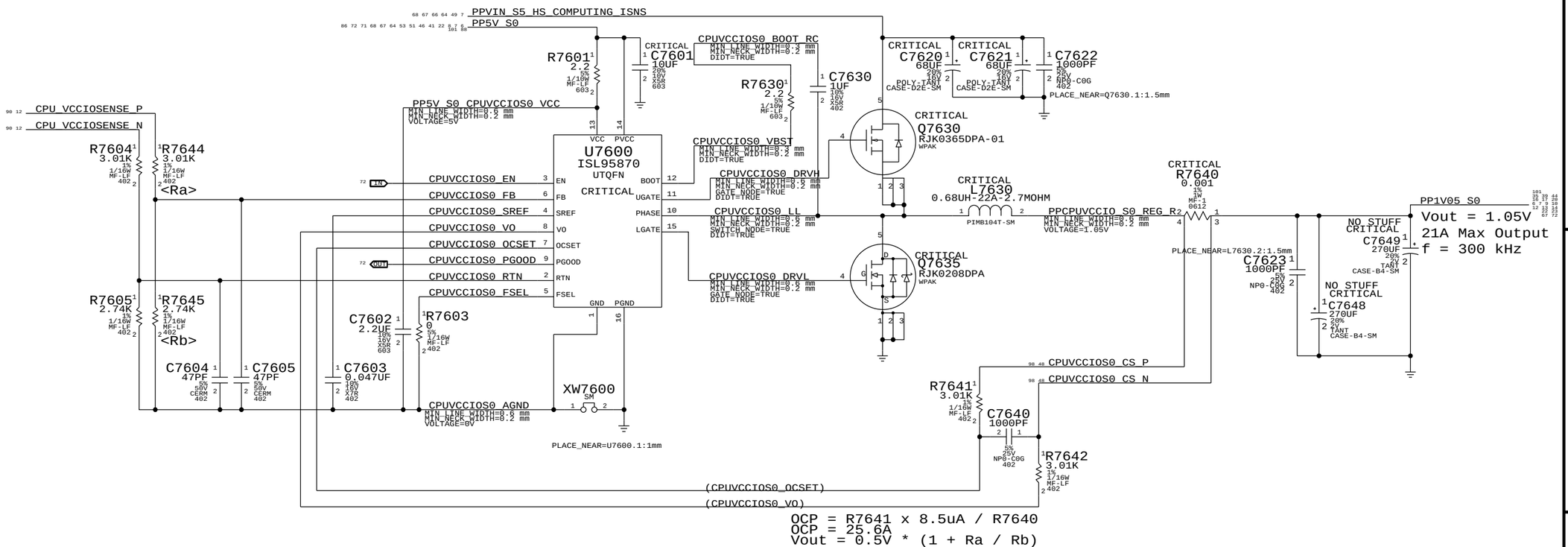
CPU VCCIO (1.05V S0) Regulator



SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE: CPU VCCIO (1.05V) Power Supply

Apple Inc.

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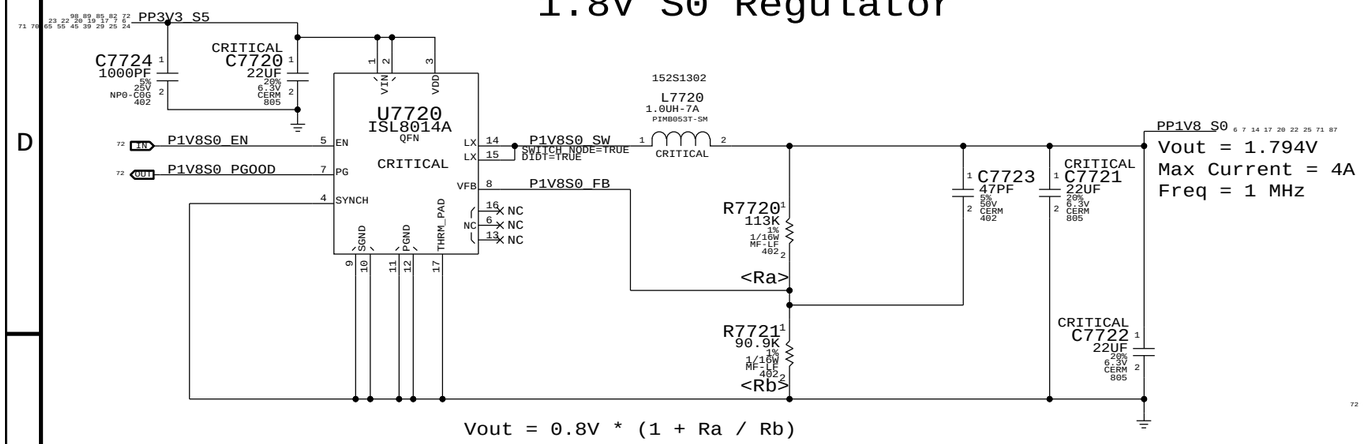
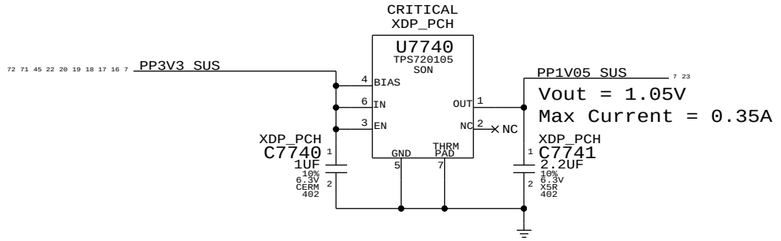
1.8V S0 Regulator

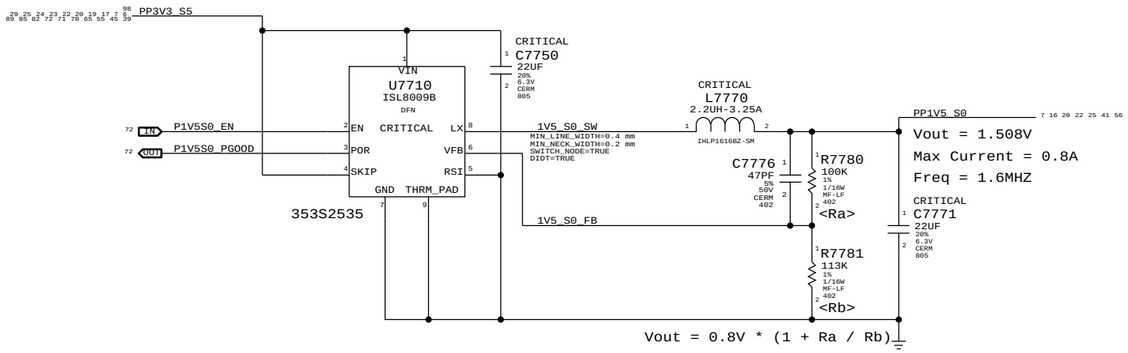


1.05V SUS LDO

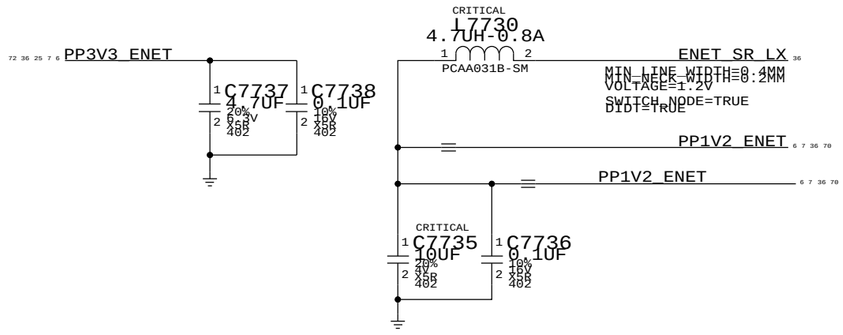
Cougar Point-M requires JTAG pull-ups to be powered at 1.05V in Sus.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V Sus, which burns 100mW in all S-states.



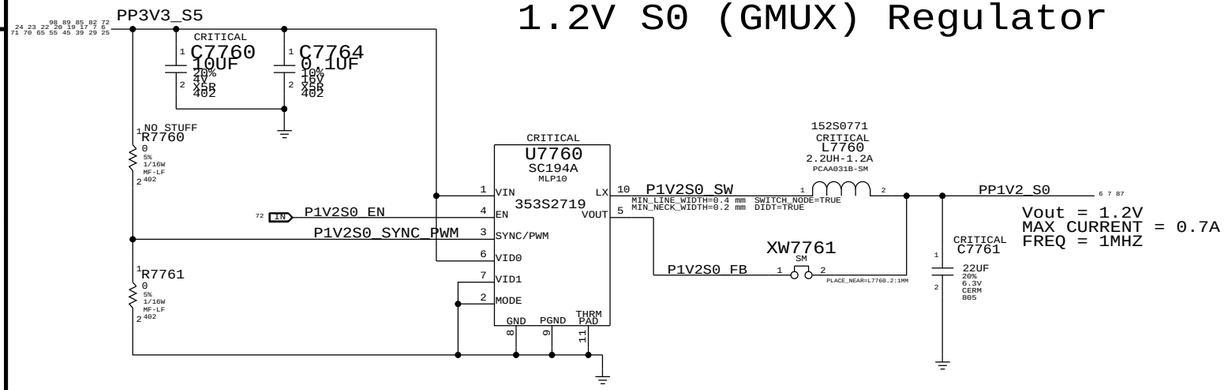
1.5V S0 Regulator



CAESAR IV 1.2V INT.VR CMPTS



1.2V S0 (GMUX) Regulator



SYNC_MASTER=K91_ERIC	SYNC_DATE=11/01/2010
PAGE TITLE	Misc Power Supplies
Apple Inc.	DRAWING NUMBER / SIZE D
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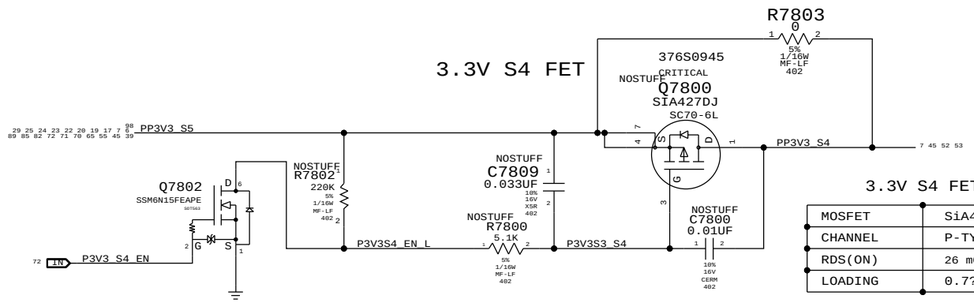
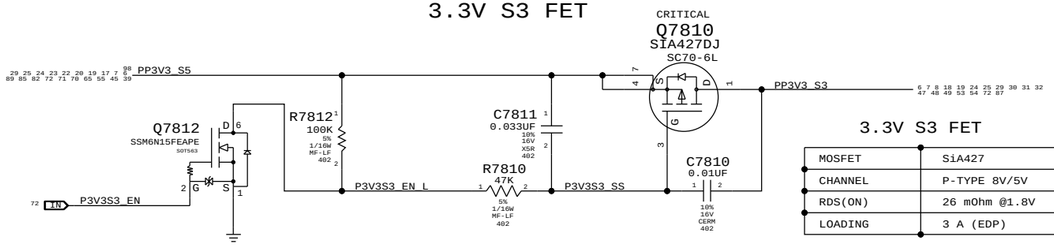
3.3V S4 FET



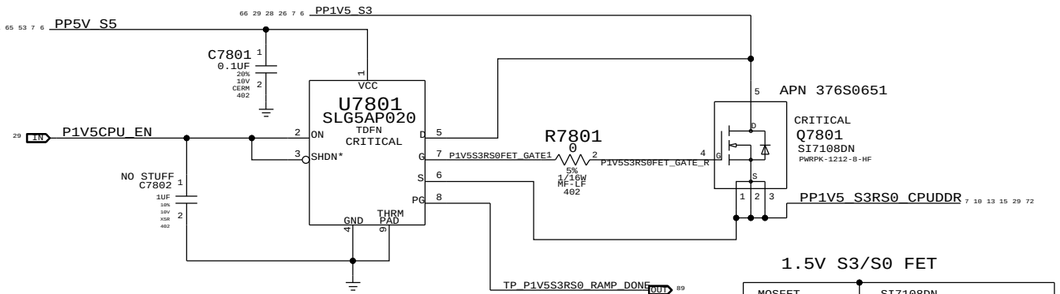
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)

3.3V S3 FET



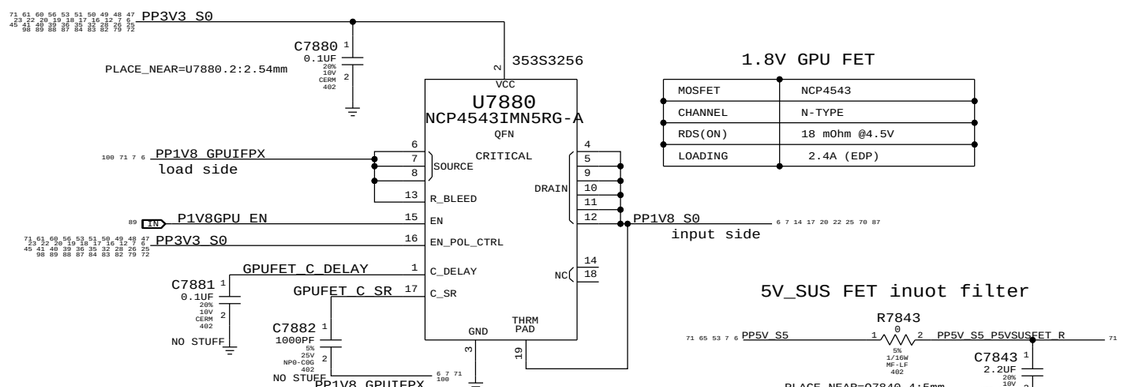
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

1.5V S3/S0 FET



1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

1.8V GPU FET

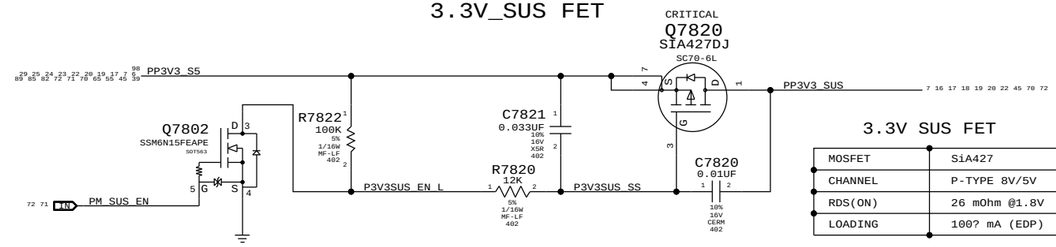


1.8V GPU FET	
MOSFET	NCP4543
CHANNEL	N-TYPE
RDS(ON)	18 mOhm @4.5V
LOADING	2.4A (EDP)

5V_SUS FET inuot filter

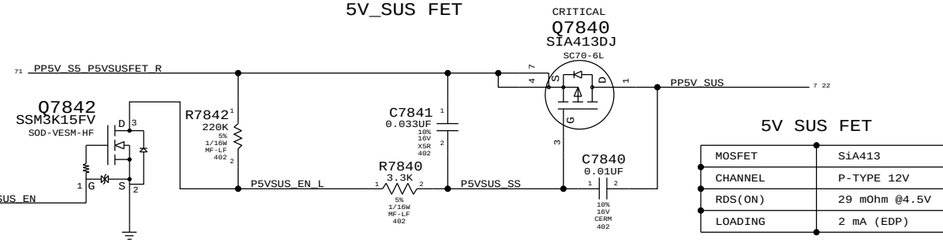
U7880 default Turn on delay EN--> on is 200~650us.

3.3V_SUS FET



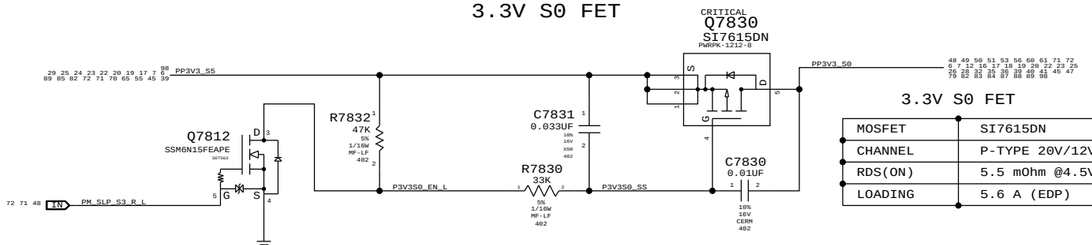
3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V_SUS FET



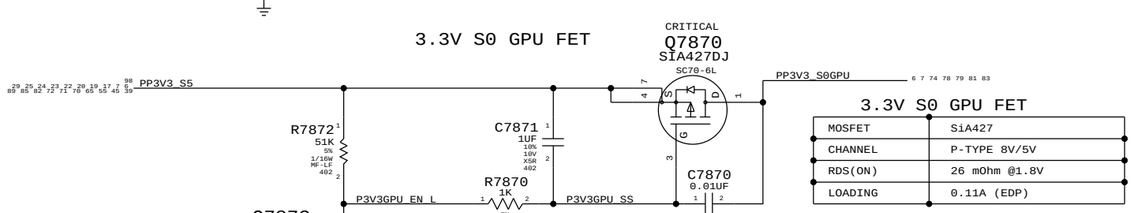
5V SUS FET	
MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

3.3V S0 FET



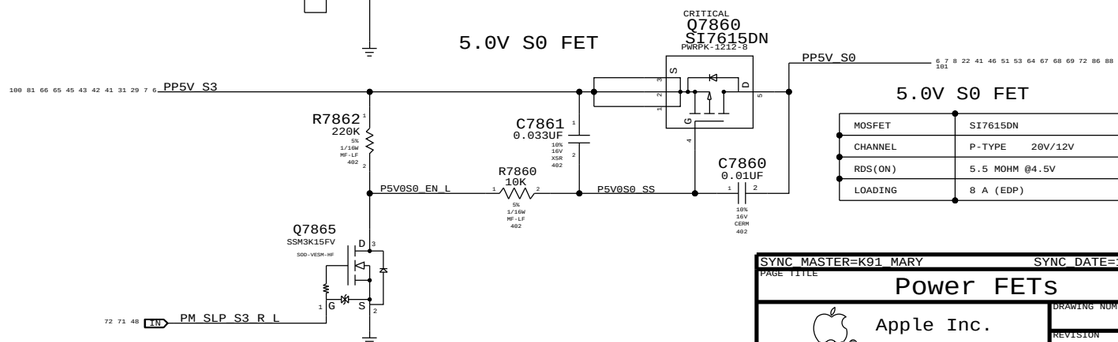
3.3V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)

3.3V S0 GPU FET



3.3V S0 GPU FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	8 A (EDP)

SYNC_MASTER=K91_MARY SYNC_DATE=10/14/2016

PAGE TITLE: Power FETs

Apple Inc.

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S5 Rail Enables & PGOOD

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

SMC_PM_G2_EN
SMC_PM_G2_EN MAKE_BASE=TRUE
R7940 100 5% 1/16W MF-LF 402
PLACE_NEAR=U7201.21:7mm
C7942 0.0033UF 10% 50V CERM 402 NO STUFF
P3V3S5_EN MAKE_BASE=TRUE
P3V3S5_EN
PP3V42_G3H
PLACE_NEAR=U7201.20:7mm
R7941 100K 5% 1/16W MF-LF 402
S5_PWRGD
S5_PWRGD MAKE_BASE=TRUE
S5_PWRGD (old name RSMRST_PWRGD)-->SMC
SMC-->PM_DSW_PWRGD

3.3V/5.0V S4 ENABLE

NOSTUFF
R7916 0 5% 1/16W MF-LF 402
PLACE_NEAR=U1800.G18:5mm
PM_SLP_S5_L
P3V3_S4_EN MAKE_BASE=TRUE
P3V3_S4_EN
PM_SLP_S5_L:100K pull down on PCH page

3.3V,5V S3 ENABLE

PM_SLP_S4_L
PM_SLP_S4_L MAKE_BASE=TRUE
PM_SLP_S4_L:100K pull down in PCH page
R7911 5.1K 5% 1/16W MF-LF 402 PLACE_NEAR=U7300.16:6mm
R7912 0 5% 1/16W MF-LF 402 PLACE_NEAR=Q7812.2:6mm
R7913 3.3K 5% 1/16W MF-LF 402
PLACE_NEAR=U5701.4:6mm
TPAD_VBUS_EN
P3V3S3_EN MAKE_BASE=TRUE
P3V3S3_EN
DDRREG_EN MAKE_BASE=TRUE
DDRREG_EN
C7910 0.47UF 10% 6.3V CERM-X5R 402
C7912 0.47UF 10% 6.3V CERM-X5R 402 NO STUFF

3.3V/5.0V Sus ENABLE

PP3V3_S5
PLACE_NEAR=U7940.1:2.3mm
C7940 0.1uF 20% 10V CERM 402
U7940 74AUP1G3208 SOT891
SMC_BATLOW_L:100K pull up on SMC page
SMC_BATLOW_L
PM_SLP_SUS_L:100K pull down on PCH page
PM_SLP_SUS_L
PM_SUS_EN MAKE_BASE=TRUE
PM_SUS_EN
PM_SUS_EN
NO STUFF
R7917 0 5% 1/16W MF-LF 402

S0 ENABLE

R7978 100 5% 1/16W MF-LF 402
PM_SLP_S3_L
PM_SLP_S3_L:100K pull down in PCH page
(PM_SLP_S3_R_L)
PM_SLP_S3_R_L MAKE_BASE=TRUE
PM_SLP_S3_R_L
PM_SLP_S3_R_L
PM_SLP_S3_R_L
R7987 33K 5% 1/16W MF-LF 402 PLACE_NEAR=U7100.15:6mm
R7981 20K 5% 1/16W MF-LF 402 PLACE_NEAR=U7600.3:6mm
R7985 20K 5% 1/16W MF-LF 402 PLACE_NEAR=U7760.4:6mm
R7988 10K 5% 1/16W MF-LF 402 PLACE_NEAR=U7720.5:6mm
R7986 5.1K 5% 1/16W MF-LF 402
P1V8S0_EN MAKE_BASE=TRUE
P1V8S0_EN
P1V5S0_EN MAKE_BASE=TRUE
P1V5S0_EN
P1V2S0_EN MAKE_BASE=TRUE
P1V2S0_EN
CPUVCCIOS0_EN MAKE_BASE=TRUE
CPUVCCIOS0_EN
PVCCSA_EN MAKE_BASE=TRUE
PVCCSA_EN
C7987 0.47UF 10% 6.3V CERM-X5R 402 PLACE_NEAR=U7100.15:6mm
C7981 0.47UF 10% 6.3V CERM-X5R 402 PLACE_NEAR=U7600.3:6mm
C7985 1UF 10% 6.3V CERM-X5R 402 PLACE_NEAR=U7760.4:6mm
C7988 0.47UF 10% 6.3V CERM-X5R 402 PLACE_NEAR=U7710.2:6mm
C7986 0.47UF 10% 6.3V CERM-X5R 402 PLACE_NEAR=U7720.5:6mm

CPUVCORE ENABLE

ALL_SYS_PWRGD
R7974 0 5% 1/16W MF-LF 402 PLACE_NEAR=U7400.7:5mm
CPUIMVP_VR_ON
PLACE_NEAR=U7400.7:5mm
R7976 0 5% 1/16W MF-LF 402 NO STUFF
CPUVCCIOS0_PGOOD
R7975 0 5% 1/16W MF-LF 402 PLACE_NEAR=U7400.7:5mm
PM_PECI_PWRGD

CHGR VFRQ Generation

PP3V42_G3H
R7931 100K 5% 1/16W MF-LF 402
CHGR_VFRQ
Q7931 SSM3K15FV SOD-VESM-HF
VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency

S0 Rail PGOOD (BJT Version)

PP3V3_S5
PP3V3_S0
R7951 15.0K 1% 1/16W MF-LF 402
R7956 150K 1% 1/16W MF-LF 402
S0PGD_C
ALL_SYS_PWRGD
R7953 1K 5% 1/16W MF-LF 402
VMON_3V3_DIV
VMON_Q2_BASE
R7952 7.15K 1% 1/16W MF-LF 402
R7954 1K 5% 1/16W MF-LF 402
NC
VMON_Q3_BASE
PP1V5_S3RS0_CPUDDR
PP1V5_S3RS0
NC
R7955 1K 5% 1/16W MF-LF 402
PP1V05_S0
VMON_Q4_BASE
Q7950 ASMCC0179 DFN2015H4-8
CRITICAL
353S2809
S0PGD_BJT_GND_R
R7957 100 5% 1/16W MF-LF 402
Worst-Case Thresholds:
Q2: 0.XXXV
Q3: 0.640V
3.3V w/Divider: 2.345V
Q4: 0.660V

3.3V SUS Detect

PP3V3_S5
PLACE_NEAR=U7930.6:2.3mm
No stuff C7931, 12ms Min delay time
U7930 Sense input threhold is 3.07V
C7930 0.1uF 20% 16V CERM 402
CRITICAL
R7933 100K 5% 1/16W MF-LF 402
PP3V3_SUS
U7930 TPS3808G33DBVRG4 SOT23-6
PP3V3_SUS
PM_RSMRST_L
PM_RSMRST_L goes to U1800.C21
Sus_PGOOD_CT
C7931 0.001UF 10% 50V CERM 402 NO STUFF

ENET Enable Generation

3.3V ENET FET

CRITICAL
Q7922 NTR4101P SOT-23-HF
PP3V3_S3
PP3V3_ENET
R7921 10K 5% 1/16W MF-LF 402
C7921 0.033UF 10% 16V CERM 402
R7922 100K 5% 1/16W MF-LF 402
PM_SLP_S3_ENET
P3V3ENET_SS
C7922 0.01UF 10% 16V CERM 402
"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.
Q7921 SSM3K15FV SOD-VESM-HF
PM_SLP_S3_L
Q7925 2N7002DW-X-G SOT-363
WOL_EN
PM_WLAN_EN_L
Q7925 2N7002DW-X-G SOT-363
AP_PWR_EN
AC_EN_L
(AC_EN_L)
Q7920 2N7002DW-X-G SOT-363
NO STUFF
R7929 0 5% 1/16W MF-LF 402
SMC_ADAPTER_EN
Q7920 2N7002DW-X-G SOT-363
(PM_SLP_S3_L)

S0 Rail PGOOD Circuitry (ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

PP5V_S0
PP1V5_S3RS0_CPUDDR
PP1V05_S0
S0PGOOD_ISL
R7960 6.04K 1% 1/16W MF-LF 402
R7970 10K 1% 1/16W MF-LF 402
R7972 6.04K 1% 1/16W MF-LF 402
C7960 0.1uF 20% 10V CERM 402
U7960 ISL88042IRTEZ TDFN (IPU)
CRITICAL
PP5V_DIV_VMON
PP1V05_DIV_VMON
PP1V05_VID_VMON
R7961 15.0K 1% 1/16W MF-LF 402
R7971 10K 1% 1/16W MF-LF 402
R7973 15.0K 1% 1/16W MF-LF 402
V2MON
V3MON
V4MON
NC
RST*
GND THRM_PAD
353S2310
ALL_SYS_PWRGD_R
R7962 330 5% 1/16W MF-LF 402
ALL_SYS_PWRGD
PP3V3_S0
R7967 10K 5% 1/16W MF-LF 402
R7968 100 5% 1/16W MF-LF 402
P1V5S0_PGOOD
P1V5S0_PGOOD from U7710
P1V8S0_PGOOD
R7966 100 5% 1/16W MF-LF 402
R7965 100 5% 1/16W MF-LF 402
P5VS3_PGOOD
CPUVCCIOS0_PGOOD
R7964 100 5% 1/16W MF-LF 402
R7963 100 5% 1/16W MF-LF 402
PVCCSA_PGOOD
SMC_S4_WAKESRC_EN MAKE_BASE=TRUE
SMC_S4_WAKESRC_EN

SYNC_MASTER=K91_MARY SYNC_DATE=07/22/2010
PAGE TITLE
Power Control 1/ENABLE
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Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PEG_R2D_C_P<0>	C8020	PEG_R2D_P<0>	PEG_R2D_C_N<0>	C8021	PEG_R2D_N<0>	PEG_R2D_C_P<1>	C8022	PEG_R2D_P<1>	PEG_R2D_C_N<1>	C8023	PEG_R2D_N<1>	PEG_R2D_C_P<2>	C8024	PEG_R2D_P<2>	PEG_R2D_C_N<2>	C8025	PEG_R2D_N<2>
PEG_R2D_C_P<3>	C8026	PEG_R2D_P<3>	PEG_R2D_C_N<3>	C8027	PEG_R2D_N<3>	PEG_R2D_C_P<4>	C8028	PEG_R2D_P<4>	PEG_R2D_C_N<4>	C8029	PEG_R2D_N<4>	PEG_R2D_C_P<5>	C8030	PEG_R2D_P<5>	PEG_R2D_C_N<5>	C8031	PEG_R2D_N<5>
PEG_R2D_C_P<6>	C8032	PEG_R2D_P<6>	PEG_R2D_C_N<6>	C8033	PEG_R2D_N<6>	PEG_R2D_C_P<7>	C8034	PEG_R2D_P<7>	PEG_R2D_C_N<7>	C8035	PEG_R2D_N<7>						

PEG_D2R_C_P<0>	C8055	PEG_D2R_P<0>	PEG_D2R_C_N<0>	C8056	PEG_D2R_N<0>	PEG_D2R_C_P<1>	C8057	PEG_D2R_P<1>	PEG_D2R_C_N<1>	C8058	PEG_D2R_N<1>	PEG_D2R_C_P<2>	C8059	PEG_D2R_P<2>	PEG_D2R_C_N<2>	C8060	PEG_D2R_N<2>
PEG_D2R_C_P<3>	C8061	PEG_D2R_P<3>	PEG_D2R_C_N<3>	C8062	PEG_D2R_N<3>	PEG_D2R_C_P<4>	C8063	PEG_D2R_P<4>	PEG_D2R_C_N<4>	C8064	PEG_D2R_N<4>	PEG_D2R_C_P<5>	C8065	PEG_D2R_P<5>	PEG_D2R_C_N<5>	C8066	PEG_D2R_N<5>
PEG_D2R_C_P<6>	C8067	PEG_D2R_P<6>	PEG_D2R_C_N<6>	C8068	PEG_D2R_N<6>	PEG_D2R_C_P<7>	C8069	PEG_D2R_P<7>	PEG_D2R_C_N<7>	C8070	PEG_D2R_N<7>						

All: 0.1UF, 10%6.3V X5R 201

PEG_R2D_P<0>	AA38	PCIE_RX0P	PEG_R2D_N<0>	Y37	PCIE_RX0N	PEG_R2D_P<1>	Y35	PCIE_RX1P	PEG_R2D_N<1>	W36	PCIE_RX1N	PEG_R2D_P<2>	W38	PCIE_RX2P	PEG_R2D_N<2>	V37	PCIE_RX2N
PEG_R2D_P<3>	V35	PCIE_RX3P	PEG_R2D_N<3>	U36	PCIE_RX3N	PEG_R2D_P<4>	U38	PCIE_RX4P	PEG_R2D_N<4>	T37	PCIE_RX4N	PEG_R2D_P<5>	T35	PCIE_RX5P	PEG_R2D_N<5>	R36	PCIE_RX5N
PEG_R2D_P<6>	R38	PCIE_RX6P	PEG_R2D_N<6>	P37	PCIE_RX6N	PEG_R2D_P<7>	P35	PCIE_RX7P	PEG_R2D_N<7>	N36	PCIE_RX7N						

NC	N38	PCIE_RX8P	NC	M37	PCIE_RX8N	NC	M35	PCIE_RX9P	NC	L36	PCIE_RX9N	NC	L38	PCIE_RX10P	NC	K37	PCIE_RX10N
NC	K35	PCIE_RX11P	NC	J36	PCIE_RX11N	NC	J38	PCIE_RX12P	NC	H37	PCIE_RX12N	NC	H35	PCIE_RX13P	NC	G36	PCIE_RX13N
NC	G38	PCIE_RX14P	NC	F37	PCIE_RX14N	NC	F35	PCIE_RX15P	NC	E37	PCIE_RX15N						

PCIE_TX0P	Y33	PEG_D2R_C_P<0>	PCIE_TX0N	Y32	PEG_D2R_C_N<0>	PCIE_TX1P	W33	PEG_D2R_C_P<1>	PCIE_TX1N	W32	PEG_D2R_C_N<1>	PCIE_TX2P	U33	PEG_D2R_C_P<2>	PCIE_TX2N	U32	PEG_D2R_C_N<2>
PCIE_TX3P	U30	PEG_D2R_C_P<3>	PCIE_TX3N	U29	PEG_D2R_C_N<3>	PCIE_TX4P	T33	PEG_D2R_C_P<4>	PCIE_TX4N	T32	PEG_D2R_C_N<4>	PCIE_TX5P	T30	PEG_D2R_C_P<5>	PCIE_TX5N	T29	PEG_D2R_C_N<5>
PCIE_TX6P	P33	PEG_D2R_C_P<6>	PCIE_TX6N	P32	PEG_D2R_C_N<6>	PCIE_TX7P	P30	PEG_D2R_C_P<7>	PCIE_TX7N	P29	PEG_D2R_C_N<7>						

PCIE_TX8P	N33	NC	PCIE_TX8N	N32	NC	PCIE_TX9P	N30	NC	PCIE_TX9N	N29	NC	PCIE_TX10P	L33	NC	PCIE_TX10N	L32	NC
PCIE_TX11P	L30	NC	PCIE_TX11N	L29	NC	PCIE_TX12P	K33	NC	PCIE_TX12N	K32	NC	PCIE_TX13P	J33	NC	PCIE_TX13N	J32	NC
PCIE_TX14P	K30	NC	PCIE_TX14N	K29	NC	PCIE_TX15P	H33	NC	PCIE_TX15N	H32	NC						

U8000
FCBGA
(1 OF 9)
PCIE
WHISTLER
40NM-ES
OMIT

PEG_CLK100M_P	AB35	PCIE_REFCLKP	PEG_CLK100M_N	AA36	PCIE_REFCLKN	GPU_PWRGOOD	AH16	PWRGOOD								
PCIE_CALRP	Y30	PEG_CALRP	PCIE_CALRN	Y29	PEG_CALRN	EG_RESET_L	R8000	0	GPU_RESET_R_L	AA30	PERST*					

PM_ALL_GPU_PGOOD — R8003 NOSTUFF 0 5% 1/16W MF-LF 402 — R8004 10K 5% 1/16W MF-LF 402

R8001 2.0K 1% 1/10W MF-LF 402 — PP1V0_S0GPU_ISNS

R8002 1.27K 1% 1/16W MF-LF 402

SYNC_MASTER=K92_SUMA	SYNC_DATE=06/15/2010
PAGE TITLE: Whistler PCI-E	
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	REVISION:
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Page Notes

Power aliases required by this page:

- =PPVCORE_GPU
- =PP1V5R1V35_GPU_FB_VDDR1
- =PP1V8_GPU_VDD_CT
- =PP1V0_GPU_PLL
- =PP3V3_GPU_VDDR3
- =PP3V3_GPU_VDDR4
- =PP1V8_GPU_MEM_PLL
- =PP1V8_GPU_PLL
- =PP1V8_GPU_PCIE_VDDR
- =PP1V8_GPU_PCIE_VDDC

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

PP1V5_S0GPU_ISNS — TBD mA

C8100 10UF, C8101 10UF, C8102 10UF, C8103 10UF, C8104 10UF (20% 10V X5R 603)

C8105 1UF, C8106 1UF, C8107 1UF, C8108 1UF, C8109 1UF, C8110 1UF, C8111 1UF, C8112 1UF, C8113 1UF, C8114 1UF (10% 25V X5R 402)

C8115 0.1UF, C8116 0.1UF, C8117 0.1UF, C8118 0.1UF, C8119 0.1UF, C8120 0.1UF, C8121 0.1UF, C8122 0.1UF, C8123 0.1UF, C8124 0.1UF (10% 6.3V X5R 201)

PP1V8_S0GPU_ISNS — L8120 120OHM-0.3A (0402) CRITICAL — PP1V8_GPU_VDD_CT — 219mA

MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

C8125 10UF, C8126 1UF, C8127 1UF, C8128 1UF, C8129 0.1UF

PP1V0_S0GPU_ISNS — L8130 470OHM-1A-150MOHM (0603) CRITICAL — PP1V0_GPU_PLL

MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1V

C8130 10UF, C8131 1UF, C8132 0.1UF

GND_GPU_PLL

PP3V3_S0GPU — 60 mA

C8133 10UF, C8134 1UF, C8135 1UF, C8136 1UF

PP1V8_S0GPU_ISNS — L8131 4700HM-1A-150MOHM (0603) CRITICAL — PP1V8_GPU_MEM_PLL

MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

C8137 10UF, C8138 1UF, C8139 1UF, C8140 0.1UF, C8141 0.1UF

PP1V8_S0GPU_ISNS — L8132 120OHM-0.3A (0402) CRITICAL — PP1V8_GPU_PLL — 150mA

MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

C8142 10UF, C8143 1UF, C8144 0.1UF

XW8100 SM

PP1V8_S0GPU_ISNS — L8140 FERR-220-OHM-2A (0603) CRITICAL — PP1V8_GPU_PCIE_VDDR — 504mA

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

C8145 10UF, C8146 1UF, C8147 1UF, C8148 1UF, C8149 0.1UF, C8150 0.1UF

PP1V0_S0GPU_ISNS — L8155 FERR-120-OHM-3A (0603) CRITICAL — PP1V0_GPU_PCIE_VDDC — 1920mA

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1V

C8151 10UF, C8152 1UF, C8153 1UF, C8154 1UF, C8155 1UF, C8156 1UF, C8157 1UF, C8158 1UF

U8000 WHISTLER 40NM-ES FCBGA (7 OF 9)

MEM I/O

AC7	VDDR1_AC7
AD11	VDDR1_AD11
AF7	VDDR1_AF7
AG10	VDDR1_AG10
AJ7	VDDR1_AJ7
AK8	VDDR1_AK8
AL9	VDDR1_AL9
G11	VDDR1_G11
G14	VDDR1_G14
G17	VDDR1_G17
G20	VDDR1_G20
G23	VDDR1_G23
G26	VDDR1_G26
G29	VDDR1_G29
H10	VDDR1_H10
J7	VDDR1_J7
J9	VDDR1_J9
K8	VDDR1_K8
K11	VDDR1_K11
K13	VDDR1_K13
L7	VDDR1_L7
L12	VDDR1_L12
L16	VDDR1_L16
L21	VDDR1_L21
L23	VDDR1_L23
L26	VDDR1_L26
M11	VDDR1_M11
N11	VDDR1_N11
P7	VDDR1_P7
R11	VDDR1_R11
U7	VDDR1_U7
U11	VDDR1_U11
Y7	VDDR1_Y7
Y11	VDDR1_Y11

OMIT

CORE

AF26	VDD_CT_AF26
AF27	VDD_CT_AF27
AG26	VDD_CT_AG26
AG27	VDD_CT_AG27

LEVEL TRNSL

AF23	VDDR3_AF23
AF24	VDDR3_AF24
AG23	VDDR3_AG23
AG24	VDDR3_AG24

I/O

AF13	VDDR4_AF13
AF15	VDDR4_AF15
AG13	VDDR4_AG13
AG15	VDDR4_AG15

PP1V8_GPU_VDDR4 — TBD mA

AD12	VDDR4_AD12
AF11	VDDR4_AF11
AF12	VDDR4_AF12
AG11	VDDR4_AG11

NC	M20 NC/VDDRHA
NC	M21 NC/VSSRHA
NC	U12 NC/VSSRHB
NC	V12 NC/VDDRHB

H7	MPV18_H7
H8	MPV18_H8

PLL

AM10	SPV18
AN9	SPV10
AN10	SPVSS

VOLT SENSE

AF28	FB_VDDC
NC	AG28 FB_VDDCI
AH29	FB_GND

GPU_VDD_SENSE (OUT)

GPU_GND_SENSE (OUT)

PCIE ISOLATED CORE I/O

AA31	PCIE_VDDR_AA31
AA32	PCIE_VDDR_AA32
AA33	PCIE_VDDR_AA33
AA34	PCIE_VDDR_AA34
AB37	PCIE_VDDR_AB37
V28	PCIE_VDDR_V28
W29	PCIE_VDDR_W29
W30	PCIE_VDDR_W30
Y31	PCIE_VDDR_Y31
G30	PCIE_VDDC_G30
G31	PCIE_VDDC_G31
H29	PCIE_VDDC_H29
H30	PCIE_VDDC_H30
J29	PCIE_VDDC_J29
J30	PCIE_VDDC_J30
L28	PCIE_VDDC_L28
M28	PCIE_VDDC_M28
N28	PCIE_VDDC_N28
R28	PCIE_VDDC_R28
T28	PCIE_VDDC_T28
U28	PCIE_VDDC_U28

CRITICAL L8150 120OHM-0.3A (0402)

PP1V8_S0GPU_ISNS — PP1V8_GPU_VDDR4

MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

C81C0 1UF, C81C1 0.1UF

PPVCORE_GPU

VDDC_AA15	AA15
VDDC_AA17	AA17
VDDC_AA20	AA20
VDDC_AA22	AA22
VDDC_AA24	AA24
VDDC_AA27	AA27
VDDC_AB16	AB16
VDDC_AB18	AB18
VDDC_AB21	AB21
VDDC_AB23	AB23
VDDC_AB26	AB26
VDDC_AB28	AB28
VDDC_AC17	AC17
VDDC_AC20	AC20
VDDC_AC22	AC22
VDDC_AC24	AC24
VDDC_AC27	AC27
VDDC_AD18	AD18
VDDC_AD21	AD21
VDDC_AD23	AD23
VDDC_AD26	AD26
VDDC_AF17	AF17
VDDC_AF20	AF20
VDDC_AF22	AF22
VDDC_AG16	AG16
VDDC_AG18	AG18
VDDC_AG21	AG21
VDDC_AH22	AH22
VDDC_AH27	AH27
VDDC_AH28	AH28
VDDC_M26	M26
VDDC_N24	N24
BIF_VDDC_N27	N27
VDDC_R18	R18
VDDC_R21	R21
VDDC_R23	R23
VDDC_R26	R26
VDDC_T17	T17
VDDC_T20	T20
VDDC_T22	T22
VDDC_T24	T24
BIF_VDDC_T27	T27
VDDC_U16	U16
VDDC_U18	U18
VDDC_U21	U21
VDDC_U23	U23
VDDC_U26	U26
VDDC_V17	V17
VDDC_V20	V20
VDDC_V22	V22
VDDC_V24	V24
VDDC_V27	V27
VDDC_Y16	Y16
VDDC_Y18	Y18
VDDC_Y21	Y21
VDDC_Y23	Y23
VDDC_Y26	Y26
VDDC_Y28	Y28

C8160 1UF, C8161 1UF, C8162 1UF, C8163 1UF, C8164 1UF, C8165 1UF, C8166 1UF, C8167 1UF, C8168 1UF, C8169 1UF (10% 25V X5R 402)

C8170 1UF, C8171 1UF, C8172 1UF, C8173 1UF, C8174 1UF, C8175 1UF, C8176 1UF, C8177 1UF, C8178 1UF, C8179 1UF (10% 25V X5R 402)

C8180 1UF, C8181 1UF, C8182 1UF, C8183 1UF, C8184 1UF, C8185 1UF, C8186 1UF, C8187 1UF, C8188 1UF, C8189 1UF (10% 25V X5R 402)

C8190 10UF, C8191 10UF, C8192 10UF, C8193 10UF, C8194 10UF, C8195 10UF, C8196 10UF, C8197 10UF, C8198 10UF, C8199 10UF (20% 10V X5R 603)

VDDCI_AA13	AA13
VDDCI_AB13	AB13
VDDCI_AC12	AC12
VDDCI_AC15	AC15
VDDCI_AD13	AD13
VDDCI_AD16	AD16
VDDCI_M15	M15
VDDCI_M16	M16
VDDCI_M18	M18
VDDCI_M23	M23
VDDCI_N13	N13
VDDCI_N15	N15
VDDCI_N17	N17
VDDCI_N20	N20
VDDCI_N22	N22
VDDCI_R12	R12
VDDCI_R13	R13
VDDCI_R16	R16
VDDCI_T12	T12
VDDCI_T15	T15
VDDCI_V15	V15
VDDCI_Y13	Y13

C81A0 1UF, C81A1 1UF, C81A2 1UF, C81A3 1UF, C81A4 1UF, C81A5 1UF, C81A6 1UF, C81A7 1UF, C81A8 1UF, C81A9 1UF (10% 25V X5R 402)

C81B0 10UF, C81B1 10UF, C81B2 10UF (20% 10V X5R 603)

SYNC_MASTER=K92_SUMA SYNC_DATE=06/15/2010
PAGE TITLE: Whistler CORE/FB POWER

Apple Inc.

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REVISION
BRANCH
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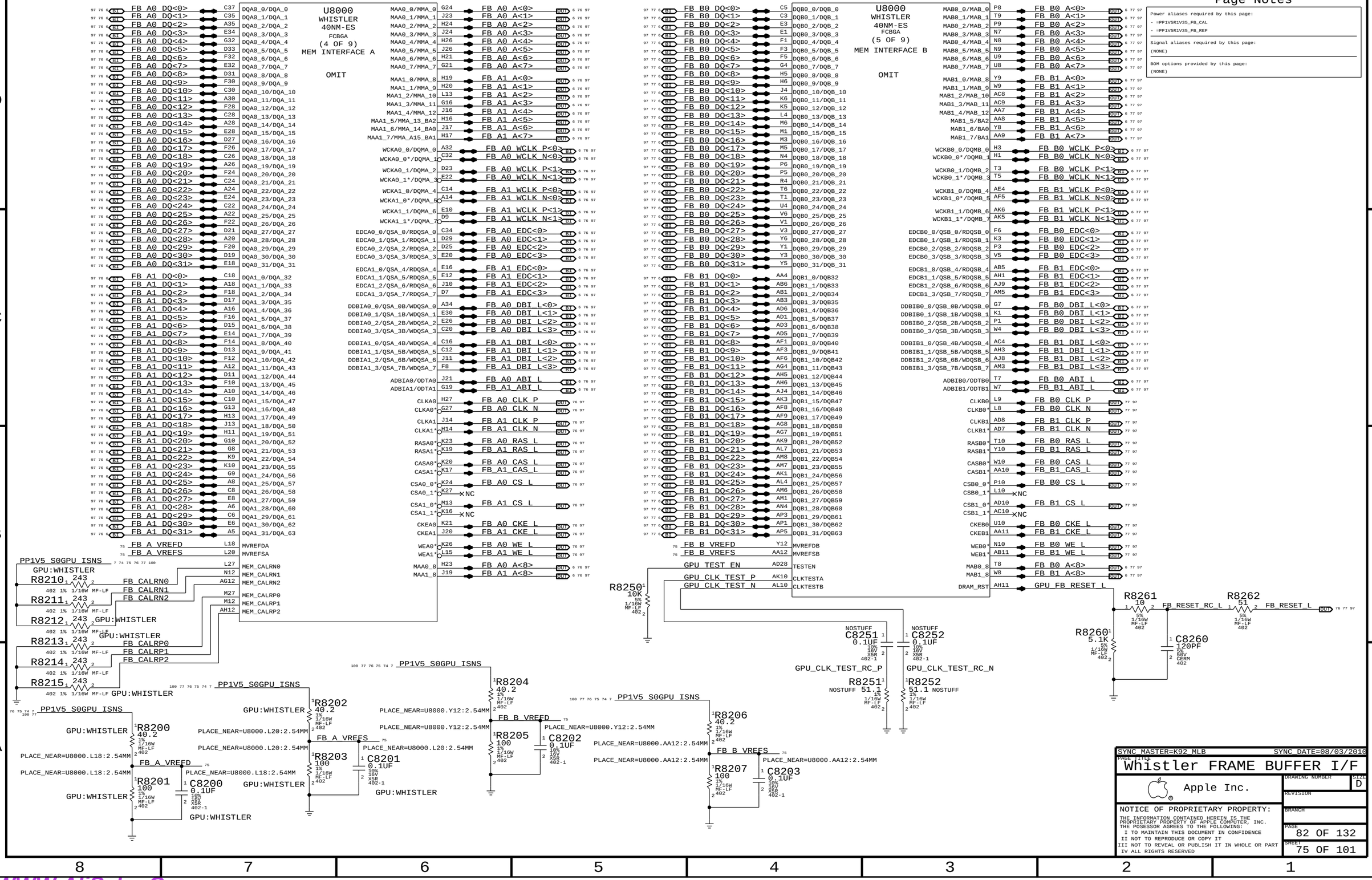
SHEET 74 OF 101



Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
GPU:WHISTLER is the BOM option called out on all Rs and Cs on this page

GPU:WHISTLER is the BOM option called out on ALL Rs and Cs on this page!

U8400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT

U8450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT

U8400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT

U8450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT

SYNC_MASTER=K92_MLB	SYNC_DATE=08/19/2010
PAGE TITLE	GDDR5 Frame Buffer A
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Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT

U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT

U8550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT

U8550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT

PP1V5_S0GPU_ISNS

FB_B0_VREFC
FB_B0_VREFD1
FB_B0_VREFD2

FB_B1_VREFC
FB_B1_VREFD1
FB_B1_VREFD2

SYNC_MASTER=K92_MLB
SYNC_DATE=08/19/2016

PAGE TITLE: GDDR5 Frame Buffer B

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VRAM BOM OPTION TABLE

	VRAM_DVP0 (STUFF R8613?)	VRAM_DVP1 (STUFF R8612?)	VRAM_DVP2 (STUFF R8611?)
K92 SAMSUNG 1G	NO	NO	YES
K92 HYNIX 1G	YES	NO	YES
K91F SAMSUNG 512M	NO	NO	NO
K91F HYNIX 512M	NO	YES	NO
K91F SAMSUNG 1G	YES	NO	NO
K91F HYNIX 1G	YES	YES	NO

NOTE: AMD STRAPS FOR IDENTIFYING VRAM VENDOR & SIZE FOR WHISTLER

K92 Samsung 1G - NOSTUFF R8613, NOSTUFF R8612, STUFF R8611
K92 Hynix 1G - STUFF R8613, NOSTUFF R8612, STUFF R8611

K91FSamsung 512M - NOSTUFF R8613, NOSTUFF R8612, NOSTUFF R8611
K91FHynix 512M - NOSTUFF R8613, STUFF R8612, NOSTUFF R8611
K91FSamsung 1G - STUFF R8613, NOSTUFF R8612, NOSTUFF R8611
K91FHynix 1G - STUFF R8613, STUFF R8612, NOSTUFF R8611

NO STRAP CHANGES ARE REQUIRED FOR SEYMOUR BASED SYSTEMS

PP1V8_S0GPU_ISNS — R8610 10K 5% 1/16W MF-LF 402 (NOSTUFF) — R8611 10K (VRAM_DVP2) — R8612 10K (VRAM_DVP1) — R8613 10K (VRAM_DVP0)

PP3V3_S0GPU — R8600 4.7K 5% 1/16W MF-LF 402 — R8601 4.7K 5% 1/16W MF-LF 402

PP1V8_S0GPU_ISNS — R8602 499 1% 1/16W MF-LF 402 — C8600 0.1UF 10% 16V X5R 402-1 — R8603 249 1% 1/16W MF-LF 402

CRITICAL L8600 470OHM-1A-150MOHM 0603 — PP1V8_S0GPU_ISNS VOLTAGE=1.8V — C8601 10UF 20% 10V X5R 603 — C8602 1UF 10% 16V X5R 402 — C8603 0.1UF 10% 16V X5R 402-1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.8V

CRITICAL L8601 470OHM-1A-150MOHM 0603 — PP1V0_S0GPU_ISNS — C8604 10UF 20% 10V X5R 603 — C8605 1UF 10% 16V X5R 402 — C8606 0.1UF 10% 16V X5R 402-1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1V

XW8600 SM — GND_GPU_DPLL — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

CRITICAL L8602 120OHM-0.3A 0402 — PP1V8_S0GPU_ISNS — C8607 10UF 20% 10V X5R 603 — C8608 1UF 10% 16V X5R 402 — C8609 0.1UF 10% 16V X5R 402-1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.8V

XW8601 SM — GND_GPU_TSVSS — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

U8000 WHISTLER 40NM-ES FCBGA (2 OF 9)

TP_DVPCNTL_M<0>	AR8	DVPCNTL_MVP_0	DPA
TP_DVPCNTL_M<1>	AU8	DVPCNTL_MVP_1	DPA
TP_DVPCNTL<0>	AP8	DVPCNTL_0	DPA
TP_DVPCNTL<1>	AW8	DVPCNTL_1	DPA
TP_DVPCNTL<2>	AR3	DVPCNTL_2	DPA
TP_DVPCLK	AR1	DVPCLK	DPA
DVPDATA<0>	AU1	DVPDATA_0	DPA
DVPDATA<1>	AU3	DVPDATA_1	DPA
DVPDATA<2>	AW3	DVPDATA_2	DPA
DVPDATA<3>	AP6	DVPDATA_3	DPA
TP_DVPDATA<4>	AW5	DVPDATA_4	DPA
TP_DVPDATA<5>	AU5	DVPDATA_5	DPA
TP_DVPDATA<6>	AR6	DVPDATA_6	DPA
TP_DVPDATA<7>	AW6	DVPDATA_7	DPA
TP_DVPDATA<8>	AU6	DVPDATA_8	DPA
TP_DVPDATA<9>	AT7	DVPDATA_9	DPA
TP_DVPDATA<10>	AV7	DVPDATA_10	DPA
TP_DVPDATA<11>	AN7	DVPDATA_11	DPA
TP_DVPDATA<12>	AV9	DVPDATA_12	DPA
TP_DVPDATA<13>	AT9	DVPDATA_13	DPA
TP_DVPDATA<14>	AR10	DVPDATA_14	DPA
TP_DVPDATA<15>	AW10	DVPDATA_15	DPA
TP_DVPDATA<16>	AU10	DVPDATA_16	DPA
TP_DVPDATA<17>	AP10	DVPDATA_17	DPA
TP_DVPDATA<18>	AV11	DVPDATA_18	DPA
TP_DVPDATA<19>	AT11	DVPDATA_19	DPA
TP_DVPDATA<20>	AR12	DVPDATA_20	DPA
TP_DVPDATA<21>	AW12	DVPDATA_21	DPA
TP_DVPDATA<22>	AU12	DVPDATA_22	DPA
TP_DVPDATA<23>	AP12	DVPDATA_23	DPA
NC	AJ21	SWAPLOCKA	MULTI GFX
NC	AK21	SWAPLOCKB	MULTI GFX
GPU_I2C_SCL	AK26	SCL	I2C
GPU_I2C_SDA	AJ26	SDA	I2C
GPU_PCIE_TX_PWR	AH20	GPIO_0	DPD
GPU_GPIO_TX_DEEMP	AH18	GPIO_1	DPD
GPU_PCIE_GEN2	AN16	GPIO_2	DPD
GPU_SMB_DAT	AH23	GPIO_3_SMBDATA	DPD
GPU_SMB_CLK	AJ23	GPIO_4_SMBCLK	DPD
GPU_AC_BATT	AH17	GPIO_5_AC_BATT	DPD
GPU_VCORE_VID0	AJ17	GPIO_6	DPD
EG_BKLT_EN	AK17	GPIO_7_BLON	DPD
GPU_ROM_SO	AJ13	GPIO_8_ROMSO	DPD
GPU_ROM_SI	AH15	GPIO_9_ROMSI	DPD
GPU_ROM_SCLK	AJ16	GPIO_10_ROMSCK	DPD
GPU_CONFIG_0	AK16	GPIO_11	DPD
GPU_CONFIG_1	AL16	GPIO_12	DPD
GPU_CONFIG_2	AM16	GPIO_13	DPD
DP_T29SNK0_HPD_GPU	AM14	GPIO_14_HPD2	DPD
GPU_VCORE_VID1	AM13	GPIO_15_PWRCNTL_0	DPD
GPU_VCORE_VID2	AK14	GPIO_16	DPD
SMC_GFX_THROTTLE_R_L	AG30	GPIO_17_THERMAL_INT	DPD
DP_T29SNK1_HPD_GPU	AN14	GPIO_18_HPD3	DPD
SMC_GFX_OVERTEMP_R_L	AM17	GPIO_19_CTF	DPD
GPU_VCORE_VID3	AL13	GPIO_20_PWRCNTL_1	DPD
FBVDD_ALTVO	AJ14	GPIO_21_BB_EN	DPD
GPU_ROM_CS_L	AK13	GPIO_22_ROMCS*	DPD
PEX_CLKREQ_L_R	AN13	GPIO_23_CLKREQ*	DPD
TP_GPU_JTAG_TRST_L	AM23	JTAG_TRST*	GPIO
TP_GPU_JTAG_TDI	AN23	JTAG_TDI	GPIO
TP_GPU_JTAG_TCK	AK23	JTAG_TCK	GPIO
TP_GPU_JTAG_TMS	AL24	JTAG_TMS	GPIO
TP_GPU_JTAG_TDO	AM24	JTAG_TDO	GPIO
NC_GPU_GENERICA	AJ19	GENERICA	GPIO
NC_GPU_GENERICB	AK19	GENERICB	GPIO
NC_GPU_GENERICC	AJ20	GENERICC	GPIO
DP_CA_DET_EG_R	AK20	GENERICD	GPIO
NC_GPU_GENERICE	AJ24	GENERICE_HPD4	GPIO
NC_GPU_GENERICF	AH26	GENERICF_HPD5	GPIO
NC_GPU_GENERICG	AH24	GENERICG_HPD6	GPIO
DP_EG_HPD	AK24	HPD1	GPIO
GPU_VREFG	AH13	VREFG	PLL/CLK
PP1V8_GPU_DPLL 75mA (GND_GPU_DPLL)	AM32	DPLL_PVDD	PLL/CLK
	AN32	DPLL_PVSS	PLL/CLK
PP1V0_GPU_DPLL 125mA	AN31	DPLL_VDDC	PLL/CLK
NC	AV33	XTALIN	PLL/CLK
NC	AU34	XTALOUT	PLL/CLK
GPU_CLK27M	AW34	XO_IN	PLL/CLK
GPU_CLK100M	AW35	XO_IN2	PLL/CLK
GPU_TDIODE_P	AF29	DPLUS	THERMAL
GPU_TDIODE_N	AG29	DMINUS	THERMAL
NC	AK32	TS_FDO	THERMAL
NC	AL31	TSA/NC	THERMAL
PP1V8_GPU_TSVDD 20mA (GND_GPU_TSVSS)	AJ32	TSVDD	DDC/AUX
	AJ33	TSVSS	DDC/AUX

OMIT

TXCAP_DPA3P	AU24	DP_EXTA_ML_C_P<3>	DAC2
TXCAM_DPA3N	AV23	DP_EXTA_ML_C_N<3>	DAC2
TX0P_DPA2P	AT25	DP_EXTA_ML_C_P<2>	DAC2
TX0M_DPA2N	AR24	DP_EXTA_ML_C_N<2>	DAC2
TX1P_DPA1P	AU26	DP_EXTA_ML_C_P<1>	DAC2
TX1M_DPA1N	AV25	DP_EXTA_ML_C_N<1>	DAC2
TX2P_DPA0P	AT27	DP_EXTA_ML_C_P<0>	DAC2
TX2M_DPA0N	AR26	DP_EXTA_ML_C_N<0>	DAC2
TXCBP_DPB3P	AR30	DP_T29SNK0_ML_C_P<3>	DPB
TXCBM_DPB3N	AT29	DP_T29SNK0_ML_C_N<3>	DPB
TX3P_DPB2P	AV31	DP_T29SNK0_ML_C_P<2>	DPB
TX3M_DPB2N	AU30	DP_T29SNK0_ML_C_N<2>	DPB
TX4P_DPB1P	AR32	DP_T29SNK0_ML_C_P<1>	DPB
TX4M_DPB1N	AT31	DP_T29SNK0_ML_C_N<1>	DPB
TX5P_DPB0P	AT33	DP_T29SNK0_ML_C_P<0>	DPB
TX5M_DPB0N	AU32	DP_T29SNK0_ML_C_N<0>	DPB
TXCCP_DPC3P	AU14	DP_T29SNK1_ML_C_P<3>	DPC
TXCCM_DPC3N	AV13	DP_T29SNK1_ML_C_N<3>	DPC
TX0P_DPC2P	AT15	DP_T29SNK1_ML_C_P<2>	DPC
TX0M_DPC2N	AR14	DP_T29SNK1_ML_C_N<2>	DPC
TX1P_DPC1P	AU16	DP_T29SNK1_ML_C_P<1>	DPC
TX1M_DPC1N	AV15	DP_T29SNK1_ML_C_N<1>	DPC
TX2P_DPC0P	AT17	DP_T29SNK1_ML_C_P<0>	DPC
TX2M_DPC0N	AR16	DP_T29SNK1_ML_C_N<0>	DPC
TXCDP_DPD3P	AU20	NC	DPD
TXCDM_DPD3N	AT19	NC	DPD
TX3P_DPD2P	AT21	NC	DPD
TX3M_DPD2N	AR20	NC	DPD
TX4P_DPD1P	AU22	NC	DPD
TX4M_DPD1N	AV21	NC	DPD
TX5P_DPD0P	AT23	NC	DPD
TX5M_DPD0N	AR22	NC	DPD
R	AD39	NC	DAC1
R*	AD37	NC	DAC1
G	AE36	NC	DAC1
G*	AD35	NC	DAC1
B	AF37	NC	DAC1
B*	AE38	NC	DAC1
HSYNC	AC36	GPU_AUD_1	DAC1
VSYNC	AC38	GPU_AUD_0	DAC1
RSET	AB34	NC	DAC1
AVDD	AD34	PP1V8_S0GPU_ISNS	DAC1
AVSSQ	AE34		DAC1
VDD1DI	AC33		DAC1
VSS1DI	AC34		DAC1
R2/NC	AC30	NC	DAC2
R2*/NC	AC31	NC	DAC2
G2/NC	AD30	NC	DAC2
G2*/NC	AD31	NC	DAC2
B2/NC	AF30	NC	DAC2
B2*/NC	AF31	NC	DAC2
C/NC	AC32	NC	DAC2
Y/NC	AD32	NC	DAC2
COMP/NC	AF32	NC	DAC2
H2SYNC/GENLK_CLK	AD29	NC	DAC2
V2SYNC/GENLK_VSYNC	AC29	NC	DAC2
VDD2DI/NC	AG31	NC	DAC2
VSS2DI/NC	AG32	NC	DAC2
A2VDD/NC	AG33	NC	DAC2
A2VDDQ/NC	AD33	NC	DAC2
A2VSSQ/TSVSSQ	AF33	GND_GPU_TVSSQ	DAC2
R2SET/NC	AA29	NC	DAC2
DDC1CLK	AM26	DP_EG_DDC_CLK	DDC/AUX
DDC1DATA	AM26	DP_EG_DDC_DATA	DDC/AUX
AUX1P	AM27	DP_EG_AUXCH_P	DDC/AUX
AUX1N	AL27	DP_EG_AUXCH_N	DDC/AUX
DDC2CLK	AM19	NC	DDC/AUX
DDC2DATA	AL19	NC	DDC/AUX
AUX2P	AN20	DP_T29SNK0_AUXCH_C_P	DDC/AUX
AUX2N	AM20	DP_T29SNK0_AUXCH_C_N	DDC/AUX
DDCCLK_AUX3P	AL30	DP_T29SNK1_AUXCH_C_P	DDC/AUX
DDCDATA_AUX3N	AM30	DP_T29SNK1_AUXCH_C_N	DDC/AUX
DDCCLK_AUX4P	AL29	NC	DDC/AUX
DDCDATA_AUX4N	AM29	NC	DDC/AUX
DDCCLK_AUX5P	AN21	LVDS_EG_DDC_CLK	DDC/AUX
DDCDATA_AUX5N	AM21	LVDS_EG_DDC_DATA	DDC/AUX
DDC6CLK	AJ30	NC	DDC/AUX
DDC6DATA	AJ31	NC	DDC/AUX
DDCCLK_AUX7P	AK30	NC	DDC/AUX
DDCDATA_AUX7N	AK29	NC	DDC/AUX

XW8602 SM — GND_GPU_TVSSQ — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

PP3V3_S0GPU — Straps for audio on DP and HDMI — R8604 10K 5% 1/16W MF-LF 402 — R8605 10K 5% 1/16W MF-LF 402

U8000 WHISTLER 40NM-ES FCBGA (3 OF 9) LVDS CNTL

VARY_BL	AK27	LVDS_EG_BLK_PWM	LVTMDP
DIGON	AJ27	EG_LCD_PWR_EN	LVTMDP
TXCLK_UP_DPF3P	AK35	NC_LVDS_EG_B_CLK_P	LVTMDP
TXCLK_UN_DPF3N	AL36	NC_LVDS_EG_B_CLK_N	LVTMDP
TXOUT_U0P_DPF2P	AJ38	LVDS_EG_B_DATA_P<0>	LVTMDP
TXOUT_U0N_DPF2N	AK37	LVDS_EG_B_DATA_N<0>	LVTMDP
TXOUT_U1P_DPF1P	AH35	LVDS_EG_B_DATA_P<1>	LVTMDP
TXOUT_U1N_DPF1N	AJ36	LVDS_EG_B_DATA_N<1>	LVTMDP
TXOUT_U2P_DPF0P	AG38	LVDS_EG_B_DATA_P<2>	LVTMDP
TXOUT_U2N_DPF0N	AH37	LVDS_EG_B_DATA_N<2>	LVTMDP
TXOUT_U3P	AF35	NC_LVDS_EG_B_DATA_P<3>	LVTMDP
TXOUT_U3N	AG36	NC_LVDS_EG_B_DATA_N<3>	LVTMDP
TXCLK_LP_DPE3P	AP34	LVDS_EG_A_CLK_P	LVTMDP
TXCLK_LN_DPE3N	AR34	LVDS_EG_A_CLK_N	LVTMDP
TXOUT_L0P_DPE2P	AW37	LVDS_EG_A_DATA_P<0>	LVTMDP
TXOUT_L0N_DPE2N	AU35	LVDS_EG_A_DATA_N<0>	LVTMDP
TXOUT_L1P_DPE1P	AR37	LVDS_EG_A_DATA_P<1>	LVTMDP
TXOUT_L1N_DPE1N	AU39	LVDS_EG_A_DATA_N<1>	LVTMDP
TXOUT_L2P_DPE0P	AP35	LVDS_EG_A_DATA_P<2>	LVTMDP
TXOUT_L2N_DPE0N	AR35	LVDS_EG_A_DATA_N<2>	LVTMDP
TXOUT_L3P	AN36	NC_LVDS_EG_A_DATA_P<3>	LVTMDP
TXOUT_L3N	AP37	NC_LVDS_EG_A_DATA_N<3>	LVTMDP

R8606 10K 5% 1/16W MF-LF 402

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_I2C
- =PP1V8_GPU_VREFG
- =PP1V8_GPU_DPLL
- =PP1V8_GPU_DPLL
- =PP1V0_GPU_DPLL
- =PP1V0_GPU_TS

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=K92_MLB SYNC_DATE=12/01/2010

PAGE TITLE: Whistler LVDS/DP/GPIO

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GPIOs

GPU_PCIE_TX_PWR	GP	GPU_PCIE_TX_PWR	MAKE_BASE=TRUE
GPU_GPIO_TX_DEEMP	GP	GPU_GPIO_TX_DEEMP	MAKE_BASE=TRUE
GPU_PCIE_GEN2	GP	GPU_PCIE_GEN2	MAKE_BASE=TRUE
GPU_SMB_DAT	GP	GPU_SMB_DAT	MAKE_BASE=TRUE
GPU_SMB_CLK	GP	GPU_SMB_CLK	MAKE_BASE=TRUE
GPU_AC_BATT	GP	GPU_AC_BATT	MAKE_BASE=TRUE
GPU_VCORE_VID0	GP	GPU_VCORE_VID0	MAKE_BASE=TRUE
EG_BKLT_EN	GP	EG_BKLT_EN	MAKE_BASE=TRUE
GPU_ROM_SO	GP	GPU_ROM_SO	MAKE_BASE=TRUE
GPU_ROM_SI	GP	GPU_ROM_SI	MAKE_BASE=TRUE
GPU_ROM_SCLK	GP	GPU_ROM_SCLK	MAKE_BASE=TRUE
GPU_CONFIG_0	GP	GPU_CONFIG_0	MAKE_BASE=TRUE
GPU_CONFIG_1	GP	GPU_CONFIG_1	MAKE_BASE=TRUE
GPU_CONFIG_2	GP	GPU_CONFIG_2	MAKE_BASE=TRUE
DP_T29SNK0_HPD_GPU	GP	DP_T29SNK0_HPD_GPU	MAKE_BASE=TRUE
GPU_VCORE_VID1	GP	GPU_VCORE_VID1	MAKE_BASE=TRUE

GPIOs

GPU_VCORE_VID2	GP	GPU_VCORE_VID2	MAKE_BASE=TRUE
SMC_GFX_THROTTLE_R_L	GP	SMC_GFX_THROTTLE_R_L	MAKE_BASE=TRUE
DP_T29SNK1_HPD_GPU	GP	DP_T29SNK1_HPD_GPU	MAKE_BASE=TRUE
SMC_GFX_OVERTEMP_R_L	GP	SMC_GFX_OVERTEMP_R_L	MAKE_BASE=TRUE
GPU_VCORE_VID3	GP	GPU_VCORE_VID3	MAKE_BASE=TRUE
FBVDD_ALTVO	GP	FBVDD_ALTVO	MAKE_BASE=TRUE
GPU_ROM_CS_L	GP	GPU_ROM_CS_L	MAKE_BASE=TRUE
PEX_CLKREQ_L_R	GP	PEX_CLKREQ_L_R	MAKE_BASE=TRUE
NC_GPU_GENERICA	GP	NC_GPU_GENERICA	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICB	GP	NC_GPU_GENERICB	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICC	GP	NC_GPU_GENERICC	MAKE_BASE=TRUE NO_TEST=TRUE
DP_CA_DET_EG_R	GP	DP_CA_DET_EG_R	MAKE_BASE=TRUE
NC_GPU_GENERICE	GP	NC_GPU_GENERICE	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICF	GP	NC_GPU_GENERICF	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICG	GP	NC_GPU_GENERICG	MAKE_BASE=TRUE NO_TEST=TRUE
DP_EG_HPD	GP	DP_EG_HPD	MAKE_BASE=TRUE

T29 HPD GPU isolation

PP3V3_S0 — C8741 0.1UF 20% 10V CERM 402

CRITICAL U8741 74LVC2G08GT SOT833

DP_T29SNK0_HPD → U8741 A → U8741 B08 → DP_T29SNK0_HPD_GPU

PP3V3_GPU_VDD33_R — R8741 0 5% 1/16W MF-LF 402 — PP3V3_S0GPU

PP3V3_S0 — U8741 A

DP_T29SNK1_HPD → U8741 B08 → DP_T29SNK1_HPD_GPU

Unused signals

TP_GPU_JTAG_TCK	MAKE_BASE=TRUE	TP_GPU_JTAG_TCK	
TP_GPU_JTAG_TDI	MAKE_BASE=TRUE	TP_GPU_JTAG_TDI	
TP_GPU_JTAG_TDO	MAKE_BASE=TRUE	TP_GPU_JTAG_TDO	
TP_GPU_JTAG_TMS	MAKE_BASE=TRUE	TP_GPU_JTAG_TMS	
TP_GPU_JTAG_TRST_L	MAKE_BASE=TRUE	TP_GPU_JTAG_TRST_L	
NC_LVDS_EG_B_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_B_CLK_P	
NC_LVDS_EG_B_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_B_CLK_N	
NC_LVDS_EG_A_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_A_DATA_P<3>	
NC_LVDS_EG_A_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_A_DATA_N<3>	
NC_LVDS_EG_B_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_B_DATA_P<3>	
NC_LVDS_EG_B_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_B_DATA_N<3>	

Config Straps

PP3V3_S0GPU

R8700	NOSTUFF	10K 5% 1/16W MF-LF 402	GPU_PCIE_TX_PWR
R8701	NOSTUFF	10K 5% 1/16W MF-LF 402	GPU_GPIO_TX_DEEMP
R8702		10K 5% 1/16W MF-LF 402	GPU_PCIE_GEN2
R8703	NOSTUFF	10K 5% 1/16W MF-LF 402	GPU_SMB_DAT
R8704	NOSTUFF	10K 5% 1/16W MF-LF 402	GPU_SMB_CLK
R8705	NOSTUFF	10K 5% 1/16W MF-LF 402	GPU_AC_BATT
R8706	NOSTUFF	10K 5% 1/16W MF-LF 402	EG_BKLT_EN
R8707	NOSTUFF	10K 5% 1/16W MF-LF 402	GPU_ROM_SO
R8708	NOSTUFF	10K 5% 1/16W MF-LF 402	GPU_ROM_SI
R8709	NOSTUFF	10K 5% 1/16W MF-LF 402	GPU_ROM_SCLK
R8710		10K 5% 1/16W MF-LF 402	GPU_CONFIG_0
R8711	NOSTUFF	10K 5% 1/16W MF-LF 402	GPU_CONFIG_1
R8712	GPU_ROM:YES	10K 5% 1/16W MF-LF 402	GPU_CONFIG_2
R8713	NOSTUFF	10K 5% 1/16W MF-LF 402	FBVDD_ALTVO
R8714	NOSTUFF	10K 5% 1/16W MF-LF 402	PEX_CLKREQ_L_R

ISOLATION R's for GPU Int Temp Sense

GPU_SMB_DAT — R8780 NOSTUFF 0 5% 1/16W MF-LF 402 — SMBUS_SMC_0_S0_SDA

GPU_SMB_CLK — R8781 NOSTUFF 0 5% 1/16W MF-LF 402 — SMBUS_SMC_0_S0_SCL

PP3V3_S0GPU

R8723	GPU_ROM:YES	33 5% 1/16W MF-LF 402	GPU_ROM_SI
R8724	GPU_ROM:YES	33 5% 1/16W MF-LF 402	GPU_ROM_SCLK
R8725	GPU_ROM:YES	33 5% 1/16W MF-LF 402	GPU_ROM_CS_L
R8720	GPU_ROM:YES	10K 5% 1/16W MF-LF 402	GPU_ROM_SI_R
R8721		0 5% 1/16W MF-LF 402	GPU_ROM_CS_L_R
R8722	NO STUFF	0 5% 1/16W MF-LF 402	GPU_ROM_WP_L

U8701 M25P10A UFDFPN8 CRITICAL OMIT_TABLE — VCC, VSS, THRM PAD

C8721 0.1UF 20% 10V CERM 402 GPU_ROM:YES

GPU_ROM_SO_R — R8726 33 5% 1/16W MF-LF 402 GPU_ROM:YES — GPU_ROM_SO

PP3V3_S0 / PP3V3_S0GPU

R8750	NO STUFF	2.2K 5% 1/16W MF-LF 402	DP_EG_DDC_CLK
R8751	NO STUFF	2.2K 5% 1/16W MF-LF 402	DP_EG_DDC_DATA
R8752		4.7K 5% 1/16W MF-LF 402	DP_IG_DDC_CLK
R8753		4.7K 5% 1/16W MF-LF 402	DP_IG_DDC_DATA

PP3V3_S0GPU

R8796	NO STUFF	2.2K 5% 1/16W MF-LF 402	
R8797		2.2K 5% 1/16W MF-LF 402	
R8798		0 5% 1/16W MF-LF 402	SMC_GFX_OVERTEMP_L
R8799		0 5% 1/16W MF-LF 402	SMC_GFX_THROTTLE_L
R8792		10K 5% 1/16W MF-LF 402	
R8793		10K 5% 1/16W MF-LF 402	
R8794		10K 5% 1/16W MF-LF 402	

DP_CA_DET_EG_R	R8791 0 5% 1/16W MF-LF 402	DP_CA_DET_EG	IN
PEX_CLKREQ_L_R	R8795 0 5% 1/16W MF-LF 402	PEX_CLKREQ_L	OUT

EG_LCD_PWR_EN (OUT)

EG_BKLT_EN (OUT)

FBVDD_ALTVO (OUT)

PP3V3_S0GPU — L8703 1200OHM-0.3A 0402 — PP3V3_GPU_OSC_27M (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

L8702 1200OHM-0.3A 0402 — PP3V3_GPU_OSC_100M (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

C8702 0.1UF 10% 16V X5R 402-1

C8703 0.1UF 10% 16V X5R 402-1

GPU Reference Clocks

U8700 SL16010DC TDFN — VDD1, VDD2, XIN/CLKIN, XOUT, SSCLK, REFCLK, SSEL0, SSEL1, VSS1, VSS2, THM PAD

GPU_OSC_27M_XTALIN — GPU_OSC_27M_XTALOUT

CRITICAL Y8700 SM-2.5X2.0MM 27MHZ-15PPM-18PF

C8700 30PF 5% 50V CERM 402

C8701 30PF 5% 50V CERM 402

GPU_CLK100M_R	R8730 0 5% 1/16W MF-LF 402	GPU_CLK100M	OUT
GPU_CLK27M_R	R8731 0 5% 1/16W MF-LF 402	GPU_CLK27M	OUT

SYNC_MASTER=K92_MLB SYNC_DATE=11/23/2016

PAGE TITLE: Whistler GPIOs & STRAPs

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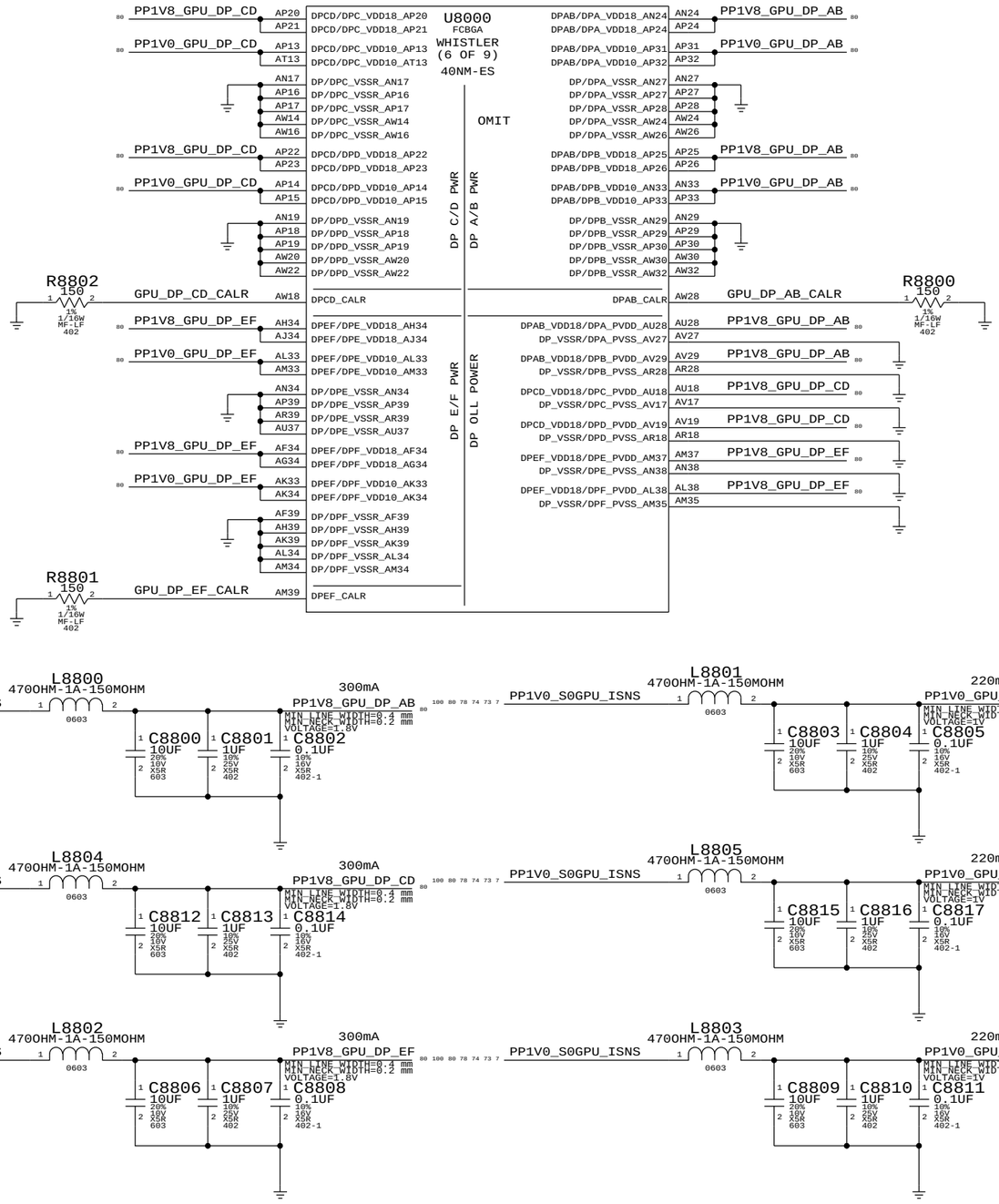

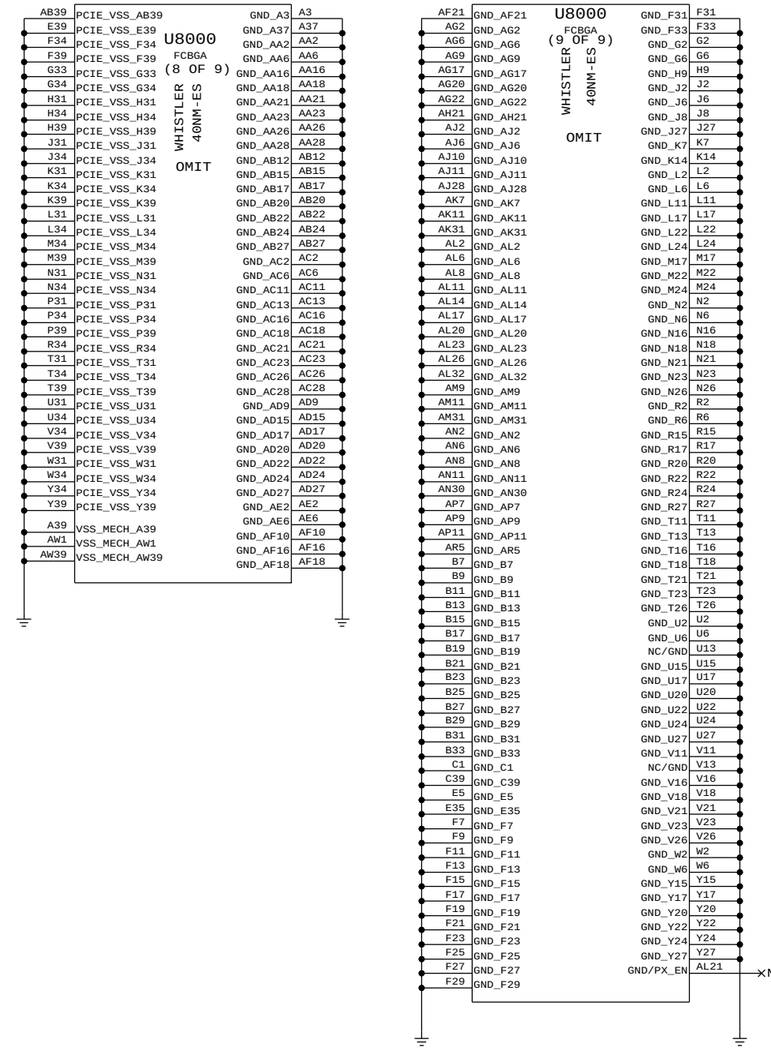

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_DP_AB
- =PP1V8_GPU_DP_CD
- =PP1V8_GPU_DP_EF
- =PP1V0_GPU_DP_AB
- =PP1V0_GPU_DP_CD
- =PP1V0_GPU_DP_EF

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=K92_SUMA SYNC_DATE=06/15/2010

PAGE TITLE: Whistler DP PWR/GNDs

Apple Inc.

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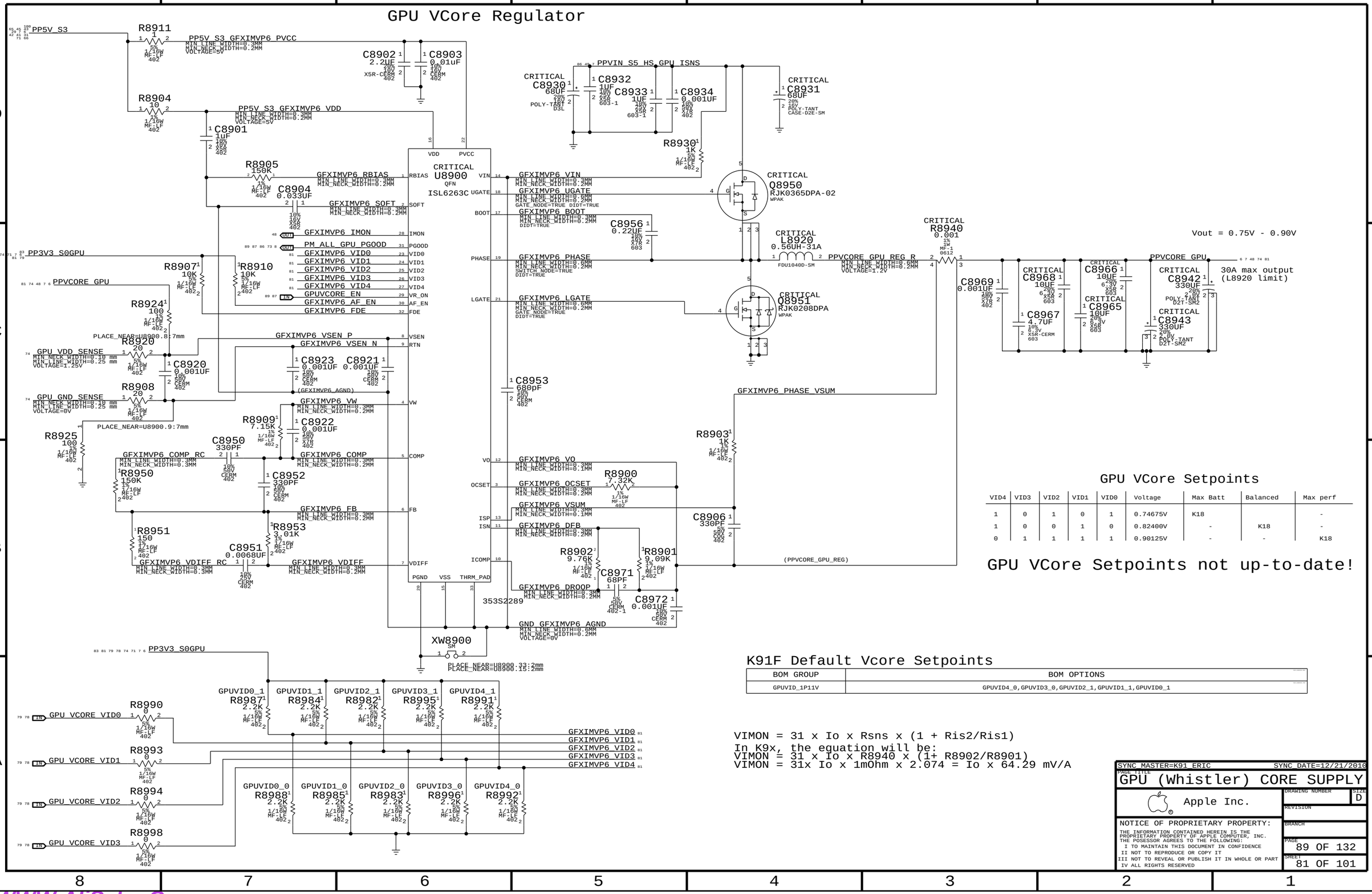
GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K18		-
1	0	0	1	0	0.82400V	-	K18	-
0	1	1	1	1	0.90125V	-	-	K18

GPU VCore Setpoints not up-to-date!

K91F Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P11V	GPUVID4_0,GPUVID3_0,GPUVID2_1,GPUVID1_1,GPUVID0_1

VIMON = 31 x Io x Rsns x (1 + Ris2/Ris1)
In K9x, the eqaution will be:
VIMON = 31 x Io x R8940 x (1+ R8902/R8901)
VIMON = 31x Io x 1mOhm x 2.074 = Io x 64.29 mV/A

SYNC_MASTER=K91_ERIC SYNC_DATE=12/21/2010

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GPU (Whistler) CORE SUPPLY

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LCD (LVDS) INTERFACE

LCD_PWR_EN

R9094 10K 5% 1/16W MF-LF 402

CRITICAL U9000 FPF1009 MFET-2X2
ON, VIN_1, VIN_2, VOUT_1, VOUT_2, GND, THRM PAD

PP3V3_S5

C9009 0.1UF 10% 16V X5R 402-1

C9011 0.1UF 10% 16V X5R 402-1

C9012 10UF 20% 6.3V X5R 603

CRITICAL L9000 FERR-250-OHM SM

PP3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

C9001 0.1UF 10% 16V X5R 402-1

C9002 0.001UF 10% 50V X7R 402

PP3V3_S0

R9010 100K 5% 1/16W MF-LF 402

R9011 100K 5% 1/16W MF-LF 402

100K pull-ups are for
no-panel case (development).
Panel has 2K pull-ups

LVDS_DDC_CLK
LVDS_DDC_DATA

C9010 0.001UF 10% 50V X7R 402

CRITICAL L9010 90-OHM-100MA DLP11S

LVDS_CONN_A_CLK_N
LVDS_CONN_A_CLK_P

Place close to the connector

CRITICAL L9011 90-OHM-100MA DLP11S

LVDS_CONN_B_CLK_N
LVDS_CONN_B_CLK_P

Place close to the connector

CRITICAL J9000 20474-040E-11 F-RT-SM

PP3V3_SW_LCD
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

NC

LVDS_CONN_A_DATA_N<0>
LVDS_CONN_A_DATA_P<0>
LVDS_CONN_A_DATA_N<1>
LVDS_CONN_A_DATA_P<1>
LVDS_CONN_A_DATA_N<2>
LVDS_CONN_A_DATA_P<2>
LVDS_CONN_A_CLK_F_N
LVDS_CONN_A_CLK_F_P
LVDS_CONN_B_DATA_N<0>
LVDS_CONN_B_DATA_P<0>
LVDS_CONN_B_DATA_N<1>
LVDS_CONN_B_DATA_P<1>
LVDS_CONN_B_DATA_N<2>
LVDS_CONN_B_DATA_P<2>
LVDS_CONN_B_CLK_F_N
LVDS_CONN_B_CLK_F_P
LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1

NC

PPVOUT_S0_LCDBKLT

C9000 0.001UF 10% 50V CERM 402

518S0651

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE
LVDS Display Connector

Apple Inc.

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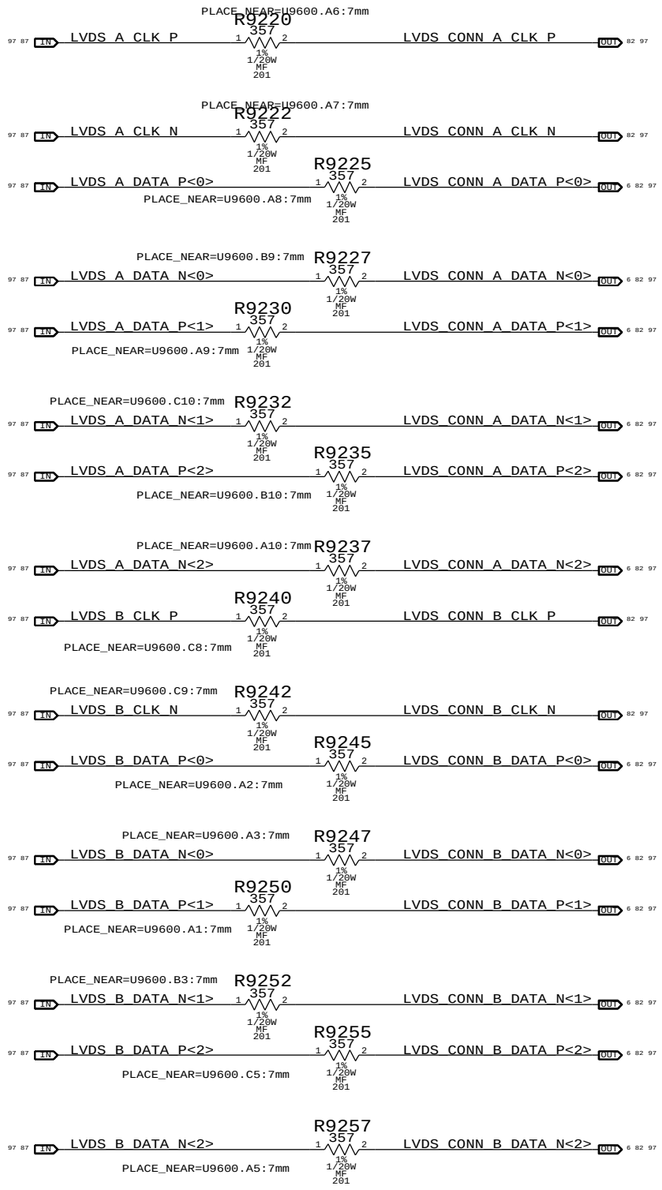
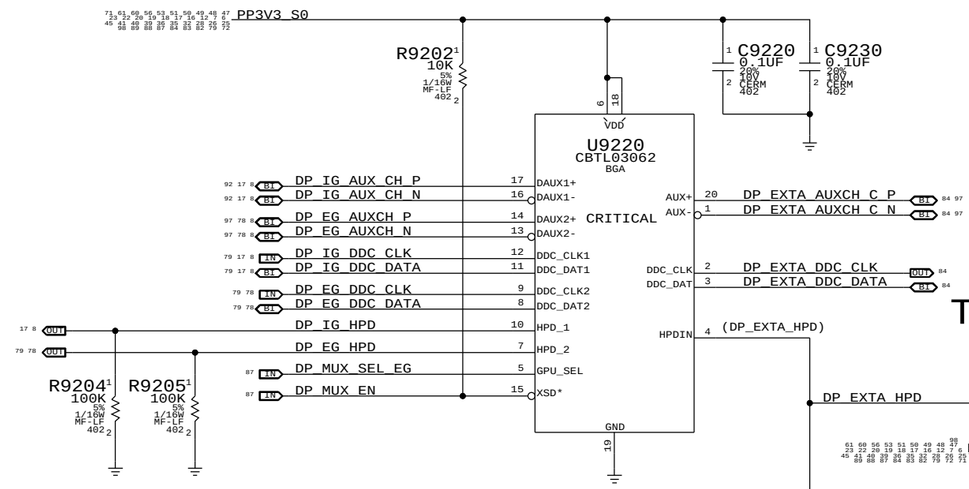
LVDS Transmitter Termination

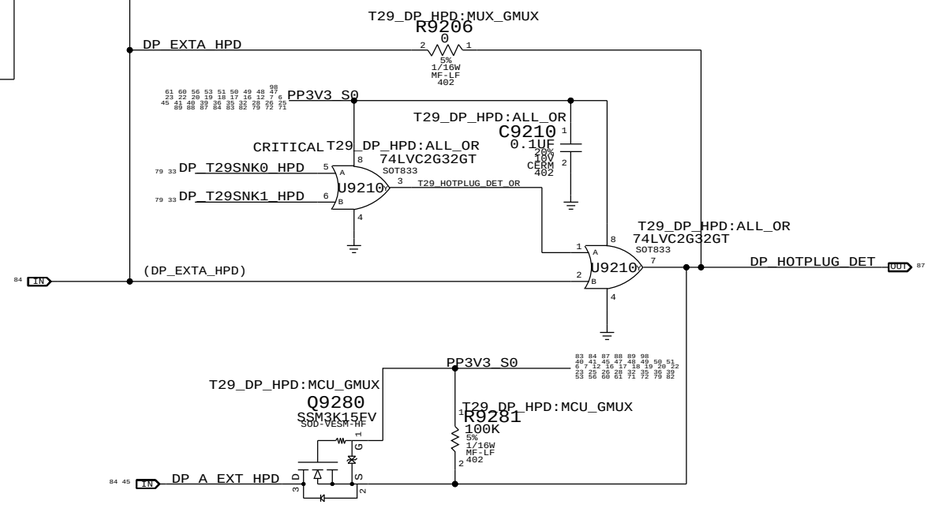
All emulated LVDS outputs require this termination



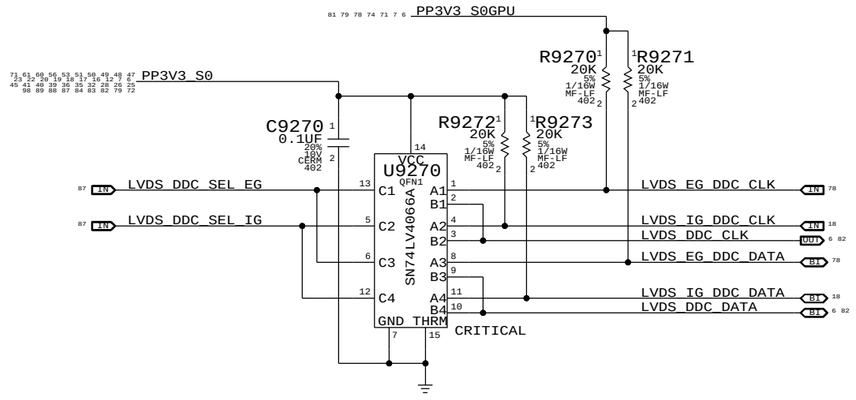
DP AUX, DDC, & HPD muxing to IG/EG



T29/DP HOT PLUG IN



LVDS DDC MUX



SYNC_MASTER=K92_MLB SYNC_DATE=11/21/2010

PAGE TITLE

Muxed Graphics Support

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T29 A High-Speed Signals

DP_EXTA_ML_C_P<0> C9300 0.1uF → DP_EXTA_ML_P<0>
DP_EXTA_ML_C_N<0> C9301 0.1uF → DP_EXTA_ML_N<0>
DP_EXTA_ML_C_P<1> C9302 0.1uF → DP_EXTA_ML_P<1>
DP_EXTA_ML_C_N<1> C9303 0.1uF → DP_EXTA_ML_N<1>
DP_EXTA_ML_C_P<2> C9304 0.1uF → DP_EXTA_ML_P<2>
DP_EXTA_ML_C_N<2> C9305 0.1uF → DP_EXTA_ML_N<2>
DP_EXTA_ML_C_P<3> C9306 0.1uF → DP_EXTA_ML_P<3>
DP_EXTA_ML_C_N<3> C9307 0.1uF → DP_EXTA_ML_N<3>
DP_EXTA_AUXCH_C_P C9308 0.1uF → DP_EXTA_AUXCH_P
DP_EXTA_AUXCH_C_N C9309 0.1uF → DP_EXTA_AUXCH_N

PP3V3_S0 → R9309 1M 5% MF-LF 1/16W 402 → DP_EXTA_AUXCH_P
PP3V3_S0 → R9308 1M 5% MF-LF 1/16W 402 → DP_EXTA_AUXCH_N

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

T29_D2R_C_N<0> → L9372 1.0NH+/-0.1NH 0201-1 → T29_R2D_C_F_N<0> → C9372 0.47UF → T29_R2D_P<0>
T29_D2R_C_P<0> → L9373 1.0NH+/-0.1NH 0201-1 → T29_R2D_C_F_P<0> → C9373 0.47UF → T29_R2D_N<0>
OVERSIZE_PAD=0.875 mm^2 (Both L's)
Inductor values TBD
(C9372.2) (C9373.2) GND_VOID=TRUE

T29 signals are P/N-swapped after AC caps to improve layout.

T29_A_BIAS_R2D_P0 → R9372 1.5K 5% MF 1/20W 201 → T29_R2D_P<0>
T29_A_BIAS_R2D_N0 → R9373 1.5K 5% MF 1/20W 201 → T29_R2D_N<0>
T29 Path Biasing

T29_D2R_C_P<0> → D9364 BAR90-02LRH TSLP-2-7 → GND_VOID=TRUE (D9364.2)
T29_D2R_C_N<0> → D9372 BAR90-02LRH TSLP-2-7 → T29: TX_0 → T29DPA_ML_C_P<0>
D9373 BAR90-02LRH TSLP-2-7 → T29DPA_ML_C_N<0>
D9365 BAR90-02LRH TSLP-2-7 → GND_VOID=TRUE (D9372/D9373) GND_VOID=TRUE (D9365.2)
CRITICAL (All 4 D's)
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY
R9374 1.5K 5% MF 1/20W 201 → GND_VOID=TRUE
R9375 1.5K 5% MF 1/20W 201 → GND_VOID=TRUE

T29_D2R_C_P<1> → T29_D2R_C_N<1>
T29_R2D_C_N<1> → L9382 1.0NH+/-0.1NH 0201-1 → T29_R2D_C_F_N<1> → C9382 0.47UF → T29_R2D_P<1>
T29_R2D_C_P<1> → L9383 1.0NH+/-0.1NH 0201-1 → T29_R2D_C_F_P<1> → C9383 0.47UF → T29_R2D_N<1>
OVERSIZE_PAD=0.875 mm^2 (Both L's)
(C9383.2) GND_VOID=TRUE

T29_A_BIAS_R2D_P1 → R9382 1.5K 5% MF 1/20W 201 → T29_R2D_P<1>
T29_A_BIAS_R2D_N1 → R9383 1.5K 5% MF 1/20W 201 → T29_R2D_N<1>

T29_D2R_C_P<1> → D9360 BAR90-02LRH TSLP-2-7 → GND_VOID=TRUE (D9360.2)
T29_D2R_C_N<1> → D9382 BAR90-02LRH TSLP-2-7 → T29: TX_1 → T29DPA_ML_C_P<2>
D9383 BAR90-02LRH TSLP-2-7 → T29DPA_ML_C_N<2>
D9361 BAR90-02LRH TSLP-2-7 → GND_VOID=TRUE (D9382/D9383) GND_VOID=TRUE (D9361.2)
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN (D9382/D9383)
SIGNAL_MODEL=EMPTY (D9360/D9361)
R9384 1.5K 5% MF 1/20W 201 → GND_VOID=TRUE
R9385 1.5K 5% MF 1/20W 201 → GND_VOID=TRUE

DP Path Biasing

DP A Super-Driver

PP3V3_S0 → C9310 2.2UF 20% 6.3V CERM 402-LF; C9311 0.1UF 20% 10V CERM 402; C9312 0.1UF 20% 10V CERM 402

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

NO STUFF R9311 1K; R9310 1K; R9312 1K

U9310 PS8301TQFN40GTR-A2 QFN CRITICAL

DP_EXTA_ML_P<0>	1 IN_D0P	OUT_D0P 30	DP_SDRVA_ML_C_P<0>
DP_EXTA_ML_N<0>	2 IN_D0N	OUT_D0N 29	DP_SDRVA_ML_C_N<0>
DP_EXTA_ML_P<1>	4 IN_D1P	OUT_D1P 28	DP_SDRVA_ML_C_P<1>
DP_EXTA_ML_N<1>	5 IN_D1N	OUT_D1N 27	DP_SDRVA_ML_C_N<1>
DP_EXTA_ML_P<2>	7 IN_D2P	OUT_D2P 25	DP_SDRVA_ML_C_P<2>
DP_EXTA_ML_N<2>	8 IN_D2N	OUT_D2N 24	DP_SDRVA_ML_C_N<2>
DP_EXTA_ML_P<3>	9 IN_D3P	OUT_D3P 23	DP_SDRVA_ML_C_P<3>
DP_EXTA_ML_N<3>	10 IN_D3N	OUT_D3N 22	DP_SDRVA_ML_C_N<3>
DP_EXTA_DDC_CLK	14 IN_SCL	AC_AUXP 20	DP_SDRVA_AUXCH_C_P
DP_EXTA_DDC_DATA	13 IN_SDA	AC_AUXN 19	DP_SDRVA_AUXCH_C_N
DP_EXTA_AUXCH_P	16 IN_AUXP	OUT_AUXP_SCL	(DP_SDRVA_AUXCH_P)
DP_EXTA_AUXCH_N	15 IN_AUXN	OUT_AUXN_SDA	(DP_SDRVA_AUXCH_N)
DP_EXTA_HPD	3 IN_HPD	(IPD) OUT_HPD	(DP_SDRVA_HPD)
DPSDRVA_I2C_CTL_EN	26 I2C_CTL_EN (IPU)	CA_DET	32 DP_A_CA_DET
DPSDRVA_I2C_ADDR0	36 I2C_ADDR0 (IPD)	CEXT	11 DPSDRVA_CEXT
DPSDRVA_I2C_ADDR1	35 I2C_ADDR1 (IPD)		
I2C_DPSDRVA_SCL	38 SCL_CTL		
I2C_DPSDRVA_SDA	37 SDA_CTL		
DPSDRVA_REXT	12 REXT		
DP_AUXCH_ISOL	39 AUXDDC_OFF (IPD)		
DP_A_PWRDWN_R	34 PD (IPD)		

PLACE_NEAR=U9310.11:2 mm
C9319 2.2UF 20% 6.3V CERM 402-LF

AUXCH Snoop Port, used by PS8301 during training.
C9369 0.1UF; C9368 0.1UF

SDRV_PD R9318 0 5% 1/16W MF-LF 402; R9319 4.99K 1% 1/16W MF-LF 402

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

GND THMPAD

R9354 30 5% 1/20W MF 201; R9353 270 5% 1/20W MF 201
R9355 30; R9350 30; R9351 30 5% 1/20W MF 201
R9352 270 5% 1/20W MF 201

DP_SDRVA_ML_R_P<0> → C9364 0.22UF 20% 6.3V X5R 0201 → DP_SDRVA_ML_P<0>
DP_SDRVA_ML_R_N<0> → C9365 0.22UF 20% 6.3V X5R 0201 → DP_SDRVA_ML_N<0>
DP_SDRVA_ML_R_P<2> → C9360 0.22UF 20% 6.3V X5R 0201 → DP_SDRVA_ML_P<2>
DP_SDRVA_ML_R_N<2> → C9361 0.22UF 20% 6.3V X5R 0201 → DP_SDRVA_ML_N<2>

PP3V3_S0 → C9359 0.1UF 10% 16V X5R 402 → CRITICAL U9359 74LVC1G04DBDCK SC70
DP_A_PWRDWN → DP_A_BIAS
IC supports input high while Vcc = 0V.

DP_A_BIAS0 VOLTAGE=3.3V → R9361 1.5K 5% MF 1/20W 201 → R9360 1.5K → R9365 1.5K → R9364 1.5K
DP_A_BIAS2 VOLTAGE=3.3V → R9363 51 5% 1/20W MF 201 PLACE_NEAR=C9361.1:2mm
R9362 51 5% 1/20W MF 201 PLACE_NEAR=C9361.1:2mm

DP/T29 A Low-Speed MUX

PP3V3_SW_DPAPWR Must be 3.3V DP A port power

U9390 CBTL04DP081 HVQFN

DP_SDRVA_ML_N<3>	31 DIN1_0+	DOUT_0+ 1	T29DPA_ML_N<3>
DP_SDRVA_ML_P<3>	30 DIN1_0-	DOUT_0- 2	T29DPA_ML_P<3>
DP_SDRVA_ML_N<1>	27 DIN1_1+		T29: Unused
DP_SDRVA_ML_P<1>	26 DIN1_1-	DOUT_1+ 4	T29DPA_ML_N<1>
DP_SDRVA_AUXCH_P	19 AUX1+	DOUT_1- 5	T29DPA_ML_P<1>
DP_SDRVA_AUXCH_N	18 AUX1-		T29: LSX_A_R2P/P2R (P/N)
DP_SDRVA_HPD	17 HPD_1	AUX+ 6	DP_A_EXT_AUXCH_P
CKPLUS_WAIVE=NdifPr_badTerm		AUX- 7	DP_A_EXT_AUXCH_N
T29_A_RSVD_N	25 DIN2_0+		T29: RX_1 Bias Sink
T29_A_RSVD_P	24 DIN2_0-	HPD_IN 8	DP_A_EXT_HPD
(T29_A_LSX_P2R)	23 DIN2_1+		
(T29_A_LSX_R2P)	22 DIN2_1-		
T29_D2R1_BIASP	15 AUX2+		
T29_D2R1_BIASN	14 AUX2-		
	13 HPD_2		
DP_A_PWRDWN	10 GPU_SEL		
T29_A_BIAS	32 AUX_SEL		
	11 NC		

CRITICAL
OMIT_TABLE: LO=Port A, HI=Port B
THMPAD GND
SIGNAL_MODEL=T29DP_MUX

R9396 1K; R9397 1K; R9398 100K
R9399 100K
C9390 0.1UF; C9391 0.1UF

CBTL04DP081 (353S3151) and PI3VEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

Port A MCU

PP3V3_SW_DPAPWR Must be 3.3V DP A port power

U9330 LPC1112A HVQFN25 CRITICAL OMIT_TABLE

DP_A_CA_DET	1 RESET#/PIO0_0	R/PIO1_0/AD1 16	T29DPA_CONFIG1_RC
	2 PIO0_1/CLKOUT	R/PIO1_1/AD2 17	T29DPA_CONFIG2_RC
T29_LSEO<0>	7 PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3 18	T29_A_HV_EN_R
I2C_T29_SCL	8 PIO0_4/SCL (OD)	(IPU) SWDIO/PIO1_3/AD4 19	T29_A_UC_ADDR
I2C_T29_SDA	9 PIO0_5/SDA (OD)	PIO1_4/AD5/WAKEUP 20	DP_A_EXT_HPD
T29DPA_HPD	10 PIO0_6/SCK	PIO1_6/RXD 23	T29_A_LSX_P2R
T29_A_BIAS	11 PIO0_7/CTS#	PIO1_7/TXD 24	T29_A_LSX_R2P
T29_LSOE<0>	12 PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0 6	T29_LSEO<1>
T29_LSOE<1>	13 PIO0_9/MOSI/CT16B0_MAT1		
	14 SWCLK/PIO0_10/SCK/CT16B0_MAT2 (OD)		
T29_MCU_INT_L	15 R/PIO0_11/AD0 (OD)	XTALIN 4	
	VSS 3	THRM PAD 25	

C9330 0.1UF; C9331 0.1UF

R9338 10K; R9334 10K; R9339 1M

T29_A_HV_EN → R9334 → R9338
P2R = Plug to Receptacle
R2P = Receptacle to Plug

I2C Addr: 0x26/0x27 (Wr/Rd)

R9335 1K; R9336 10K

=T29_WAKE_L: use PCIe WAKE#

PCIE_WAKE_L → OMIT R9330 0 → SWCLK / SWDIO
T29_A_UC_ADDR

R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

SYNC_MASTER=T29_REF SYNC_DATE=10/16/2010
PAGE TITLE: DisplayPort/T29 A MUXing
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3.3V/HV Power MUX

Port A 3.3V Power Switch

Port A HV Power Switch

PP3V3_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

PP15V_T29
20V Max

R9416 470K 5% 1/10W MF-LF 402

C9410 0.1UF 10% 50V X7R 603-1

U9410 SN1010017 QFN
VIN VOUT EN* (IPU-Weak!) FLT* RTRY* ILIM CT IFLT GND THRM PAD

C9411 0.1UF 10% 50V X7R 603-1

PPHV_SW_DPAPWR

D9410 SM STPS2L30AF

DPAPWRSW_HVEN_L_R
TP_DPAPPWRSW_FLT_L
DPAPWRSW_ILIM
DPAPWRSW_IFLT

C9412 0.47UF 10% 16V CERM-X5R 402 <CT>
OMIT_TABLE

R9410 100K 5% 1/10W MF-LF 402 <RFLT>

R9411 210K 1% 1/10W MF-LF 402 <RLIM>

(*) U9410 tolerance unknown

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	944mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

IFLT = 200k / RFLT = 885mA
ILIM = 201k / RLIM = 935mA
TFLT = CCT * 38900
TSD = CCT * 100000

Q9415 SSM3K15FV SOD-VESM-HF

Bleeder Resistor
2.5V / 249 ohm = 10mA
R9419 249 1% 1/10W MF-LF 402 P = ~27mW

DPAPWR_BLDR_E
MIN_LINE_WIDTH=0.20 MM
MIN_NECK_WIDTH=0.20 MM

Q9419 DMB53D0UV SOT-563

DPAPWR_BLDR_B

Q9419 DMB53D0UV SOT-563

Note: Bleeder active when DPAPWRSW_HV_DET is HIGH and T29_A_HV_EN is LOW.

T29_A_HV_EN

C9490 0.1UF 10% 6.3V X5R 201

PLACE_NEAR=C9490.1:2mm

R9490 51 5% 1/20W MF 201

T29_A_BIAS_R
VOLTAGE=3.3V

T29_A_BIAS_D2R_P1
T29_A_BIAS_D2R_N1

R9498 2.2K 5% 1/20W MF 201
R9499 2.2K 5% 1/20W MF 201

GND_VOID=TRUE

T29_D2R_C_P<1>
T29_D2R_C_N<1>

D9498 BAR90-02LRH TSLP-2-7
D9499 BAR90-02LRH TSLP-2-7

CRITICAL
GND_VOID=TRUE
SIGNAL_MODEL=T29PIN
(Both L's)

DP_A_EXT_AUXCH_P
DP_A_EXT_AUXCH_N

T29DPA_HPD
T29DPA_CONFIG1_RC
T29DPA_CONFIG2_RC

R9452 1M 5% 1/10W MF-LF 402
R9451 1M 5% 1/10W MF-LF 402

C9494 330PF 10% 50V CERM 402
C9495 330PF 10% 50V CERM 402

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

R9441 100K 5% 1/10W MF-LF 402

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 65mOhm @ 2.5V Vgs
Id(max): 3.7A @ 70C

CRITICAL D9425 POWERDI-123 DFLS1100

CRITICAL Q9425 SI8409DB 8A

3.3V/HV MUXed

3.3V Always

Blocking FET, off when Source >3.4V or HV_EN high.

R9427 100K 1% 1/10W MF-LF 402
R9425 4.7K 5% 1/10W MF-LF 402
R9426 1K 5% 1/16W MF-LF 402
R9430 4.7K 5% 1/16W MF-LF 402

R9428 21.5K 1% 1/10W MF-LF 402

DPAPWRSW_VREF
DPAPWRSW_P3V3_ON_L
DPAPWRSW_HV_DET_R_L

CRITICAL U9426 ZXRE060A SOT353 IN OUT GND PGND FB

R9429 4.7K 5% 1/10W MF-LF 402
C9424 0.47UF 10% 6.3V CERM-X5R 402

DPAPWRSW_ON_L_C

NO STUFF C9429 0.1UF 20% 10V CERM 402

R9424 22 5% 1/10W MF-LF 402

C9426 0.1UF 20% 10V CERM 402

Q9426 MMDT3946XG SOT363

DPAPWRSW_HV_DET_L

DPAPWRSW_NPN_E

R9418 1K 5% 1/10W MF-LF 402

DPAPWRSW_HV_DET

ZXRE060A REF range: 0.595-0.605V (0.600V nominal)
Circuit threshold range: 3.363-3.439V (3.395V nominal)

CRITICAL U9480 TPS2051B SOT23 OUT IN OC* EN GND

DP_PWR must be S4 to support wake from T29 devices.

PP3V3_S5
T29_A_HV_EN
SMC_S4_WAKESRC_EN

C9486 10UF 20% 6.3V X5R 603
C9485 0.1UF 20% 10V CERM 402
C9481 0.1UF 20% 10V CERM 402
C9480 22UF 20% 6.3V X5R-CERM-1 603
C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM

T29_A_BIAS

CRITICAL U9435 ZXRE060A SOT353 IN OUT FB PGND GND

C9435 0.1UF 20% 10V CERM 402
C9436 1UF 10% 10V X5R 402

DPAPWRSW_P3V3_ON
DPAPWRSW_ON_C
T29_A_HV_EN

Q9430 SSM6N37FEAPE SOT563
Q9430 SSM6N37FEAPE SOT563

R9437 82 5% 1/10W MF-LF 402

T29_2V9_ENABLE

R9435 100K 1% 1/10W MF-LF 402

DPAPWR_FB_DIV

R9436 24.9K 1% 1/10W MF-LF 402

R9433 220 5% 1/16W MF-LF 402
R9432 10K 5% 1/16W MF-LF 402

DisplayPort/T29 A Connector

PP3V3RHV_SW_DPAPWR_UF
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

L9400 FERR-120-OHM-3A 0603

PP3V3RHV_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

Circuit threshold range: 2.877-2.941V (2.903V nominal)

C9400 0.01UF 10% 50V X7R 402

For J9400 T29 SMT pads (3, 5, 7, 8, 19):
GND_VOID=TRUE

CRITICAL J9400 DSPLYPRT-M97-1 F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS
2	HOT_PLUG_DETECT	GND 1
4	CONFIG1	ML_LANE0P 3
6	CONFIG2	ML_LANE0N 5
8	GND	GND 7
10	ML_LANE3P	ML_LANE1P 9
12	ML_LANE3N	ML_LANE1N 11
14	GND	GND 13
16	AUX_CHP	ML_LANE2P 15
18	AUX_CHN	ML_LANE2N 17
20	DP_PWR	RETURN 19
	SHIELD PINS	22 21

T29 Dir DP Dir

T29_D2R_C_P<0>
T29_D2R_C_N<0>

R9494 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
R9495 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

R9403 12 5% 1/16W MF-LF 402 GND_DPACONN_8 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V

R9404 12 5% 1/16W MF-LF 402 GND_DPACONN_14 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V

T29: Unused

T29DPA_ML_P<3>
T29DPA_ML_N<3>

CRITICAL L9498 650NH-5%-0.430MA-0.052OHM 0603 SIGNAL_MODEL=EMPTY

CRITICAL L9499 650NH-5%-0.430MA-0.052OHM 0603 SIGNAL_MODEL=EMPTY

T29DPA_D2R1_AUXCH_P
T29DPA_D2R1_AUXCH_N

R9402 12 5% 1/10W MF-LF 402

T29DPA_HPD_R

R9401 12 5% 1/16W MF-LF 402

DPACONN_20_RC MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18V

C9498 30PF 5% 50V CERM 402
C9499 30PF 5% 50V CERM 402

C9402 0.01UF 10% 50V X7R 402
C9401 0.01UF 10% 50V X7R 402

T29: TX_0

T29DPA_ML_P<0>
T29DPA_ML_N<0>

R9405 12 5% 1/20W MF 201 GND_DPACONN_1 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V

R9406 12 5% 1/20W MF 201 GND_DPACONN_7 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V

T29: LSX_R2P/P2R (P/N)

T29DPA_ML_P<1>
T29DPA_ML_N<1>

R9407 12 5% 1/20W MF 201 GND_DPACONN_13 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V

T29: TX_1

T29DPA_ML_P<2>
T29DPA_ML_N<2>

L9408 FERR-120-OHM-3A 0603

R9408 12 5% 1/20W MF 201 GND_DPACONN_19 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V

GND_VOID=TRUE (Both C's)

C9470 0.47UF 20% 4V CERM-X5R-1 201
C9471 0.47UF 20% 4V CERM-X5R-1 201
C9472 0.47UF 20% 4V CERM-X5R-1 201
C9473 0.47UF 20% 4V CERM-X5R-1 201

T29DPA_ML_C_P<0>
T29DPA_ML_C_N<0>
T29DPA_ML_C_P<2>
T29DPA_ML_C_N<2>

R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0 OHM,5,1/16W,0402,SMD,LF	C9412		
132S0121	1	CAP,CER,0.1UF,10%,6.3V,XSR,0201,SMD	R9405		
132S0121	1	CAP,CER,0.1UF,10%,6.3V,XSR,0201,SMD	R9406		

SYNC_MASTER=T29_REF SYNC_DATE=10/16/2010

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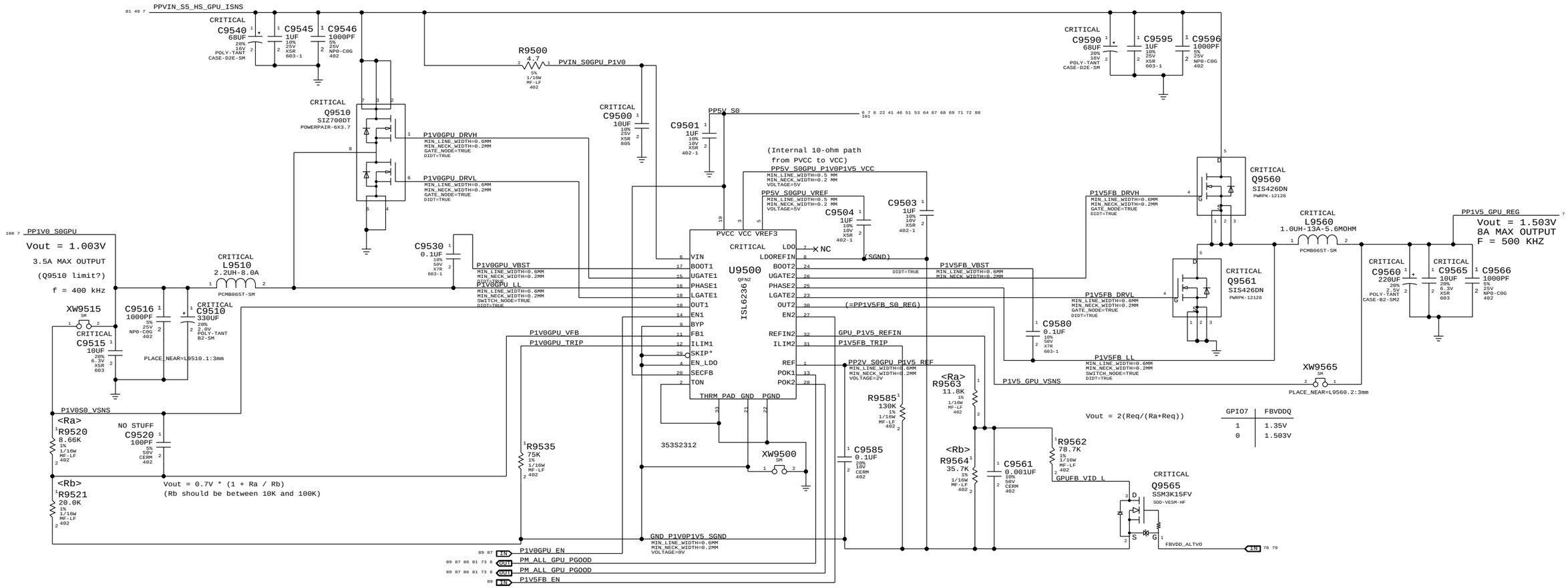

SYNC_MASTER=K91_ERIC	SYNC_DATE=10/08/2010
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GMUX CPLD

R9600 0 5% 1/16W MF-LF 402 — PP3V3_S0

C9610–C9629 0.1UF 20% 10V CERM 402 — PP3V3_S0

R9610 0 5% 1/16W MF-LF 402 — PP1V8_S0

C9611–C9617 0.1UF 20% 10V CERM 402 — PP1V8_S0

C9600 4.7UF 20% 4V X5R-1 402; C9604–C9609 0.1UF 20% 10V CERM 402 — PP1V2_S0

PP3V3_S0_GMUX_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=3.3V

PP1V8_S0_GMUX_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=1.8V

PP3V3_S0_GMUX_ULC_VCCPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=3.3V

L9621 FERR-220-OHM 0402
C9631 0.1UF 20% 10V CERM 402

PP3V3_S0_GMUX_LRC_VCCPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=3.3V

L9620 FERR-220-OHM 0402
C9630 0.1UF 20% 10V CERM 402

R9645 10K 1% 1/20W MF 201 — PP3V3_S0
R9640 10K 1% 1/20W MF 201 — PP3V3_S0
NO STUFF R9646 10K 1% 1/20W MF 201
NO STUFF R9641 10K 1% 1/20W MF 201

VCC: B11, C4, J3, J13, N11, P8
VCCAUX: C11, J2, J14, M8
VCCIO6: B5
VCCIO1: B7
VCCIO2: A12, C14, F13, M12
VCCIO3: M9
VCCIO4: M3
VCCIO5: N5
VCCIO6: M1
VCCIO7: C3, F2
VCCJ: K12
ULC_VCCPLL: A4
LRC_VCCPLL: P11

OMIT CRITICAL

U9600 XP25-5 CSBGA

JTAG_ISP_TCK	K14	TCK	
JTAG_GMUX_TDI	L13	TDI	
JTAG_GMUX_TDO	K13	TDO	
JTAG_GMUX_TMS	L12	TMS	
GMUX_TOE	K2	TOE	
GMUX_CFG0	K1	CFG0	
LCD_BKLT_EN	P2	PB7A	BANK5
LCD_BKLT_PWM	N2	PB7B	BANK5
LVDS_DDC_SEL_EG	P4	PB14A	BANK5
LVDS_DDC_SEL_IG	N4	PB14B	BANK5
DP_MUX_EN	N3	PB15A (OD)	BANK5
DP_MUX_SEL_EG	M4	PB15B	BANK5
EG_RESET_L	P5	PB16A	BANK5
P3V3GPU_EN	M5	PB16B	BANK5
GPUVCORE_EN	P6	PB17A	BANK5
P1V0GPU_EN	M6	PB17B	BANK5
P1V5FB1V8GPU_R_EN	P7	PB18A	BANK5
PEG_CLKREQ_L	M7	PB18B (OD)	BANK5
DP_CA_DET_EG	N7	PB19A	BANK5
LCD_PWR_EN	N8	PB19B	BANK5
LPC_AD<0>	P9	PB20A	BANK4
LPC_AD<1>	N9	PB20B	BANK4
LPC_AD<2>	P10	PB26A	BANK4
LPC_AD<3>	M10	PB26B	BANK4
LPC_FRAME_L	P12	PB27A	BANK4
LPCPLUS_RESET_L	P13	PB27B	BANK4
LPC_CLK33M_GMUX	N12	PB28A	BANK4
GMUX_INT	P14	PB28B	BANK4
LVDS_IG_B_DATA_P<2>	B1	PL2A	BANK7
LVDS_IG_B_DATA_N<2>	B2	PL2B	BANK7
GMUX_PL6A	C2	PL6A	BANK7
TP_GMUX_PL6B	D3	PL6B	BANK7
LVDS_IG_A_DATA_P<0>	D1	PL7A	BANK7
LVDS_IG_A_DATA_N<0>	E1	PL7B	BANK7
LVDS_IG_A_DATA_P<1>	D2	PL8A	BANK7
LVDS_IG_A_DATA_N<1>	E3	PL8B	BANK7
LVDS_IG_A_DATA_P<2>	F1	PL9A	BANK7
LVDS_IG_A_DATA_N<2>	G1	PL9B	BANK7
LVDS_IG_B_DATA_P<0>	F3	PL10A	BANK7
LVDS_IG_B_DATA_N<0>	G2	PL10B	BANK7
LVDS_IG_B_DATA_P<1>	H2	PL11A	BANK7
LVDS_IG_B_DATA_N<1>	G3	PL11B	BANK7
LVDS_IG_A_CLK_P	H1	PL12A	BANK7
LVDS_IG_A_CLK_N	H3	PL12B	BANK7
TP_LVDS_MUX_SEL_EG	L1	PL14A	BANK6
TP_GMUX_PL14B	L3	PL14B	BANK6
GMUX_RESET_L	K3	PL15A	BANK6
GMUX_VSYNC	L2	PL15B	BANK6
PM_ALL_GPU_PGOOD	N1	PL25A	BANK6
PEX_CLKREQ_L	P1	PL25B	BANK6

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

GND: J1, B8, C6, C12, C13, C15, M14, N10, N6, P3, M2, C1, E2, B4, M11

GNDIO0, GNDIO1, GNDIO2, GNDIO3, GNDIO4, GNDIO5, GNDIO6, GNDIO7, ULC_GNDPLL, LRC_GNDPLL

PT7A	A2	LVDS_B_DATA_P<0>	
PT7B	A3	LVDS_B_DATA_N<0>	
PT8A	A1	LVDS_B_DATA_P<1>	
PT8B	B3	LVDS_B_DATA_N<1>	
PT9A	C5	LVDS_B_DATA_P<2>	
PT9B	A5	LVDS_B_DATA_N<2>	
PT14A	B6	EG_PWRSEQ_EN	
PT14B	C7	GMUX_DEBUG_RESET_L	
PT15A	A6	LVDS_A_CLK_P	BANK0
PT15B	A7	LVDS_A_CLK_N	BANK0
PT16A	C8	LVDS_B_CLK_P	BANK0
PT16B	C9	LVDS_B_CLK_N	BANK0
PT17A	A8	LVDS_A_DATA_P<0>	BANK0
PT17B	B9	LVDS_A_DATA_N<0>	BANK0
PT18A	A9	LVDS_A_DATA_P<1>	BANK0
PT18B	C10	LVDS_A_DATA_N<1>	BANK0
PT19A	B10	LVDS_A_DATA_P<2>	BANK0
PT19B	A10	LVDS_A_DATA_N<2>	BANK0
PT20A	A11	GND	BANK1
PT20B	B12	GND	BANK1
PT28A	B13	GND	BANK1
PT28B	A13	GND	BANK1
PR2A	A14	DP_A_CA_DET	BANK2
PR2B	B14	DP_HOTPLUG_DET	BANK2
PR6A	D12	LVDS_EG_A_DATA_P<0>	BANK2
PR6B	D13	LVDS_EG_A_DATA_N<0>	BANK2
PR7A	D14	LVDS_EG_A_DATA_P<1>	BANK2
PR7B	E14	LVDS_EG_A_DATA_N<1>	BANK2
PR8A	E12	LVDS_EG_A_DATA_P<2>	BANK2
PR8B	F12	LVDS_EG_A_DATA_N<2>	BANK2
PR9A	F14	LVDS_EG_B_DATA_P<0>	BANK2
PR9B	G14	LVDS_EG_B_DATA_N<0>	BANK2
PR10A	G12	LVDS_EG_B_DATA_P<1>	BANK2
PR10B	G13	LVDS_EG_B_DATA_N<1>	BANK2
PR11A	H13	LVDS_EG_B_DATA_P<2>	BANK2
PR11B	H12	LVDS_EG_B_DATA_N<2>	BANK2
PR12A	H14	LVDS_EG_A_CLK_P	BANK2
PR12B	J12	LVDS_EG_A_CLK_N	BANK2
PR14A	L14	LVDS_IG_PANEL_PWR	BANK3
PR14B	M13	EG_LCD_PWR_EN	BANK3
PR24A	N14	LVDS_IG_BKL_ON	BANK3
PR24B	N13	EG_BKLT_EN	BANK3

PP3V3_S3 → R9676 100K 5% 1/20W MF 201 → GMUX_S3_PD_EN

Q9607 SSM6N15FEAPE SOT563 (D 3, G 5, S 4)

Q9607 SSM6N15FEAPE SOT563 (D 6, G 2, S 1) — ALL_SYS_PWRGD

NO STUFF R9675 0 5% 1/10W MF-LF 2402

GMUX_S3_PD_GND

CRITICAL
J9600 1909782 M-RT-SM — GMUX_JTAG_CONN

1	PP3V3_S0	
2	JTAG_GMUX_TDO	
3	JTAG_GMUX_TDI	
4	JTAG_GMUX_TMS	
5		
6	JTAG_ISP_TCK	
7		
8		

NO STUFF R9647 10K 5% 1/20W MF 201

NO STUFF R9670 10K 1% 1/20W MF 201 — PP3V3_S0 → GMUX_VSYNC

R9605 1K 5% 1/20W MF 201 — PP3V3_T29 → T29_JTAG_FET

Q9605 SSM6N15FEAPE SOT563 (D 6, G 2, S 1) — JTAG_GMUX_TDI → JTAG_ISP_TDI

Q9605 SSM6N15FEAPE SOT563 (D 3, G 5, S 4) — JTAG_GMUX_TDO → JTAG_ISP_TDO

LVDS Receiver Termination

LVDS_IG_A_CLK_P	R9650	100	LVDS_IG_A_CLK_N
LVDS_IG_A_DATA_P<0>	R9651	100	LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<1>	R9652	100	LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<2>	R9653	100	LVDS_IG_A_DATA_N<2>
LVDS_IG_B_DATA_P<0>	R9654	100	LVDS_IG_B_DATA_N<0>
LVDS_IG_B_DATA_P<1>	R9655	100	LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_P<2>	R9656	100	LVDS_IG_B_DATA_N<2>
LVDS_EG_A_CLK_P	R9660	100	LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<0>	R9661	100	LVDS_EG_A_DATA_N<0>
LVDS_EG_A_DATA_P<1>	R9662	100	LVDS_EG_A_DATA_N<1>
LVDS_EG_A_DATA_P<2>	R9663	100	LVDS_EG_A_DATA_N<2>
LVDS_EG_B_DATA_P<0>	R9664	100	LVDS_EG_B_DATA_N<0>
LVDS_EG_B_DATA_P<1>	R9665	100	LVDS_EG_B_DATA_N<1>
LVDS_EG_B_DATA_P<2>	R9666	100	LVDS_EG_B_DATA_N<2>

All: 1% 1/20W MF 201

Required Pullups

SIGNAL_MODEL=EMPTY — PP3V3_S0

EG_PWRSEQ_EN	R9684	1K	5% 1/20W MF 201
JTAG_GMUX_TDI	R9685	10K	5% 1/20W MF 201
JTAG_GMUX_TDO	R9686	10K	5% 1/20W MF 201
GMUX_DEBUG_RESET_L	R9680	1K	5% 1/20W MF 201

NO STUFF R9679 10K 1% 1/10W MF-LF 402 — SILK_PART=GMUX_RST

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K	5% 1/20W MF 201
LVDS_DDC_SEL_IG	R9682	10K	5% 1/20W MF 201
LVDS_DDC_SEL_EG	R9683	10K	5% 1/20W MF 201

NO STUFF (Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

EG_RESET_L	R9691	100K	5% 1/20W MF 201
LCD_BKLT_PWM	R9693	100K	5% 1/20W MF 201

P1V5FB1V8GPU_R_EN — R9674 4.7K 5% 1/20W MF 201

P1V0GPU_EN — R9673 4.7K 5% 1/20W MF 201

GPUVCORE_EN — R9672 4.7K 5% 1/20W MF 201

P3V3GPU_EN — R9671 4.7K 5% 1/20W MF 201

LCD_PWR_EN — R9678 4.7K 5% 1/20W MF 201

SYNC_MASTER=K91_MARY SYNC_DATE=08/03/2010

PAGE TITLE: Graphics MUX (GMUX)

Apple Inc.

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PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.715 A (EDP)

CRITICAL
Q9706
FDC638APZ_SBMS001
SSOT6-HF

PPBUS_G3H
F9700
3AMP-32V-467
603-HF
BOTTOM
PPBUS_S0_LCDBKLT_FUSED
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

PPBUS_SW_LCDBKLT_PWR
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

THERE IS A SENSE RESISTOR BETWEEN
PPBUS_SW_LCDBKLT_PWR
AND PPBUS_SW_BKL
ON THE SENSOR PAGE

R9788 301K 1% 1/16W MF-LF 402
C9782 0.1UF 10% 16V X5R 402
LCDBKLT_EN_DIV
R9789 147K 1% 1/16W MF-LF 402
LCDBKLT_EN_L

Q9707 SSM6N15FEAPE SOT563
LCD_BKLT_EN
LCDBKLT_DISABLE
Q9707 SSM6N15FEAPE SOT563
BKLT_PLT_RST_L

PP5V_S0
PPBUS_SW_BKL
PP3V3_S0

*C9797 AND C9799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

CRITICAL
L9701
33UH-1.8A-110MOHM
1217AS-2SM
PLACE_NEAR=L9701.2:3mm

CRITICAL
D9701
SOD-123
RB160M-60G
PLACE_NEAR=U9701.A5:3mm

PPVOUT_S0_LCDBKLT
MIN_LINE_WIDTH=0.375 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=50V

CRITICAL C9712 10UF 10% 25V X5R 805
C9713 0.1UF 10% 25V X5R 402
PLACE_NEAR=L9701.1:3mm
PLACE_NEAR=L9701.1:3mm
PLACE_NEAR=U9701.D1:5mm
C9710 10UF 10% 25V X5R 603-1
C9714 0.01UF 10% 25V X7R-CERM 402
PLACE_NEAR=U9701.D1:3mm

C9796 220PF 10% 50V X7R-CERM 402
CRITICAL C9797 10UF 10% 50V X5R 1210-1
CRITICAL C9799 10UF 10% 50V X5R 1210-1
PLACE_NEAR=D9701.2:5mm
PLACE_NEAR=D9701.2:3mm

PPVOUT_SW_LCDBKLT_FB
VOLTAGE=50V
XW9720 SM
PLACE_NEAR=C9797.1:5mm

C9711 0.1UF 10% 16V X5R 402
PLACE_NEAR=U9701.C4:4mm

BKL_VSYNC_R
MIN_NECK_WIDTH=0.075 mm
NO STUFF R9754 0 5% 1/16W MF-LF 402
R9755 10K 5% 1/16W MF-LF 402
NO STUFF C9741 1UF 10% 6.3V X5R 402
NO STUFF C9740 10UF 20% 6.3V X5R 603
NO STUFF R9740 47.0K 1% 1/16W MF-LF 402
GMUX_VSYNC
R9741 10K 5% 1/16W MF-LF 402
MIN_NECK_WIDTH=0.075 mm

R9753 0 5% 1/16W MF-LF 402
SMBUS_PCH_CLK
R9757 0 5% 1/16W MF-LF 402
SMBUS_PCH_DATA
Addr: 0x58(Wr)/0x59(Rd)

PPBUS_SW_LCDBKLT_PWR
R9731 301K 1% 1/16W MF-LF 402
R9715 100K 1% 1/16W MF-LF 402
R9704 33 5% 1/16W MF-LF 402
LCD_BKLT_PWM
C9704 33PF 5% 50V C0GM 402

C4 D1 C1
U9701
25-BUMP-MICRO
VDDIO VLDO VIN
LP8550
VSYNC SW_0 SW_1 FB FILTER ISET FSET SCLK SDA PWM EN FAULT GND_S GND_L GND_SW GND_SW
OUT1 OUT2 OUT3 OUT4 OUT5 OUT6
BKL_FLTR
BKL_ISET
BKL_FSET
BKL_SCL
BKL_SDA
BKL_PWM
BKL_EN
TP_BKL_FAULT
PLACE_SIDE=BOTTOM
CRITICAL
BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6

R9716 90.9K 1% 1/16W MF-LF 402
I_LED=22.7mA
R9714 16.2K 1% 1/16W MF-LF 402
Fpwm=9.62kHz
see spec for others
PLACEMENT_NOTE=Keep away from noise nodes(E4, A1, A2, B1, B2 pins)
XW9710 SM
GND_BKL_SGND
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
I_LED=369/Riset
(EEPROM should set EN_I_RES=1)

BKLT:PROD R9717 0 5% 1/16W MF-LF 402 — LED_RETURN_1
BKLT:PROD R9718 0 5% 1/16W MF-LF 402 — LED_RETURN_2
BKLT:PROD R9719 0 5% 1/16W MF-LF 402 — LED_RETURN_3
BKLT:PROD R9720 0 5% 1/16W MF-LF 402 — LED_RETURN_4
BKLT:PROD R9721 0 5% 1/16W MF-LF 402 — LED_RETURN_5
BKLT:PROD R9722 0 5% 1/16W MF-LF 402 — LED_RETURN_6
PLACE_NEAR=U9701.E5:10mm
PLACE_NEAR=U9701.D5:10mm
PLACE_NEAR=U9701.C5:10mm
PLACE_NEAR=U9701.E3:10mm
PLACE_NEAR=U9701.E2:10mm
PLACE_NEAR=U9701.E1:10mm
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.20 mm
BOTTOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SMT	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SMT	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=K901_KIRA SYNC_DATE=06/25/2010
PAGE TITLE
LCD Backlight Driver

Apple Inc.

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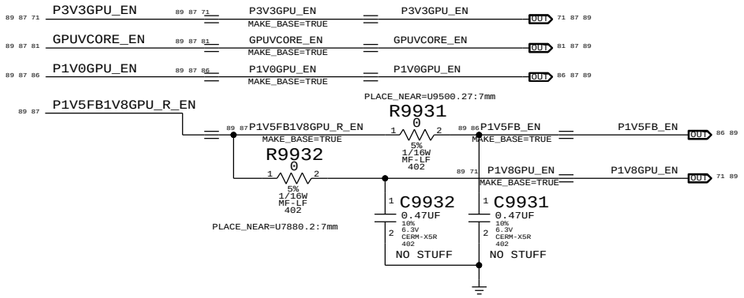
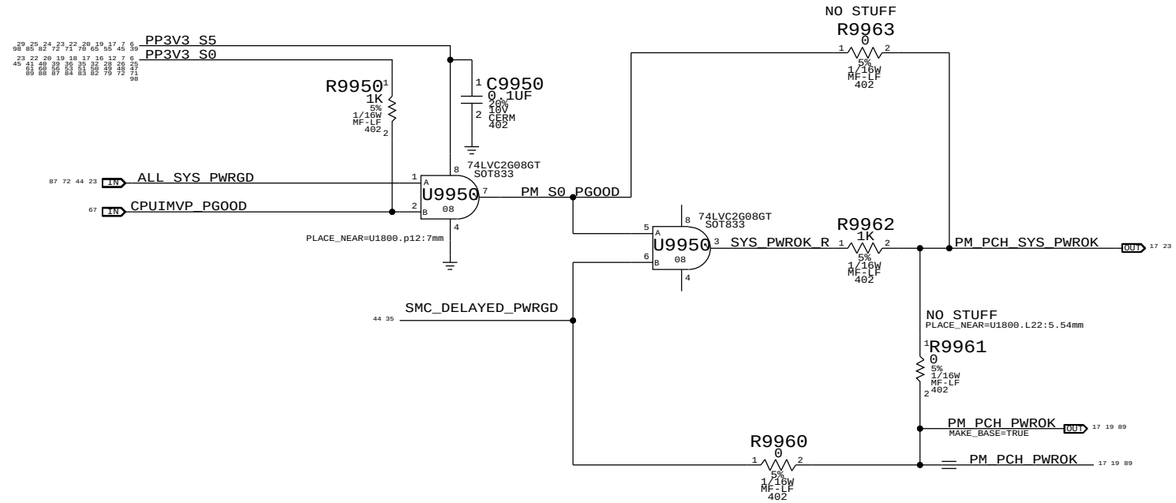
GPU Rail Sequencing

Whistler GPU requires rails to come up in the following order:

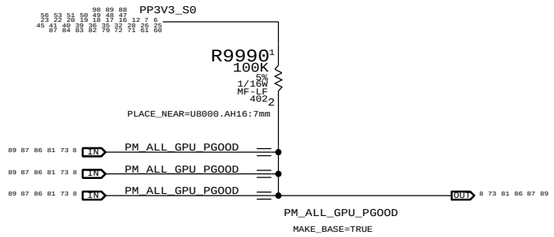
1) GPU_3.3V
2) GPUVcore
3) GPU_1.0V
4) GPU_1.8V;GDDR5 1.5/1.35V



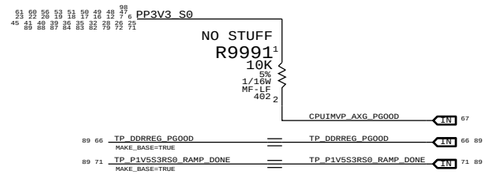
PCH S0 PWRGD



EXT GPU PWRGD Pullup



Unused PGOOD signal



SYNC_MASTER=K91_MARY SYNC_DATE=08/03/2010

PAGE TITLE: Power Sequencing EG/PCH S0

Apple Inc.

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	6 9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	6 9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	6 9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	6 9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	6 9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	6 9 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
	CPU_50S	CPU_AGTL	FDI_INT	6 9 17
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 44
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 29
XDP_CPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	23
XDP_BDRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 25
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2	
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..16>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	10 17
	CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT	8
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 45 67
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 19
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	CPU_55S	CPU_8MIL	CPU_PSI_L	
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	10 23
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	10 23
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
	CPU_55S	CPU_8MIL	CPU_VID<6..0>	8
	CPU_50S	CPU_AGTL	CPUIMVP_IMON	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 67
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	12
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	12
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	12
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	12
	CPU_55S	CPU_8MIL	GFX_VID<6..0>	8
PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	
	CPU_50S	CPU_AGTL	GFX_VR_EN	
	CPU_50S	CPU_AGTL	GFXIMVP_IMON	
	PCIE_85D	PCIE	PEG_R2D_P<7..0>	73
	PCIE_85D	PCIE	PEG_R2D_N<7..0>	73
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<7..0>	8 73
	PCIE_85D	PCIE	PEG_R2D_C_N<7..0>	8 73
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<7..0>	8 73
	PCIE_85D	PCIE	PEG_D2R_N<7..0>	8 73
	PCIE_85D	PCIE	PEG_D2R_C_P<7..0>	73
	PCIE_85D	PCIE	PEG_D2R_C_N<7..0>	73
	CPU_50S	CPU_VID	CPU_VIDSOUT	12 67
	CPU_50S	CPU_VID	CPU_VIDSCLK	12 67
	CPU_50S	CPU_VID	CPU_VIDALERT_L	12 67

SYNC_MASTER=K92_MLB SYNC_DATE=08/09/2010

PAGE TITLE: CPU Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0> 6 11 26
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0> 6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0> 6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0> 6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0> 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 6 11 26
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0> 6 11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8> 6 11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16> 6 11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24> 6 11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32> 6 11 26 27
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40> 6 11 27
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48> 6 11 27
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56> 6 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 6 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 6 11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 6 11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 6 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 6 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 6 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 6 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 6 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 6 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 6 11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 6 11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 6 11 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 6 11 26 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 6 11 26 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 6 11 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 6 11 27
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0> 6 11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0> 6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0> 6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0> 6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0> 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 6 11 28
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0> 6 11 27
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8> 6 11 27
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16> 6 11 27
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24> 6 11 27
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32> 6 11 27 28
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40> 6 11 27
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48> 6 11 27
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56> 6 11 27
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 6 11 27
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 6 11 27
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 6 11 27
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 6 11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 6 11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 6 11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 6 11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 6 11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 6 11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 6 11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 6 11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 6 11 27
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 6 11 27 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 6 11 27 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 6 11 27
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 6 11 27

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
LVDS	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
LVDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	ISL3,ISL4,ISL9,ISL10	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P 8 17 83
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N 8 17 83
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P 18 87
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N 18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0> 18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0> 18 87
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAP<3> 8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAN<3> 8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0> 18 87
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0> 18 87
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P 16 41
	SATA_90D	SATA	SATA_HDD_R2D_C_N 16 41
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_P 6 41
	SATA_90D	SATA	SATA_HDD_R2D_N 6 41
T21 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_UF_P 41
T21	SATA_90D	SATA	SATA_HDD_R2D_UF_N 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P 16 41
	SATA_90D	SATA	SATA_HDD_D2R_N 16 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_C_P 6 41
	SATA_90D	SATA	SATA_HDD_D2R_C_N 6 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P 16 41
	SATA_90D	SATA	SATA_ODD_R2D_C_N 16 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P 6 41
	SATA_90D	SATA	SATA_ODD_R2D_N 6 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P 16 41
	SATA_90D	SATA	SATA_ODD_D2R_N 16 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_UF_P 6 41
	SATA_90D	SATA	SATA_ODD_D2R_UF_N 6 41
T21 PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP 16
T21 PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP 16
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P 18 24
	USB_85D	USB	USB_HUB1_UP_N 18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P 18 24
	USB_85D	USB	USB_HUB2_UP_N 18 24
USB_EXTA	USB_85D	USB	USB_EXTA_P 24 42
	USB_85D	USB	USB_EXTA_N 24 42
USB_EXTB	USB_85D	USB	USB_EXTB_P 24 42
	USB_85D	USB	USB_EXTB_N 24 42
USB_EXTC	USB_85D	USB	USB_EXTC_P 8 24
	USB_85D	USB	USB_EXTC_N 8 24
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P 6 31
	USB_85D	USB	USB_CAMERA_CONN_N 6 31
USB_BT	USB_85D	USB	USB_BT_P 24 31
	USB_85D	USB	USB_BT_N 24 31
USB_TPAD	USB_85D	USB	USB_TPAD_P 24 52
	USB_85D	USB	USB_TPAD_N 24 52
USB_IR	USB_85D	USB	USB_IR_P 24 43
	USB_85D	USB	USB_IR_N 24 43
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS 18
T21 USB_T29A	USB_85D	USB	USB_T29A_P 8 24
T21	USB_85D	USB	USB_T29A_N 8 24

SYNC_MASTER=K92_MLB SYNC_DATE=08/09/2010

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
LPC_AD	LPC_50S	LPC	LPC AD<3..0>	6 16 44 46 87
LPC_FRAME_L	LPC_50S	LPC	LPC FRAME L	6 16 44 46 87
LPC_RESET_L	LPC_50S	LPC	LPCPLUS RESET L	6 25 46 87
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC R	18 25
	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC	25 44
	CLK_LPC_50S	CLK_LPC	LPC CLK33M LPCPLUS	6 25 46
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS PCH CLK	16 23 26 28 30 41 47 61 88
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS PCH DATA	16 23 26 28 30 41 47 61 88
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML PCH 0 CLK	16 47
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML PCH 0 DATA	16 47
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML PCH 1 CLK	16 47
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML PCH 1 DATA	16 47
HDA_BIT_CLK	HDA_50S	HDA	HDA BIT CLK	16 56
	HDA_50S	HDA	HDA BIT CLK R	16
HDA_SYNC	HDA_50S	HDA	HDA SYNC	16 56
	HDA_50S	HDA	HDA SYNC R	16
HDA_RST_L	HDA_50S	HDA	HDA RST R L	16
	HDA_50S	HDA	HDA RST L	16 56
HDA_SDIN0	HDA_50S	HDA	HDA SDIN0	16 56
	HDA_50S	HDA	AUD SDI R	56
HDA_SDOUT	HDA_50S	HDA	HDA SDOUT	16 56
	HDA_50S	HDA	HDA SDOUT R	16
SPI_CLK	SPI_55S	SPI	SPI CLK R	16 46
	SPI_55S	SPI	SPI CLK	46
SPI_MOSI	SPI_55S	SPI	SPI MOSI R	16 46
	SPI_55S	SPI	SPI MOSI	46
SPI_MISO	SPI_55S	SPI	SPI MISO	16 46
SPI_CS0	SPI_55S	SPI	SPI CS0 R L	16 46
	SPI_55S	SPI	SPI CS0 L	46
	PCIE_85D	PCIE	PCIE ENET R2D P	36
	PCIE_85D	PCIE	PCIE ENET R2D N	36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE ENET R2D C P	16 36
	PCIE_85D	PCIE	PCIE ENET R2D C N	16 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE ENET D2R P	16 36
	PCIE_85D	PCIE	PCIE ENET D2R N	16 36
	PCIE_85D	PCIE	PCIE ENET D2R C P	36
	PCIE_85D	PCIE	PCIE ENET D2R C N	36
	PCIE_85D	PCIE	PCIE AP R2D P	6 31
	PCIE_85D	PCIE	PCIE AP R2D N	6 31
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D C P	16 31
	PCIE_85D	PCIE	PCIE AP R2D C N	16 31
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R P	6 16 31
	PCIE_85D	PCIE	PCIE AP D2R N	6 16 31
	PCIE_85D	PCIE	PCIE FW R2D P	38
	PCIE_85D	PCIE	PCIE FW R2D N	38
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE FW R2D C P	16 38
	PCIE_85D	PCIE	PCIE FW R2D C N	16 38
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE FW D2R P	16 38
	PCIE_85D	PCIE	PCIE FW D2R N	16 38
	PCIE_85D	PCIE	PCIE FW D2R C P	38
	PCIE_85D	PCIE	PCIE FW D2R C N	38
T25	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M PCH P	16
T25	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M PCH N	16
T26 PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 P	16 33
T26	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 N	16 33
T25	CLK_PCIE_90D	CLK_PCIE	PCH CLK96M DOT P	16
T25	CLK_PCIE_90D	CLK_PCIE	PCH CLK96M DOT N	16
T25	CLK_PCIE_90D	CLK_PCIE	PCH CLK100M SATA P	16
T25	CLK_PCIE_90D	CLK_PCIE	PCH CLK100M SATA N	16
T25	CPU_50S	CLK_PCIE	PCH CLK14P3M REFCLK	16
T26	CPU_50S	CLK_PCIE	PCH CLK33M PCIIN	16 25
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG CLK100M P	16 73
	CLK_PCIE_90D	CLK_PCIE	PEG CLK100M N	16 73
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M ENET P	16 36
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M ENET N	16 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP P	16 31
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP N	16 31
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M FW P	16 38
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M FW N	16 38
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	NC PCIE CLK100M EXCARD P	8 16
	CLK_PCIE_90D	CLK_PCIE	NC PCIE CLK100M EXCARD N	8 16
T26 PCIE_T29_R2D	PCIE_85D	PCIE	PCIE T29 R2D C P<3..0>	8 9 33
T26 PCIE_T29_R2D	PCIE_85D	PCIE	PCIE T29 R2D C N<3..0>	8 9 33
T26 PCIE_T29_R2D	PCIE_85D	PCIE	PCIE T29 R2D P<3..0>	33
T26 PCIE_T29_R2D	PCIE_85D	PCIE	PCIE T29 R2D N<3..0>	33
T26 PCIE_T29_D2R	PCIE_85D	PCIE	PCIE T29 D2R P<3..0>	8 9 33
T26 PCIE_T29_D2R	PCIE_85D	PCIE	PCIE T29 D2R N<3..0>	8 9 33
T27 PCIE_T29_D2R	PCIE_85D	PCIE	PCIE T29 D2R C P<3..0>	33
T26 PCIE_T29_D2R	PCIE_85D	PCIE	PCIE T29 D2R C N<3..0>	33

SYNC_MASTER=K92_MLB SYNC_DATE=08/09/2010

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CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR	*	=3X_DIELECTRIC	?

SOURCE: Attila Farkas Email - 8/2/10

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	
	ENET_50S	ENET_3X	ENET_RESET_L	32 36
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	36 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	36 37
CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_DATA_R<7..0>	
CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_CMD_R	32
CR_CLK	ENET_50S	ENET_CR	SDCONN_CLK_R	32
CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_DATA<7..0>	32 36
CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_CMD	32 36
CR_CLK	ENET_50S	ENET_CR	SDCONN_CLK	32 36
CR_CLK	ENET_50S	ENET_CR	SDCONN_CLK_R_L	32

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP	6 38 40
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAN	38 40
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBP	6 38 40
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBN	6 38 40
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	38 40
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	38 40
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	38 40
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	38 40

Port 2 Not Used

SYNC_MASTER=K91_ERIC SYNC_DATE=08/03/2010

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius’s T29 Routing Notes

T29/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0>	6 84
T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0>	6 84
T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1>	6 84
T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1>	6 84
	T29DP_80D	T29DP	T29_R2D_C_F_P<1..0>	84
	T29DP_80D	T29DP	T29_R2D_C_F_N<1..0>	84
T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_P<0>	6 84 85
T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_N<0>	6 84 85
T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_P<1>	6 84 85
T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_N<1>	6 84 85
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P	6 85
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N	6 85
	T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>	6 84
	T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>	6 84
	T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>	84
	T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>	84
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2>	6 84 95
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2>	6 84 95
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2>	84
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2>	84
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P	84
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N	84
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P	84
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N	84
	T29DP_80D	T29DP	T29DPA_ML_P<3..0>	6 84 85
	T29DP_80D	T29DP	T29DPA_ML_N<3..0>	6 84 85
	T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>	84 85
	T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>	84 85
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_P	84 85
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_N	84 85
T29_R2D2	T29DP_80D	T29DP	T29_R2D_P<2>	
T29_R2D2	T29DP_80D	T29DP	T29_R2D_N<2>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D_P<3>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D_N<3>	
	T29DP_80D	T29DP	T29_R2D_C_F_P<3..2>	
	T29DP_80D	T29DP	T29_R2D_C_F_N<3..2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_P<2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_N<2>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_P<3>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_N<3>	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>	
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2>	95
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2>	95
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>	
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N	
	T29DP_80D	T29DP	T29DPB_ML_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_N<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_P	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_N	

Only used on dual-port hosts.

T29 IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	6 33 78
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	6 33
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	6 33 78
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	6 33
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	6 33 78
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	6 33
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	6 33 78
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	6 33
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N	
	T29_I2C_55S	T29_I2C	I2C_T29_SCL	33 47 84
	T29_I2C_55S	T29_I2C	I2C_T29_SDA	33 47 84
T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	33
T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	33
T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	33
T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	33
	T29DP_80D	T29DP	T29_R2D_C_P<3..0>	6 8 33 84
	T29DP_80D	T29DP	T29_R2D_C_N<3..0>	6 8 33 84
	T29DP_100D	T29DP	T29_D2R_P<3..0>	6 8 33 84
	T29DP_100D	T29DP	T29_D2R_N<3..0>	6 8 33 84

Only used on hosts supporting T29 video-in

SYNC_MASTER=T29_REF SYNC_DATE=10/16/2010

PAGE TITLE: T29 Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL 6 31 44 47 53 54
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA 6 31 44 47 53 54
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL 44 47 50
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA 44 47 50
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL 6 31 44 47 50 79
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA 6 31 44 47 50 79
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL 6 44 47 62 63
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA 6 44 47 62 63
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL 44 47 100
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA 44 47 100

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P 63
	1TO1_DIFFPAIR		CHGR_CSI_N 63
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P 63
	1TO1_DIFFPAIR		CHGR_CSO_N 63

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: SMC Constraints

Apple Inc.

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=2x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P	75 76
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N	75 76
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P	75 76
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_A<8..0>	6 75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_A<8..0>	6 75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_ABI_L	6 75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_ABI_L	6 75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_RAS_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_RAS_L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CAS_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CAS_L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_WE_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_WE_L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CKE_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CKE_L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CS_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CS_L	75 76
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0>	6 75 76
FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1>	6 75 76
FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2>	6 75 76
FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3>	6 75 76
FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0>	6 75 76
FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1>	6 75 76
FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2>	6 75 76
FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3>	6 75 76
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0>	6 75 76
FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1>	6 75 76
FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2>	6 75 76
FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3>	6 75 76
FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0>	6 75 76
FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1>	6 75 76
FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2>	6 75 76
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3>	6 75 76
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<0>	6 75 76
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<0>	6 75 76
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<1>	6 75 76
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<1>	6 75 76
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<0>	6 75 76
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<0>	6 75 76
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<1>	6 75 76
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<1>	6 75 76
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0>	6 75 76
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8>	6 75 76
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16>	6 75 76
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24>	6 75 76
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0>	6 75 76
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8>	6 75 76
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16>	6 75 76
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24>	6 75 76
FB_AB_RESET	GDDR5_45R50SE	GDDR5_CMD	FB_RESET_L	75 76 77

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P	75 77
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N	75 77
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P	75 77
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_A<8..0>	6 75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_A<8..0>	6 75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_ABI_L	6 75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_ABI_L	6 75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_RAS_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_RAS_L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CAS_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CAS_L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_WE_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_WE_L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CKE_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CKE_L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CS_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CS_L	75 77
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>	6 75 77
FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>	6 75 77
FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>	6 75 77
FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>	6 75 77
FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>	6 75 77
FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>	6 75 77
FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>	6 75 77
FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>	6 75 77
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>	6 75 77
FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>	6 75 77
FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>	6 75 77
FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>	6 75 77
FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>	6 75 77
FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>	6 75 77
FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>	6 75 77
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>	6 75 77
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>	6 75 77
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>	6 75 77
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>	6 75 77
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>	6 75 77
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>	6 75 77
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>	6 75 77
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>	6 75 77
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>	6 75 77
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>	6 75 77
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>	6 75 77
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>	6 75 77
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>	6 75 77
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>	6 75 77
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>	6 75 77
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>	6 75 77
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>	6 75 77

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_P	83 87
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_N	83 87
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_P<2..0>	83 87
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_N<2..0>	83 87
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_P	83 87
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_N	83 87
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_P<2..0>	83 87
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_N<2..0>	83 87
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_P	6 82
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_N	6 82
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_P	6 82
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_N	6 82
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_P	82 83
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_N	82 83
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_P<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_N<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_P	82 83
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_N	82 83
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_P<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_N<2..0>	6 82 83

Whistler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	78 79
GPU_CLK100M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK100M	78 79
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_P	78 87
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_N	78 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<2..0>	78 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<2..0>	78 87
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_P<3>	78 79
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_N<3>	78 79
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<2..0>	78 87
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<2..0>	78 87
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_P<3>	78 79
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_N<3>	78 79
DP_MI	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	78 84
	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	78 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	83 84
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	83 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUXCH_P	8 78 83
	DP_85D	DISPLAYPORT	DP_EG_AUXCH_N	8 78 83

SYNC_MASTER=K92_MLB SYNC_DATE=08/09/2010

PAGE TITLE: GPU (Whistler) CONSTRAINTS

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K91 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	50
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	50
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 50
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 50
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	50
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	50
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	50 78
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	50 78
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	48 64
	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	48 64
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_P	48
	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_N	48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_P	48
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_N	48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	48 69
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	48 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_P	48
	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_N	48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_N	48
	SENSE_1TO1_55S	SENSE	GPUISENS_P	48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	48 66
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	48 66
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	98
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	98
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	98
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	98
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	100
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	
	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	100
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	
	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	100
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_P	
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_P	100
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_N	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_P	
	SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_R_P	100
	SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_R_N	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_P	
	SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_R_P	100
	SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_R_N	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	49 68
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	49 68
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	49
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P	49
	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	49
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	49
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	56 59
	AUDIODIFF	AUDIO	AUD_LO1_R_N	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	56 59
	AUDIODIFF	AUDIO	AUD_LO2_L_N	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	56 59
	AUDIODIFF	AUDIO	AUD_LO2_R_N	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	59
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	59
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_SUBIN_P	59
	AUDIODIFF	AUDIO	AUD_SPKRAMP_SUBIN_N	59

K91 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 31
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 31
	1TO1_DIFFPAIR		CHGR_CSI_R_P	63
	1TO1_DIFFPAIR		CHGR_CSI_R_N	63
	1TO1_DIFFPAIR		CHGR_CSO_R_P	49 63
	1TO1_DIFFPAIR		CHGR_CSO_R_N	49 63
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	42
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	42
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	6 42
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	6 42
	USB_85D	USB	CONN_USB2_BT_P	6
	USB_85D	USB	CONN_USB2_BT_N	6
	USB_85D	USB	USB_LT2_P	6 42
	USB_85D	USB	USB_LT2_N	6 42
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375L_P	59
	AUDIODIFF	AUDIO	SSM2375L_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375R_P	59
	AUDIODIFF	AUDIO	SSM2375R_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375S_P	59
	AUDIODIFF	AUDIO	SSM2375S_N	59
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	6 59 60
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	6 59 60
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	6 59 60
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	6 59 60
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P	6 59 60
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N	6 59 60
	USB_85D	USB	USB_TPAD_R_P	52
	USB_85D	USB	USB_TPAD_R_N	52
		SB_POWER	PP3V3_S5	45 55 65 70 71 72 82 85 89 6 7 17 19 20 22 23 24 25 29 39
		SB_POWER	PP3V3_S0	48 49 50 51 53 56 60 61 71 72 6 7 12 16 17 18 19 20 22 23 25 75 83 84 87 88 89 41 45 47
		SB_POWER	PP1V5_S3RS0	75 82 83 84 87 88 89
		GND	GND	

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Project Specific Constraints

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K91 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.13 MM	0.13 MM			
45_OHM_SE	*	Y	0.099 MM	0.099 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

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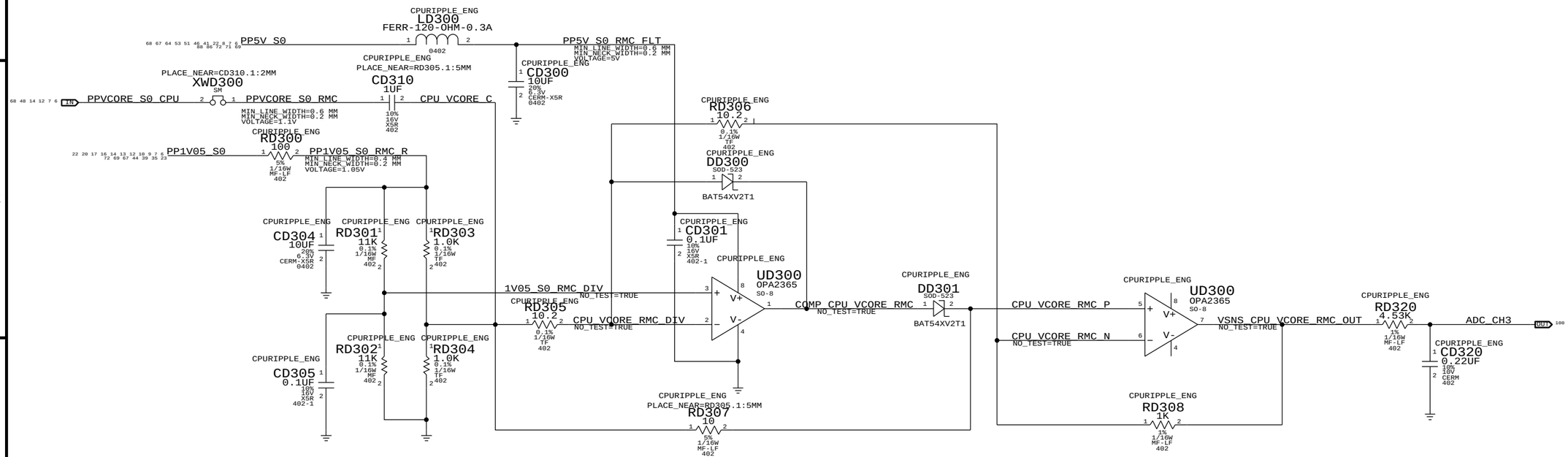

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