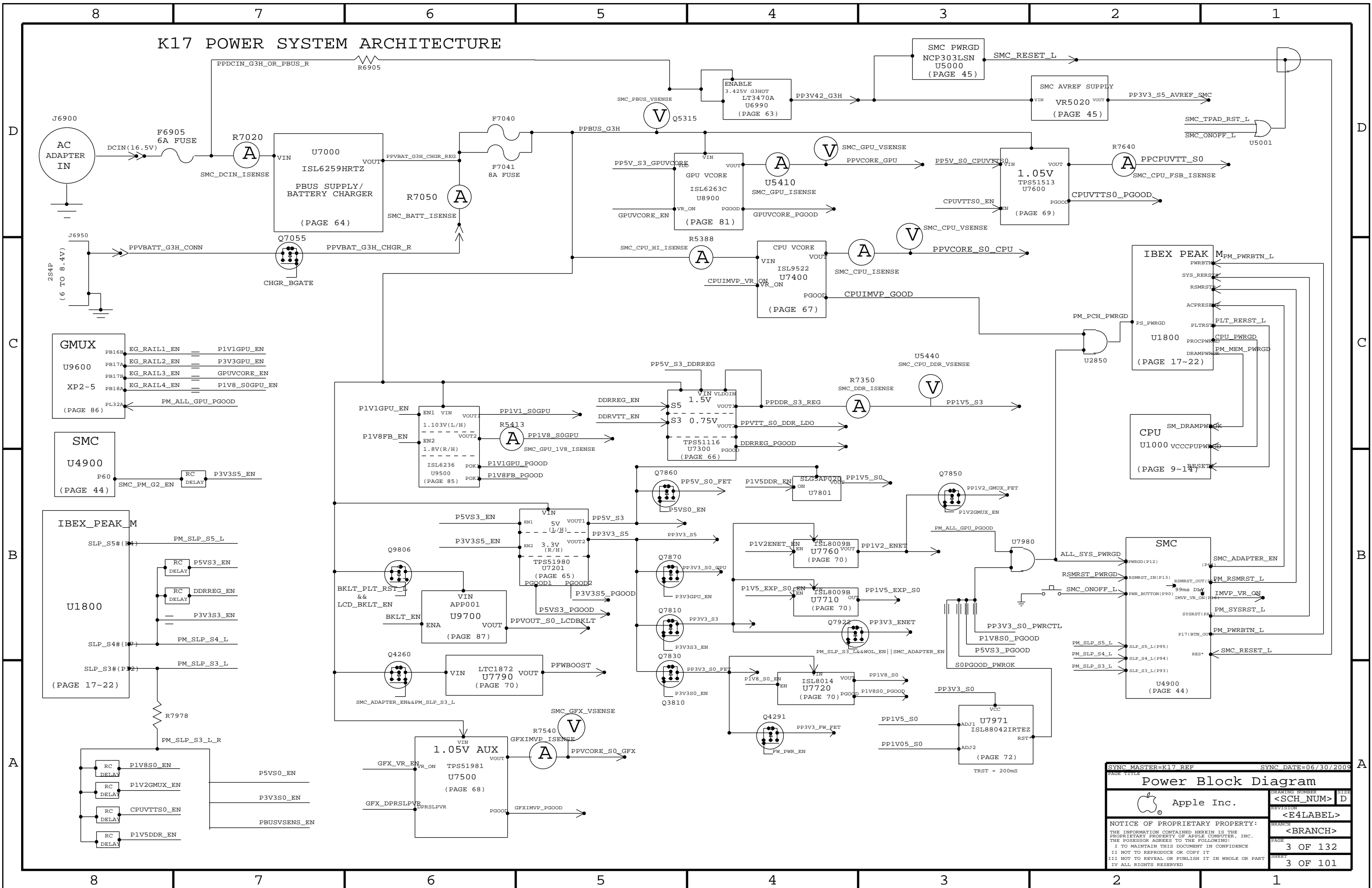


K17 POWER SYSTEM ARCHITECTURE



PAGE TITLE		PAGE NUMBER	
Power Block Diagram		3 OF 101	
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## BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0952	PCBA, 2.0G, 512SAM_VRAM, K18	K18_COMMON, CPU_2_4GHZ, FB_256_SAMSUNG, K18_PVT, EEEE_DCJ7
639-0953	PCBA, 2.0G, 512HYN_VRAM, K18	K18_COMMON, CPU_2_4GHZ, FB_256_HYNIX, K18_PVT, EEEE_DCJ8
639-0954	PCBA, 2.13G, 512SAM_VRAM, K18	K18_COMMON, CPU_2_53GHZ, FB_512_SAMSUNG, K18_PVT, EEEE_DCJ9
639-0955	PCBA, 2.13G, 512HYN_VRAM, K18	K18_COMMON, CPU_2_53GHZ, FB_512_HYNIX, K18_PVT, EEEE_DCJC
639-0956	PCBA, 2.4G, 512SAM_VRAM, K18	K18_COMMON, CPU_2_66GHZ, FB_512_SAMSUNG, K18_PVT, EEEE_DCJD
639-0957	PCBA, 2.4G, 512HYN_VRAM, K18	K18_COMMON, CPU_2_66GHZ, FB_512_HYNIX, K18_PVT, EEEE_DCJF
085-1404	K18 DEVELOPMENT BOM	

## K18 BOM GROUPS

BOM GROUP	BOM OPTIONS
K18_COMMON	ALTERNATE,COMMON,K18_COMMON1,K18_COMMON2,K18_PROGPARTS,USBHUB_2061,RDRV:8515A2,DCI
K18_COMMON1	BATT_3S,BCM5764M,GL137,CPUPOC_IMAX_40_50,CPUMEM_S0,SMC_EXCARD_NOT,SMC_DEBUG_YES,HUB1_2NONREM,HUB2_3NONREM
K18_COMMON2	GMUXPLL_3V3,GPU_SS_INT,MIKEY,GPUVID_0P90V,DPMUX_EN_PLD,DP_CA_DET_EG_PLD,DP_ESD,VFRQ_SLPS3,SMC_OSC_YES,RAIL_MON
K18_PVT	BMON_PROD,VREFMRGN_NOT,XDP,XDP_NORMAL,XDP_CPU_BPM
K18_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4, VRAM_256_SAMSUNG, FB1V55
FB_256_HYNIX	VRAM4, VRAM_256_HYNIX, FB1V55
FB_512_SAMSUNG	VRAM4, VRAM_512_SAMSUNG, FB1V35
FB_512_HYNIX	VRAM4, VRAM_512_HYNIX, FB1V35

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJ7]	CRITICAL	EEEE_DCJ7
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJ8]	CRITICAL	EEEE_DCJ8
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJ9]	CRITICAL	EEEE_DCJ9
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJC]	CRITICAL	EEEE_DCJC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJD]	CRITICAL	EEEE_DCJD
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJF]	CRITICAL	EEEE_DCJF

## Module Parts


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3848	1	ARD,SLBPE,PRQ,2.66G,35W,C2,3M,BGA	U1000	CRITICAL	CPU_2_66GHZ
337S3847	1	ARD,SLBPF,PRQ,2.53G,35W,C2,3M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3846	1	ARD,SLBNA,PRQ,2.4G,35W,C2,4M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3849	1	IC,PCH,IBEX PEAK-M,SLGZS,PRQ,B3,BGA	U1800	CRITICAL	
337S3839	1	IC,GPU,NV GT216 LP+,,969BGA,40NM,A03	U8000	CRITICAL	
343S0493	1	IC,ASIC,BCM5764M,ENET CONTROLLER,8x8,64 QFN	U3900	CRITICAL	BCM5764M
341S2731	1	IC,1MBIT,SPI FLASH,K17/K18	U3990	CRITICAL	
338S0753	1	IC,PW43-E2,1394R PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341T0233	1	IC,SMC,K18	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2562	1	IC,EFI ROM,DEVELOPMENT,K18	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
341S2616	1	IC,PSOC +W/USB,56PIN,MLF,K18	U5701	CRITICAL	TPAD_PROG
336S0025	1	IC,XP2-5,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_5K_BLANK
341S2566	1	IC,CPLD,LATTICE,132CSBGA,K18	U9600	CRITICAL	GMUX_PROG
333S0507	4	IC,SGRAM,GDDR3,16MX32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0483	4	IC,SDRAM,GDDR3,16MX32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX
333S0533	4	IC,SGRAM,GDDR3,32MX32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0535	4	IC,SDRAM,GDDR3,32MX32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_HYNIX

## Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1404	1	K18 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM

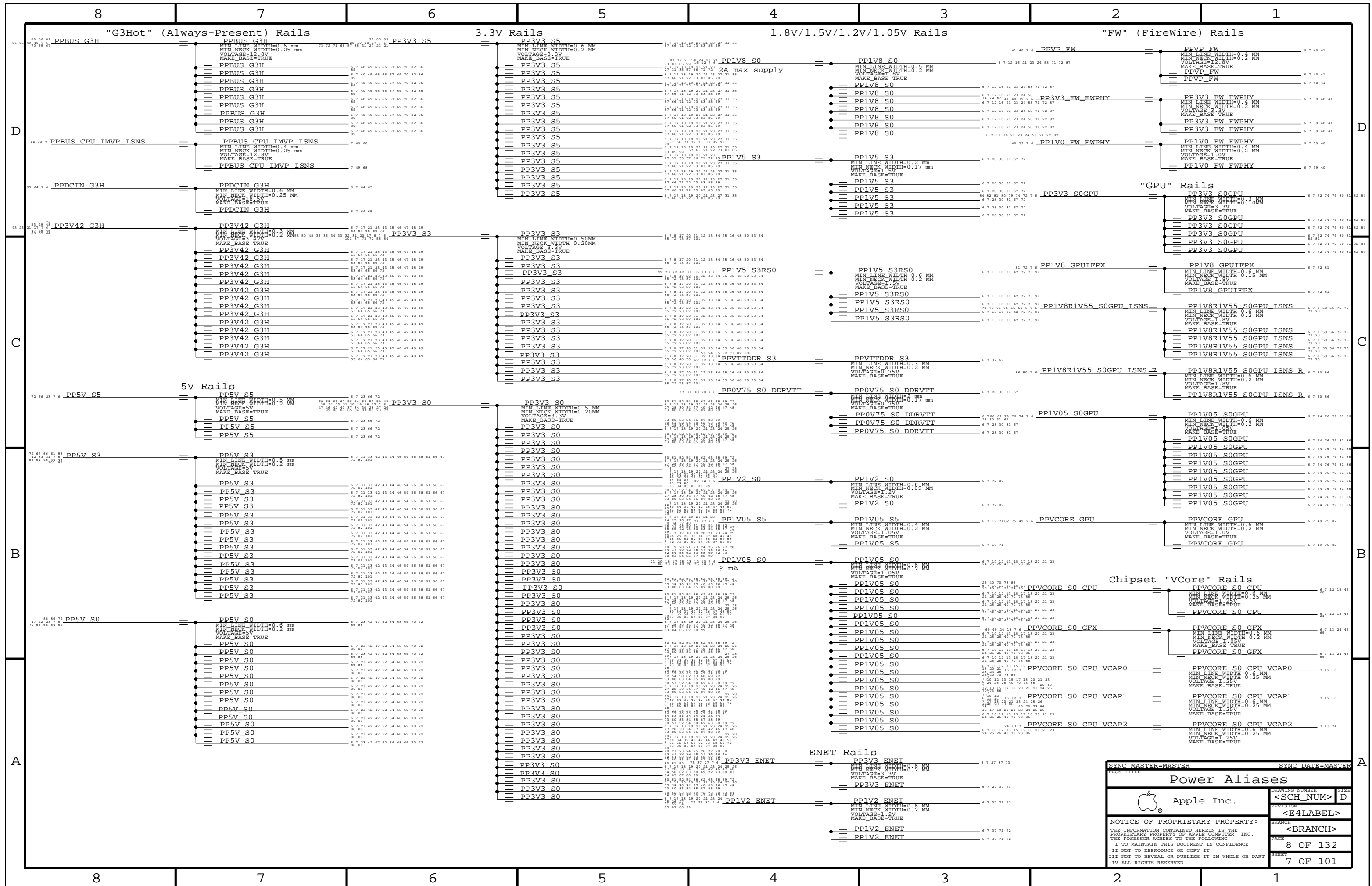
## Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYRTRC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
333S0506	333S0535		ALL	Synix 900M alt to 1000M
516S0805	516S0806		ALL	Molex alt to Foxconn
152S1102	152S1088		ALL	Mag layer alt to Vishay
333S2805	353S2603		ALL	Fairchild wafer option
333S0542	333S0507		ALL	Samsung i die alt to H
128S0264	128S0257		ALL	Sanyo alt to Kemet
128S0303	128S0282		ALL	Panasonic alt to Sanyo
337S3808	337S3839		ALL	A02 alt to A03 GPU
128S0305	128S0294		ALL	6.3V alt to 11V Sanyo

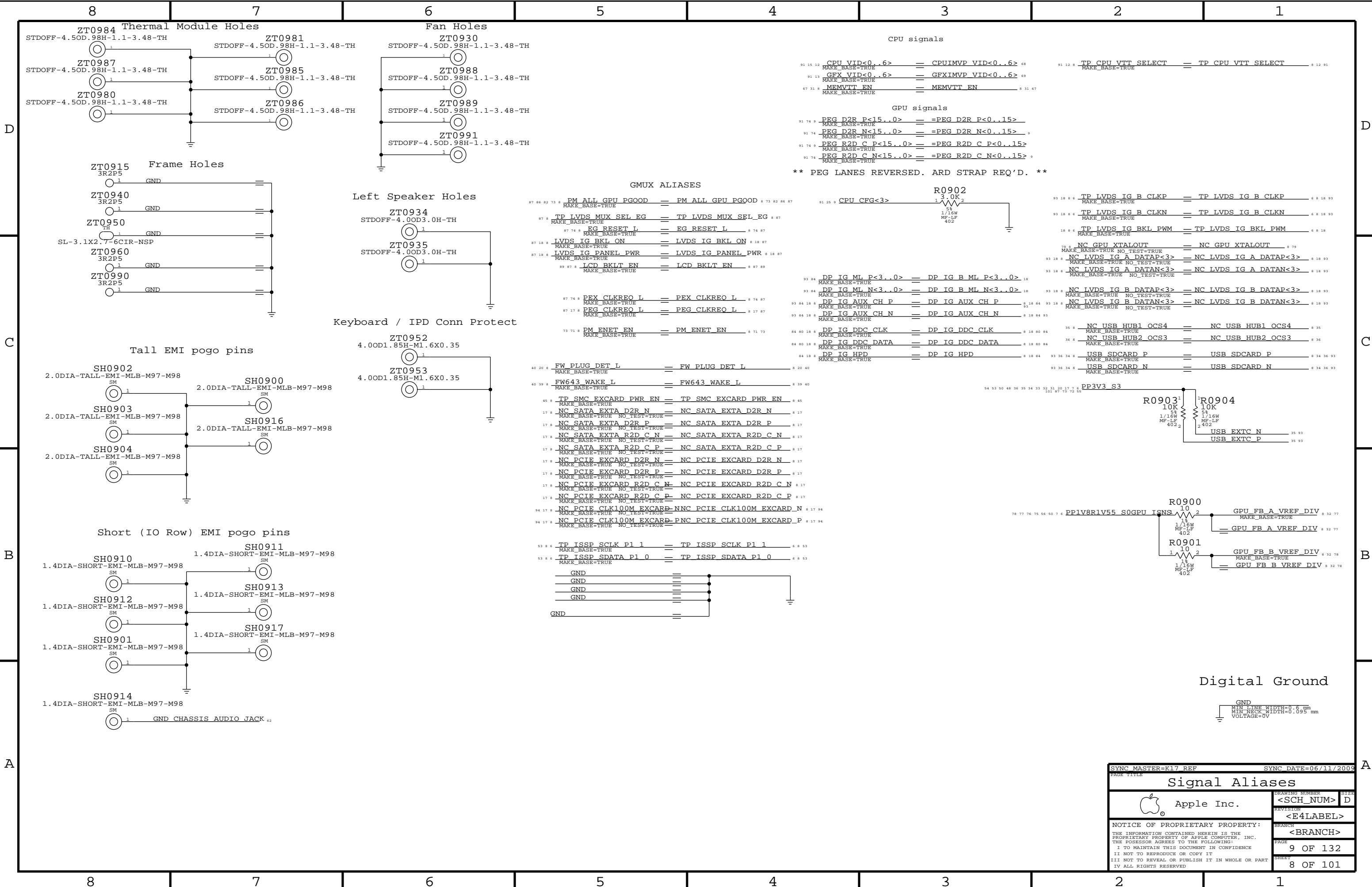
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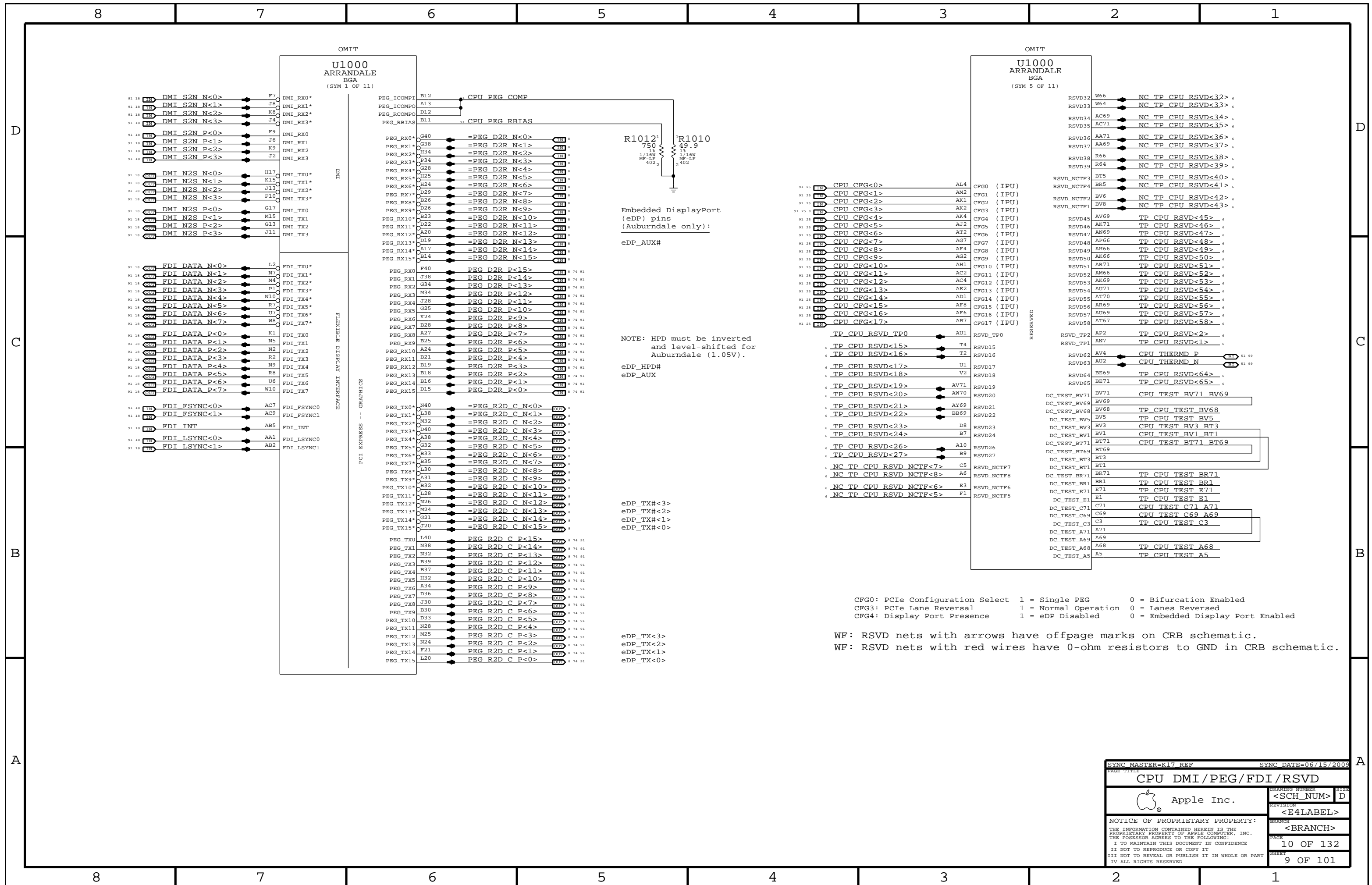


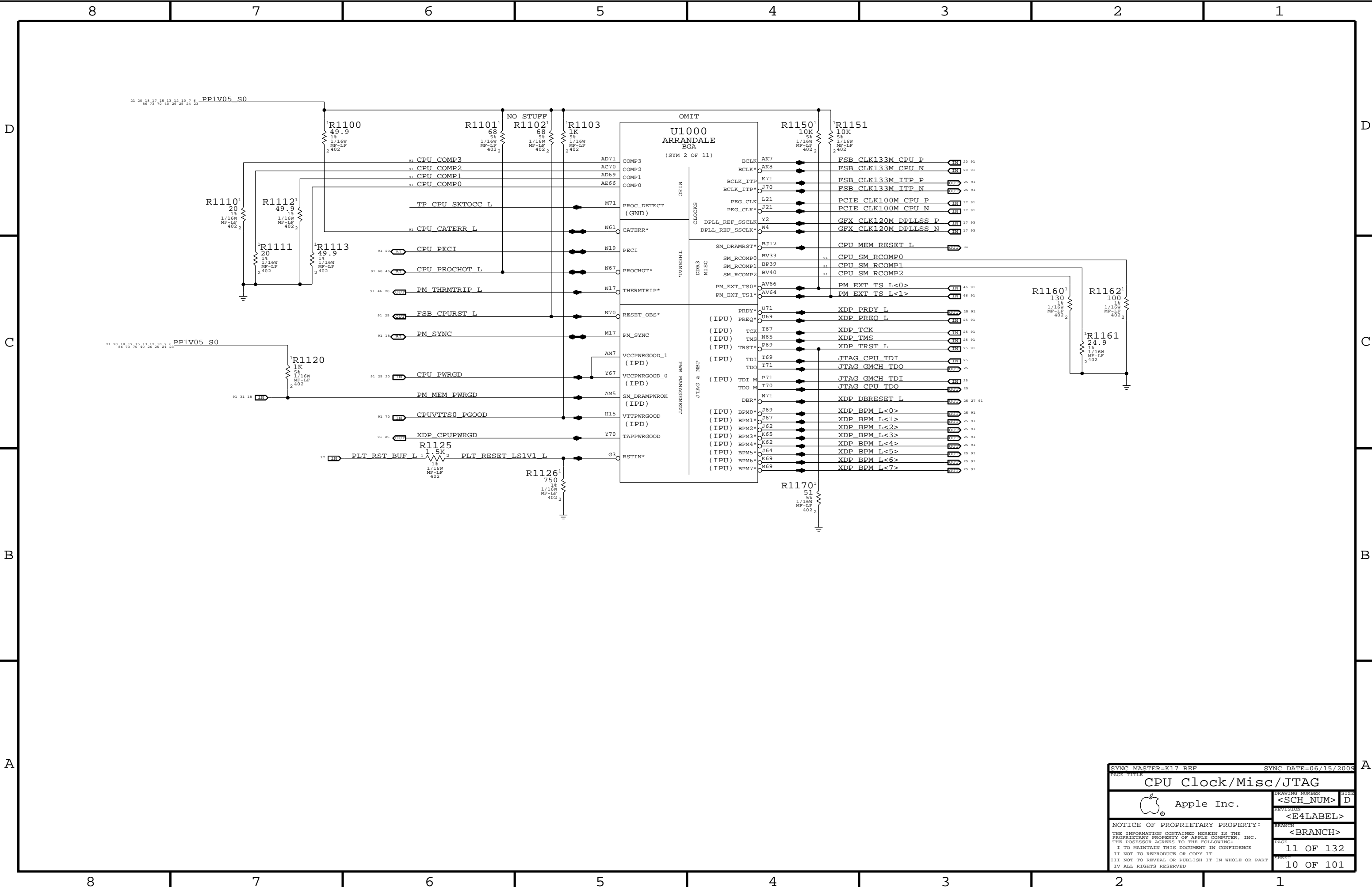


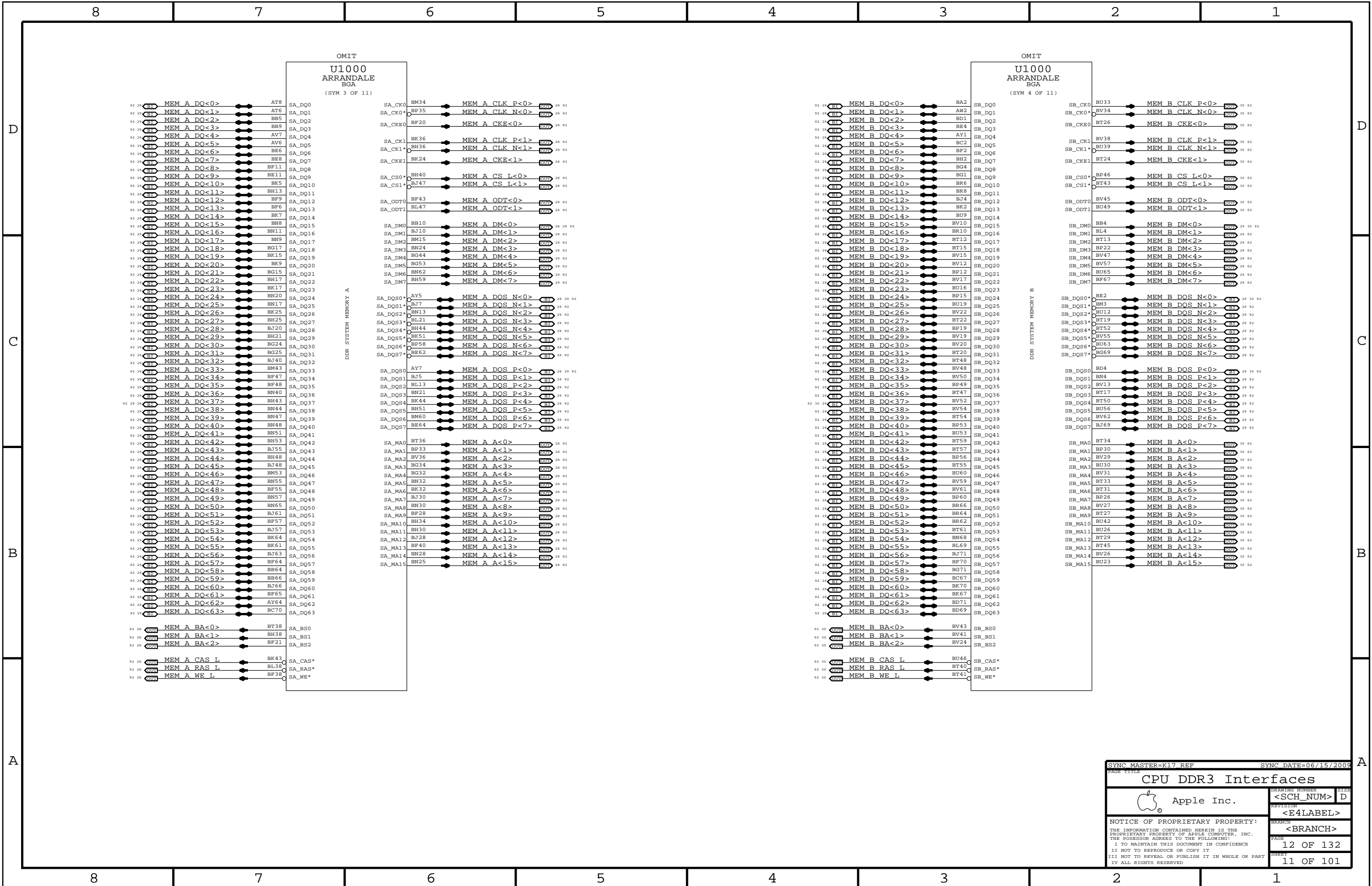


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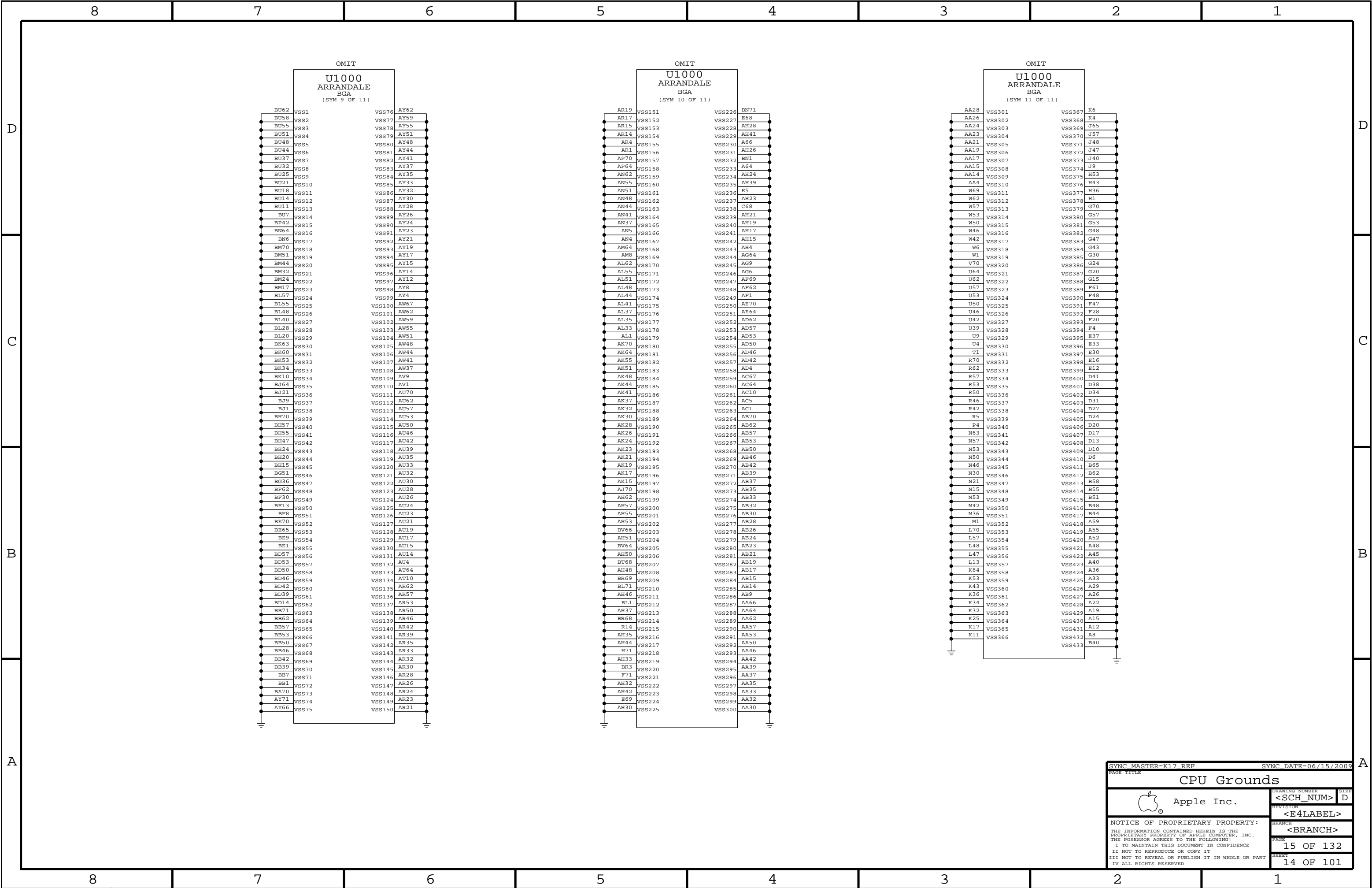













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CPU Grounds

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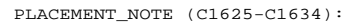
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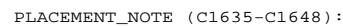
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4x 470uF 4.5mOhm, 3x 62uF B2, 10x 22uF 0603, 25x 1uF 0402

Place on bottom side of U1000..



NO STUFF	NO STUFF	
81605	81606	81607



3x 330uF 6 mOhm, 4x 22uF 0805, 7x 10uF 0603, 24x 1uF 0402

Place on bottom side of U1000

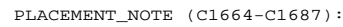
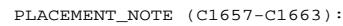
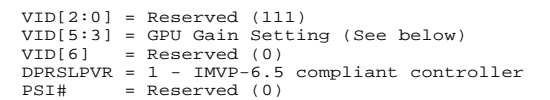


Figure 1: Schematic diagram of the test circuit. It shows three identical stages connected in series. Each stage consists of a 330uF capacitor (C1688, C1689, C1690) in parallel with a 20k resistor. The output of each stage is connected to the input of the next stage. The input voltage is 2.0V. The output voltage is measured across the 20k resistor. The circuit is labeled D2T-SM2.

Intel recommends all option straps should be provided in layout

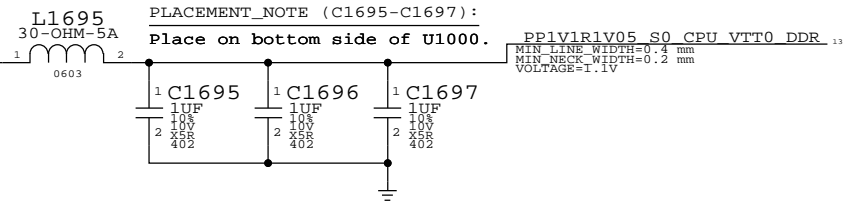


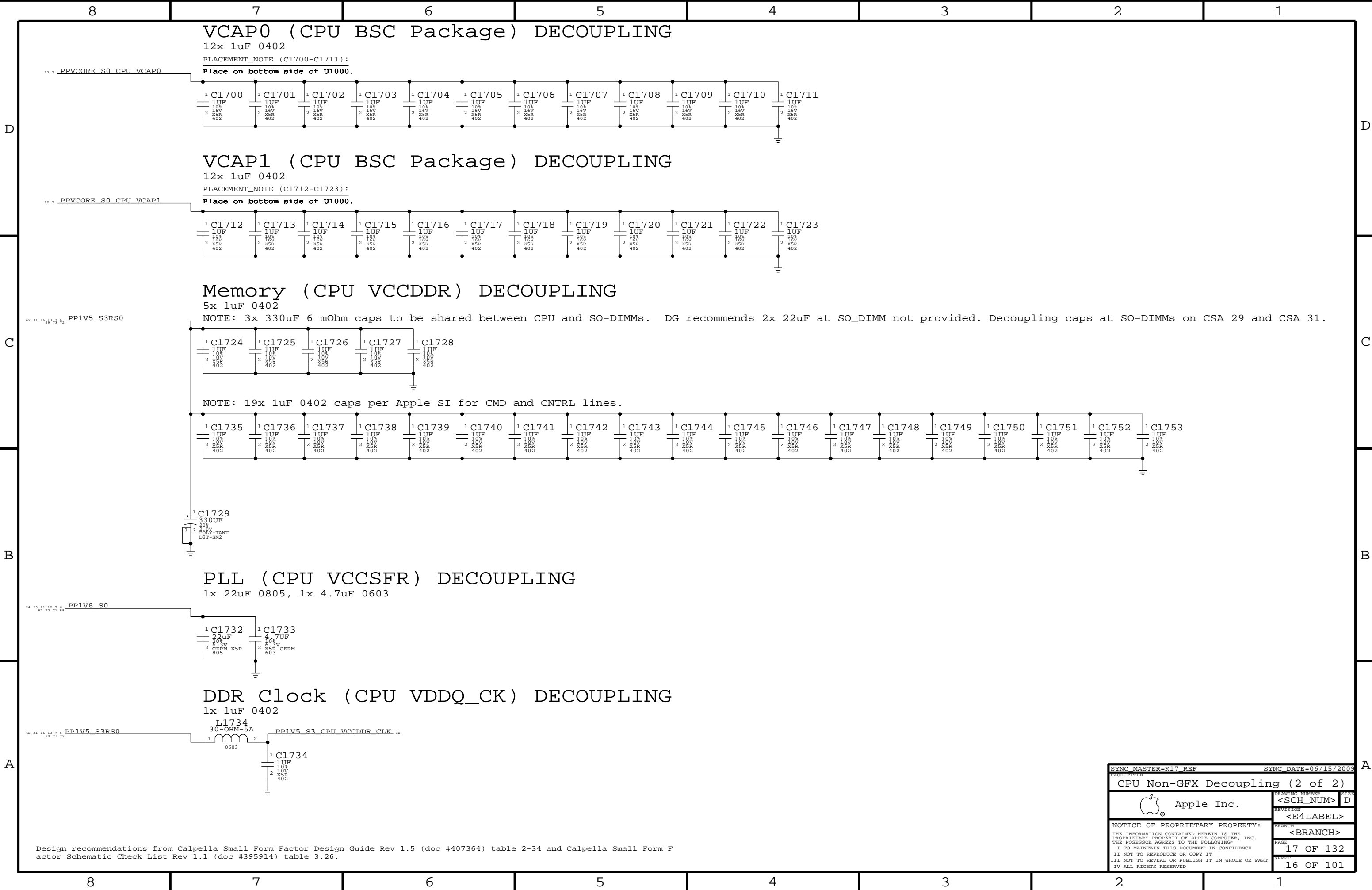
NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONS directly.  
Instead call out appropriate BOM GROUP defined in tables above.

3x 1uF 0402

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Place on bottom side of U1000

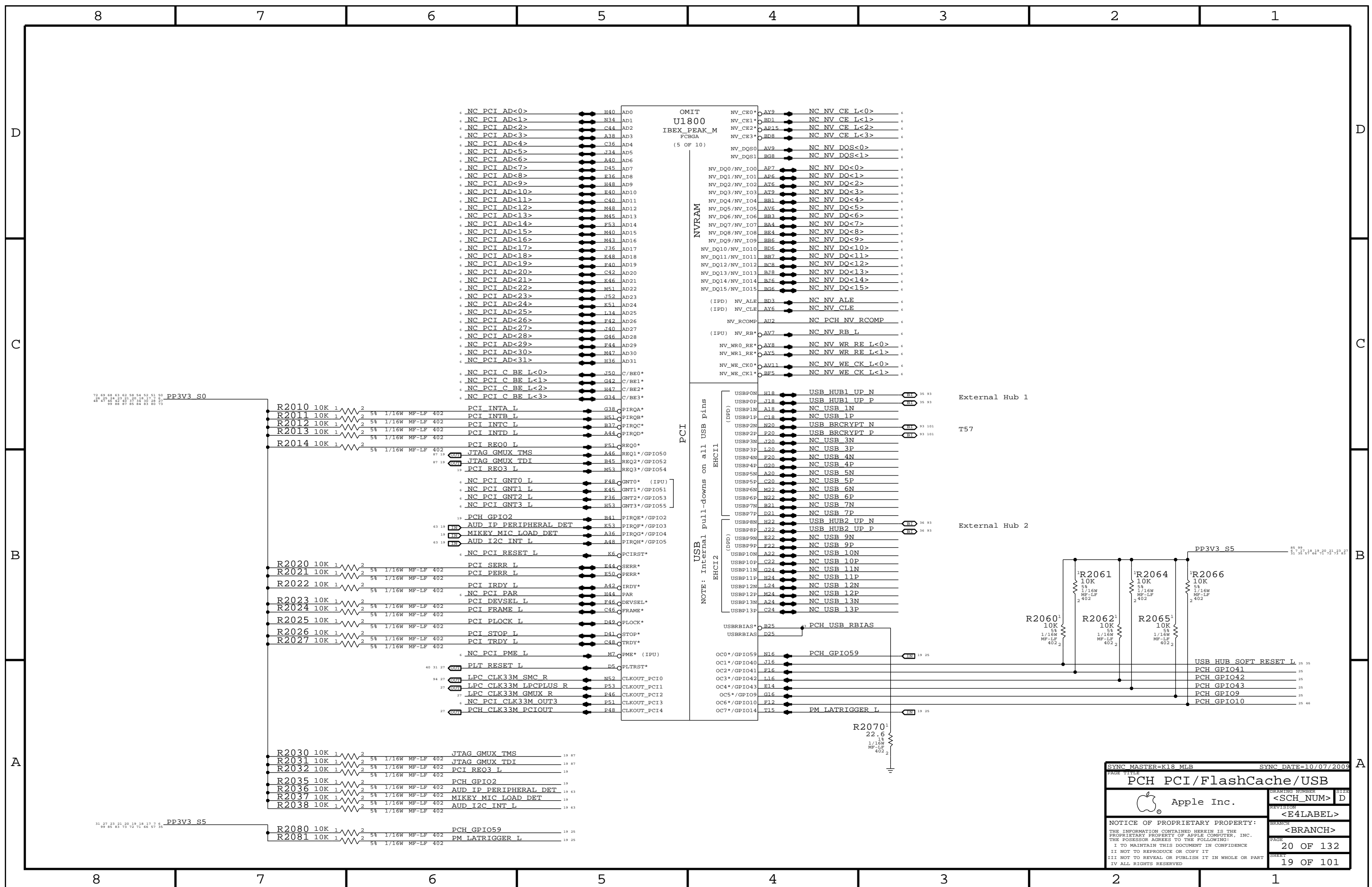




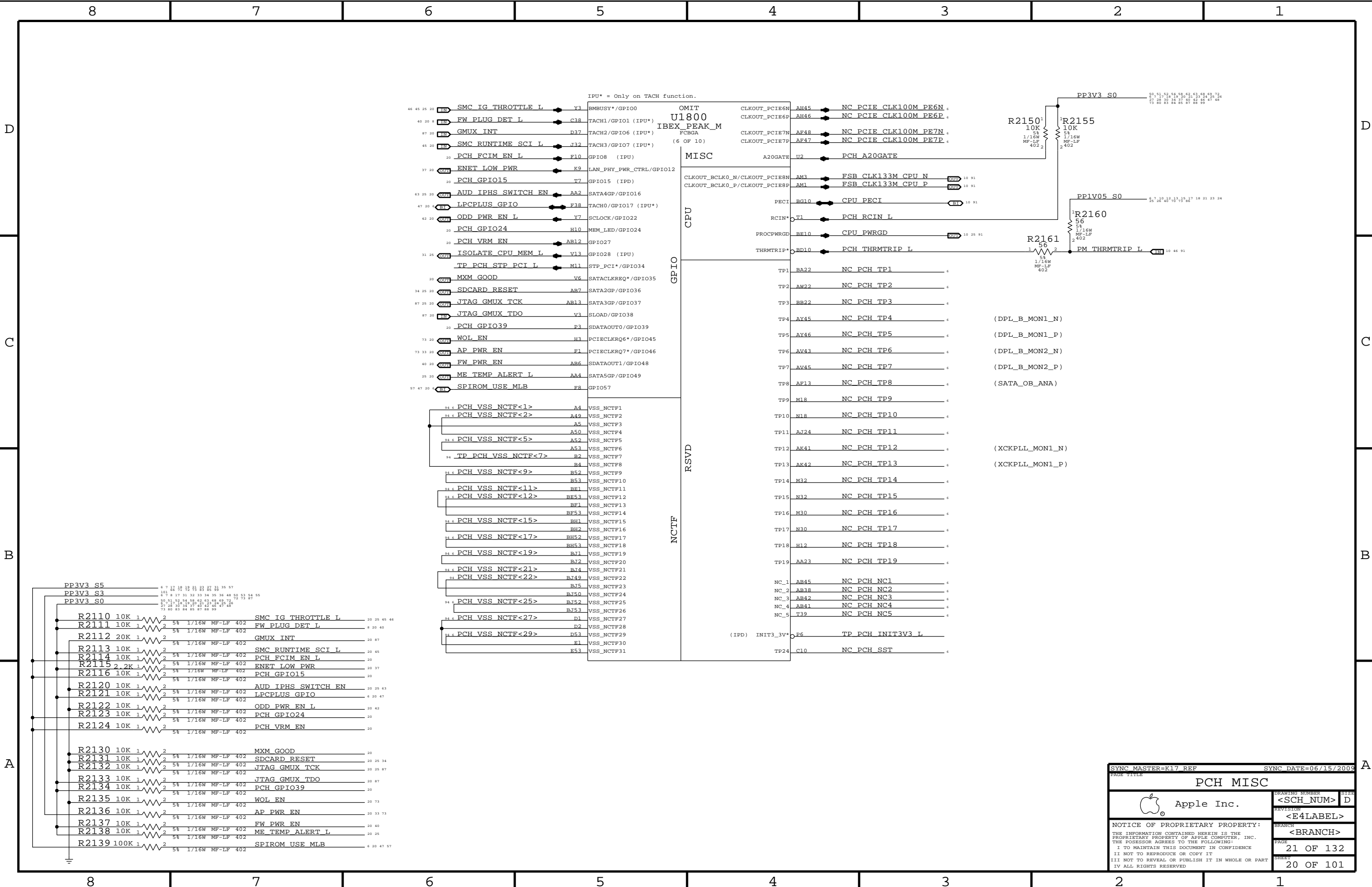







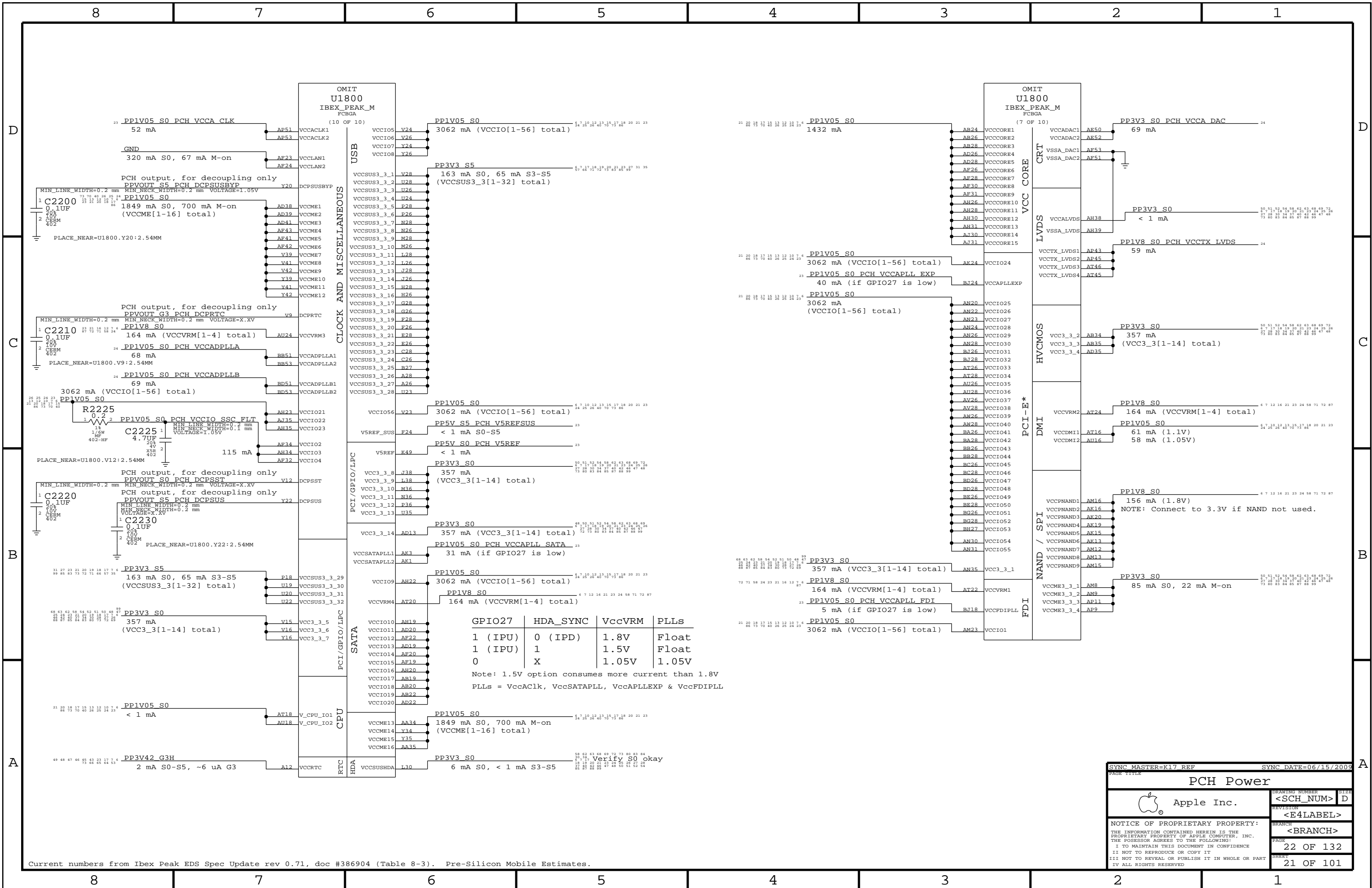






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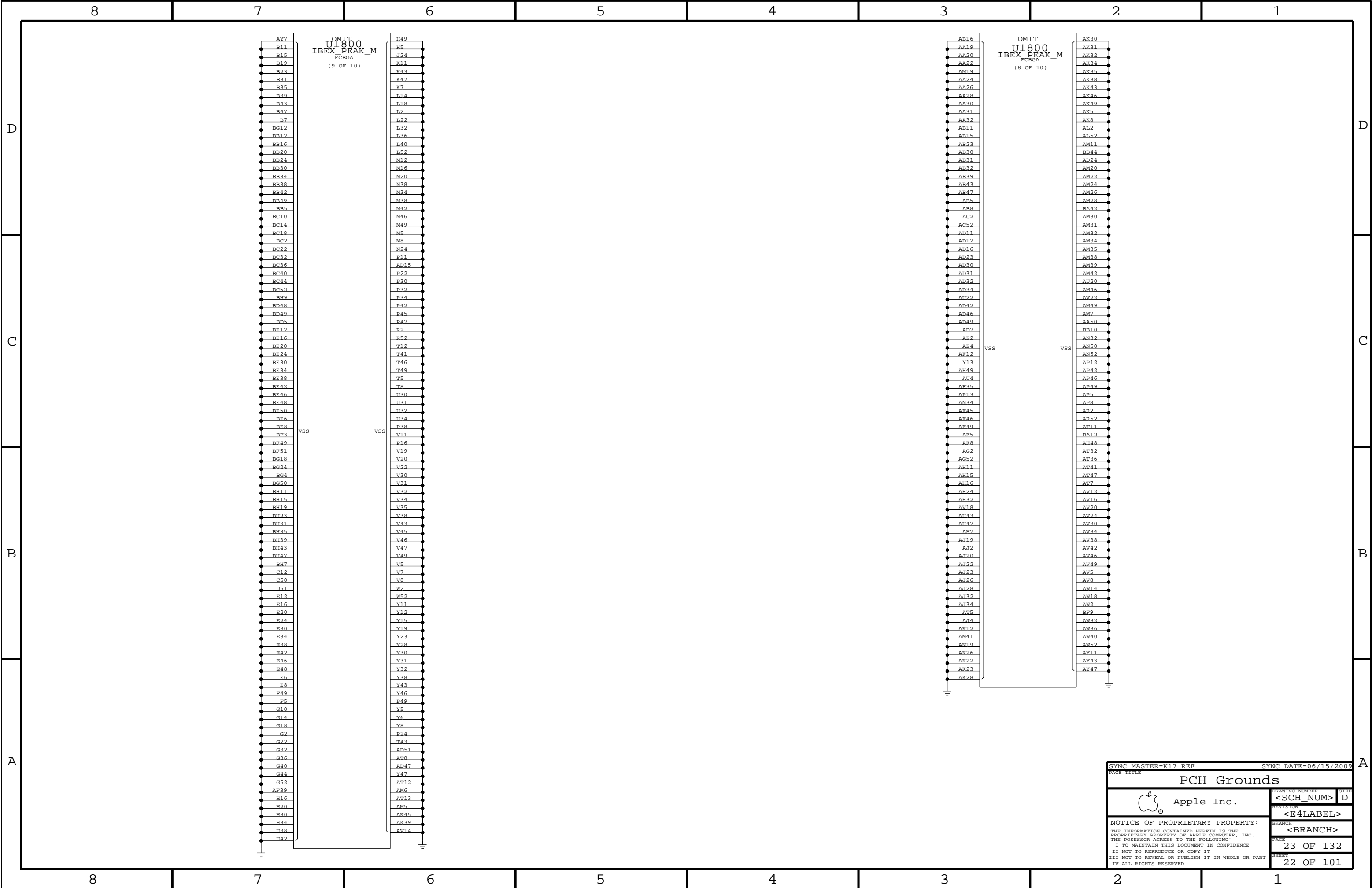
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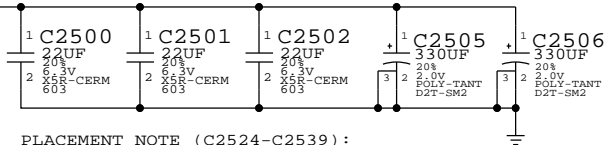


GFX (CPU VCCAXG) DECOUPLING

3x 330uF 6 mOhm (2 stuffed), 3x 22uF 0603, 16x 1uF 0402

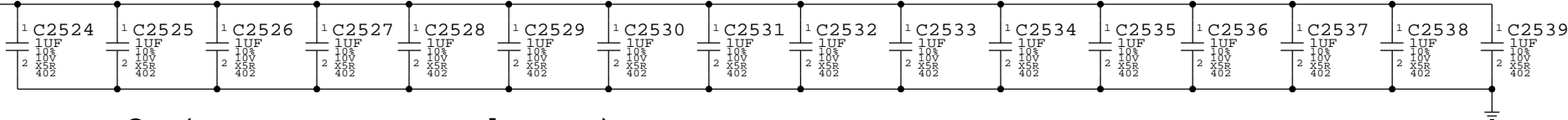
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Place on bottom side of U1000.



PLACEMENT\_NOTE (C2524-C2539):

Place on bottom side of U1000.

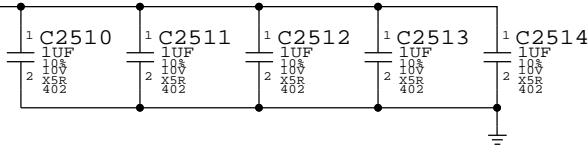


VCAP2 (CPU BSC Package) DECOUPLING

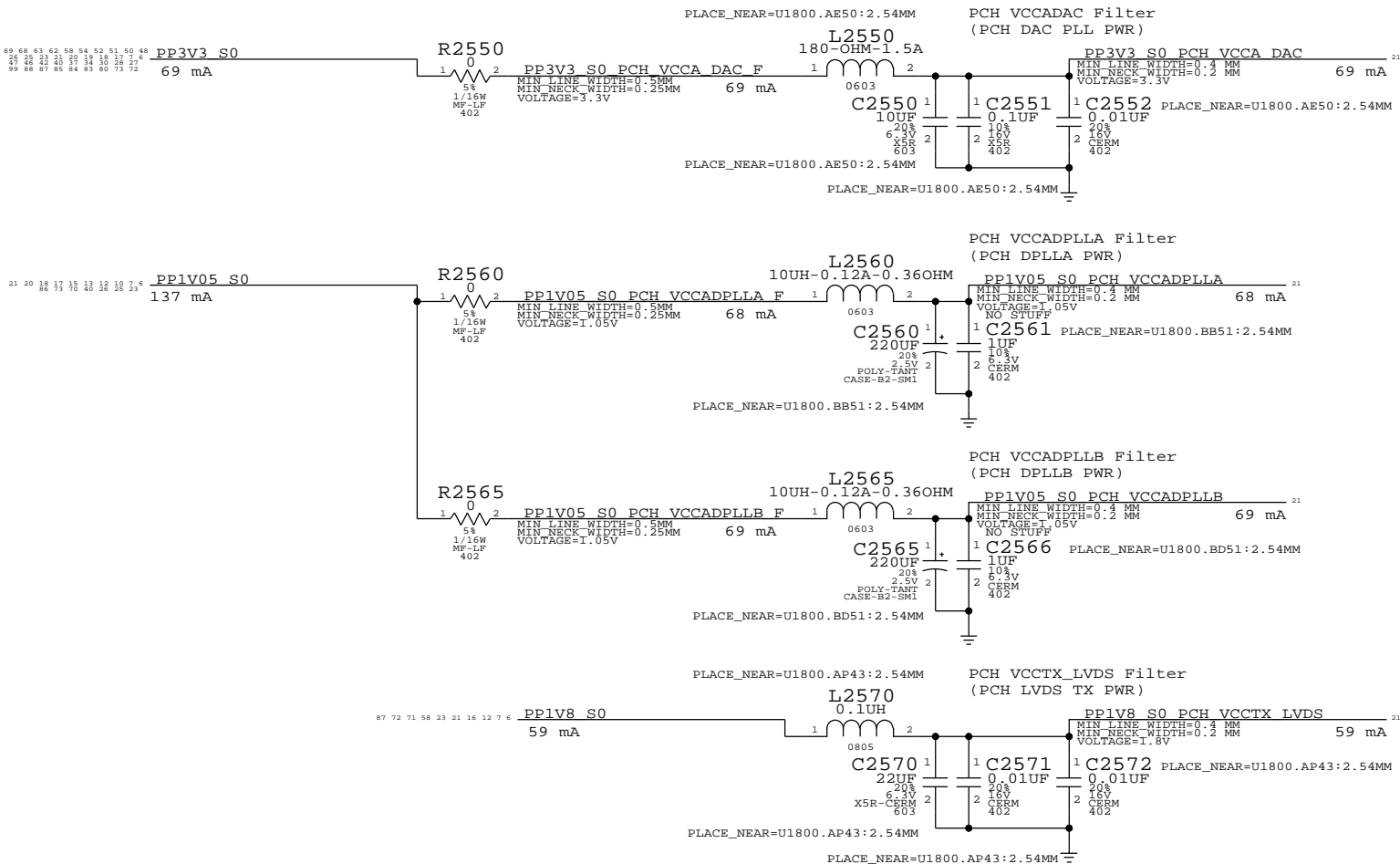
5x 1uF 0402

PLACEMENT\_NOTE (C2510-C2514):

Place on bottom side of U1000.




Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form F actor Schematic Check List Rev 1.1 (doc #395914) table 3.26.



Design recommendations from Calpella Design Guide Rev 1.5 (doc #398905) Section 3.25.3 tables 161 and 162.

Current numbers from Ibox Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

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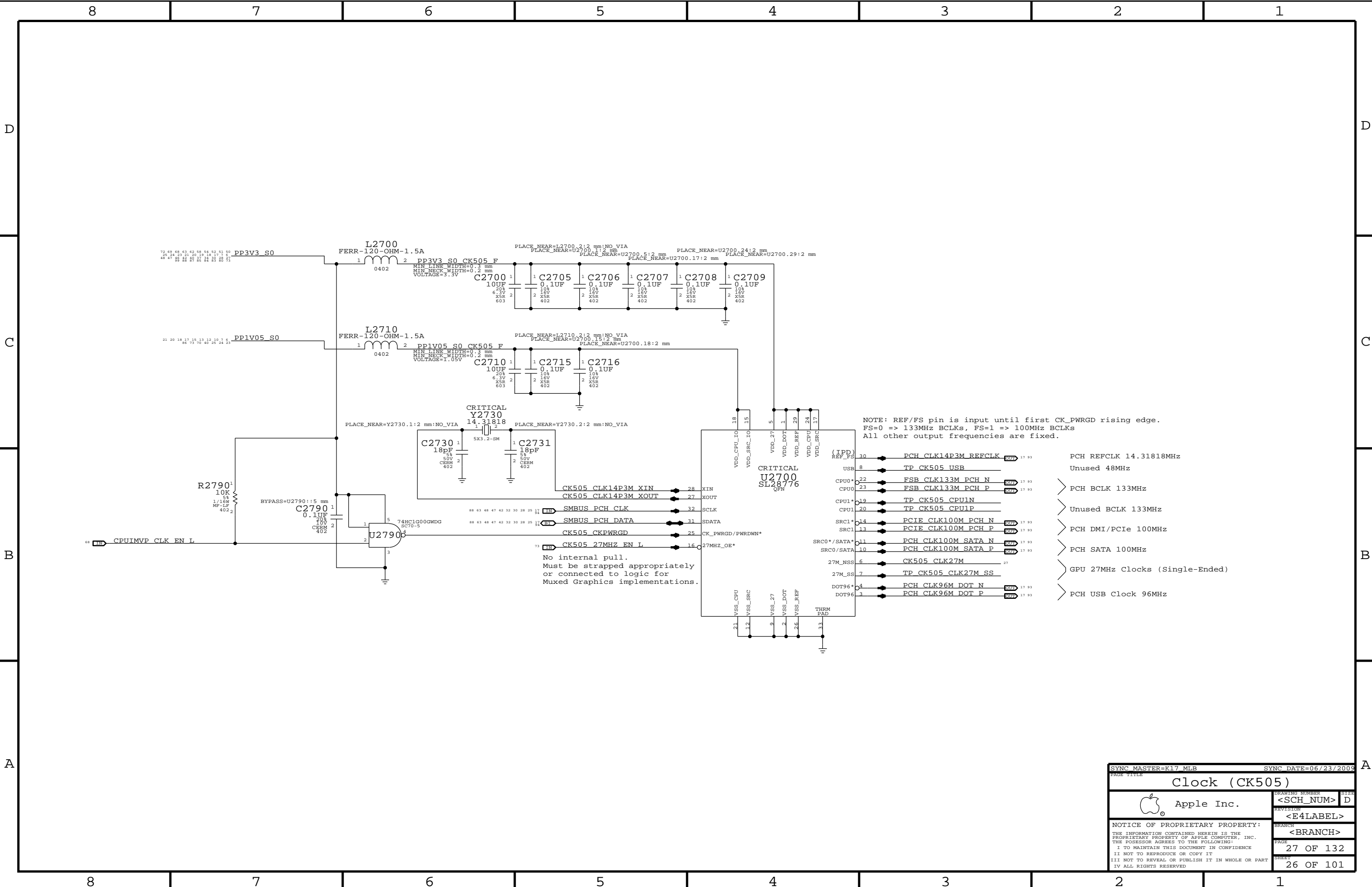
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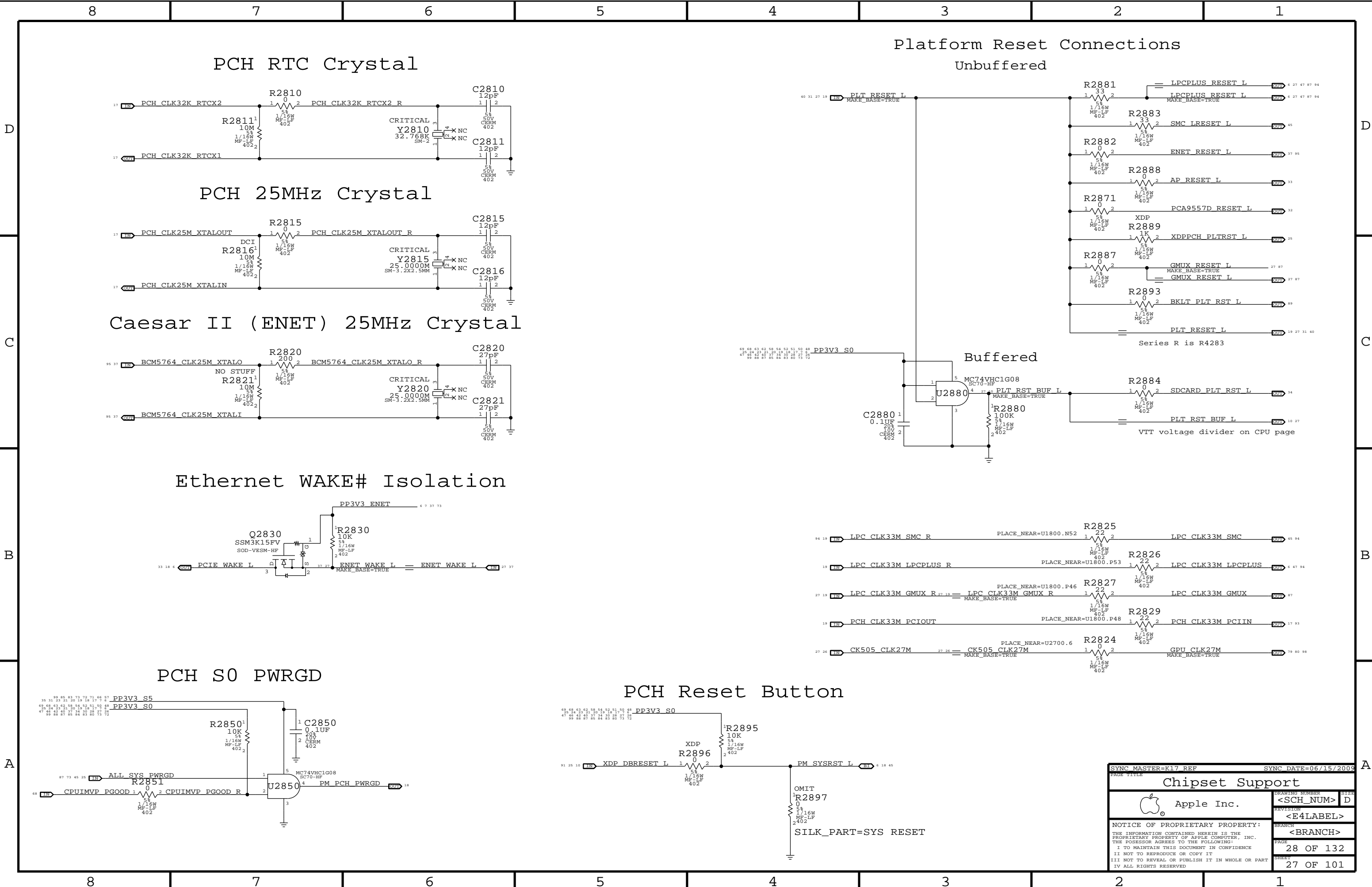
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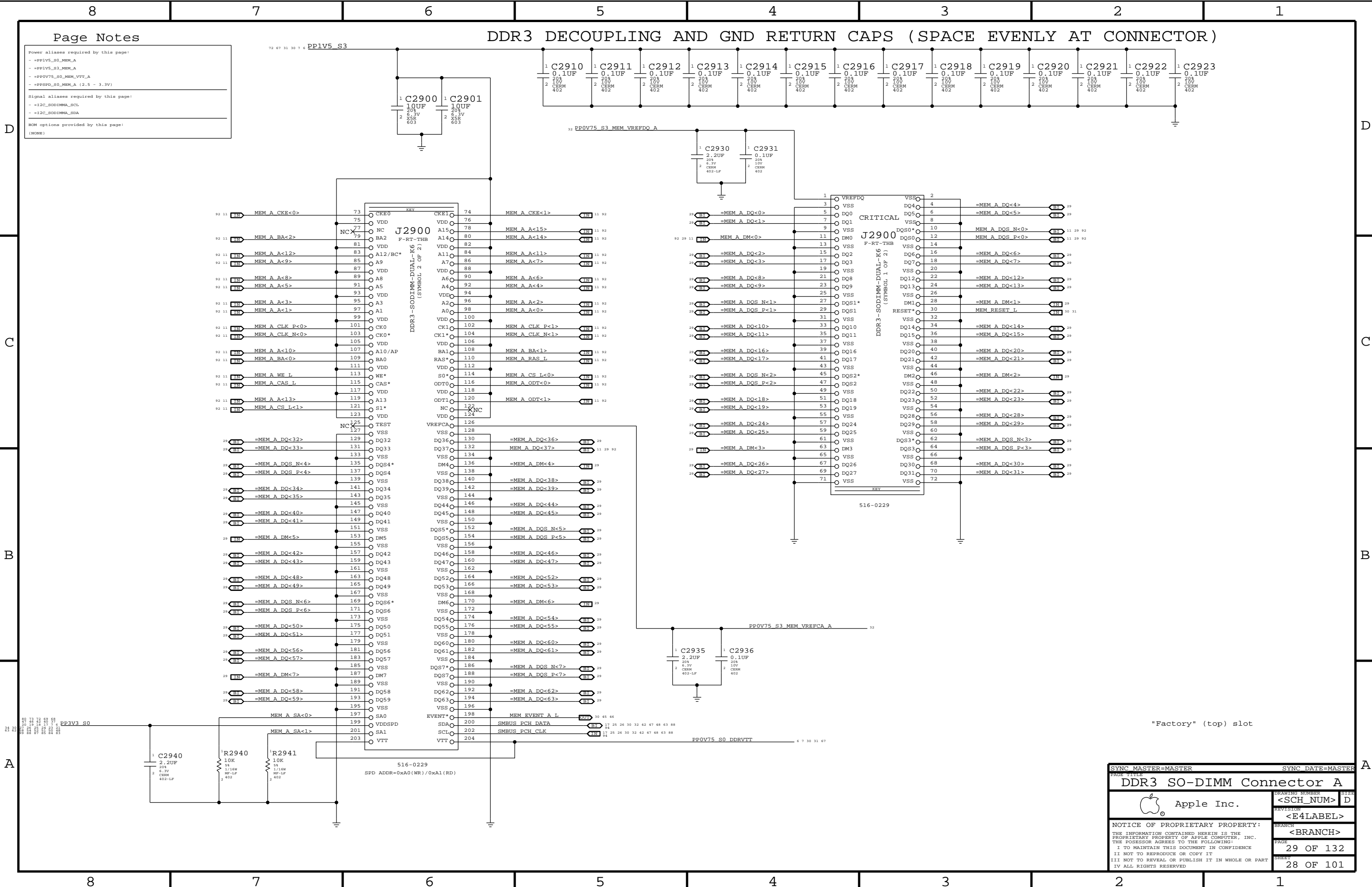
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Page Notes

Power aliases required by this page:

- =PP1V5\_S0\_MEM\_A
- =PP1V5\_S3\_MEM\_A
- =PP0V75\_S0\_MEM\_VTT\_A
- =PPSPD\_S0\_MEM\_A (2.5 - 3.3V)


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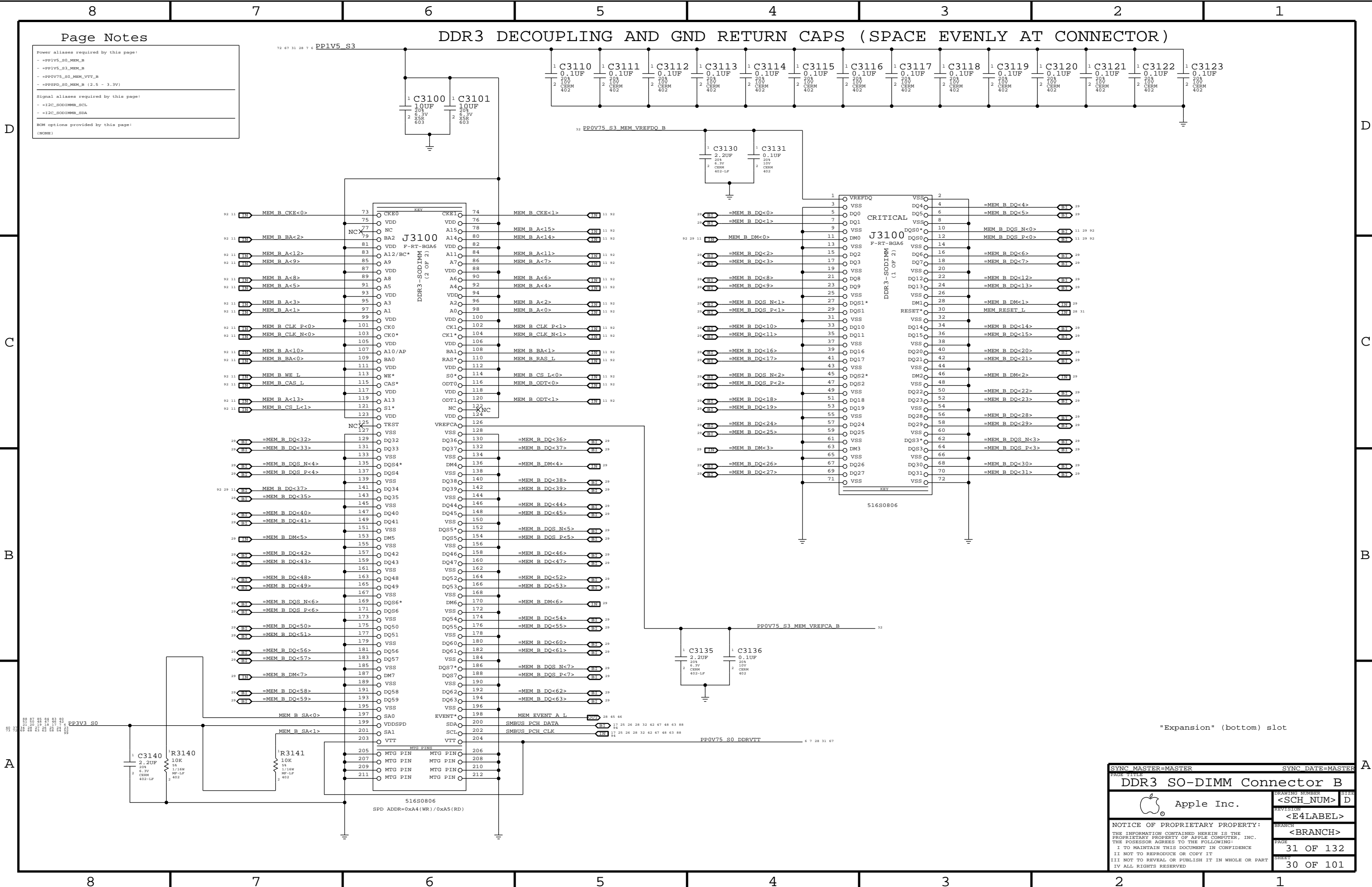
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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

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Page Notes

Power aliases required by this page:

- =PP1V5\_S0\_MEM\_B
- =PP1V5\_S3\_MEM\_B
- =PP0V75\_S0\_MEM\_VTT\_B
- =PPSPD\_S0\_MEM\_B (2.5 - 3.3V)

Signal aliases required by this page:

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BOM options provided by this page:


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DDR3 SO-DIMM Connector B

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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM\_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE\_CPU\_MEM\_L GPIO state during S3->S0 transitions determines behavior of signals.  
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM\_RESET\_L not isolated.  
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM\_RESET\_L isolated.

P1V5CPU\_EN = (ISOLATE\_CPU\_MEM\_L + PM\_SLP\_S3\_L) \* PM\_SLP\_S4\_L  
MEMVTT\_EN = (ISOLATE\_CPU\_MEM\_L + PLT\_RST\_L) \* PM\_SLP\_S3\_L  
MEM\_RESET\_L = !ISOLATE\_CPU\_MEM\_L + CPU\_MEM\_RESET\_L

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C

C

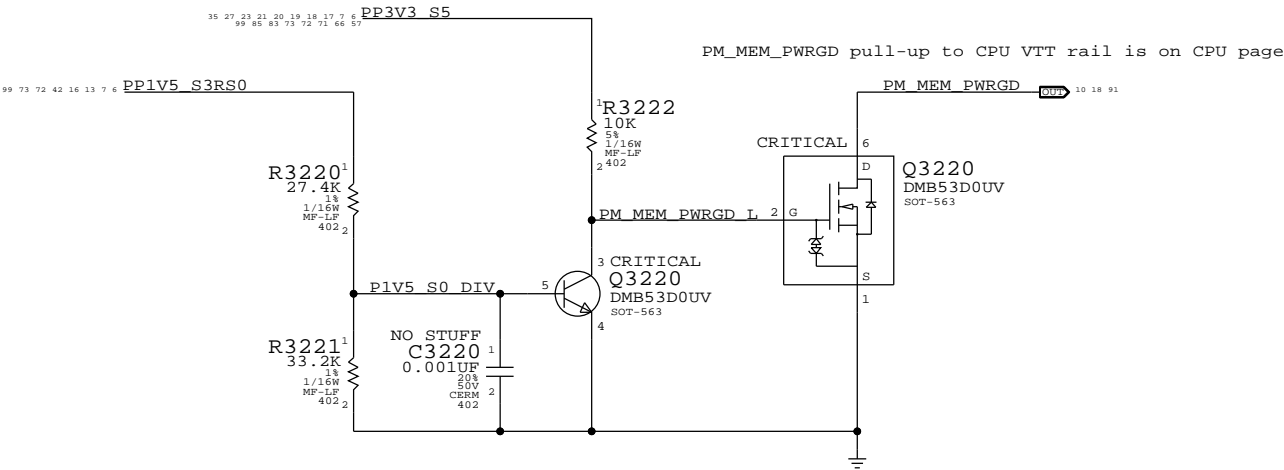
B

B

A

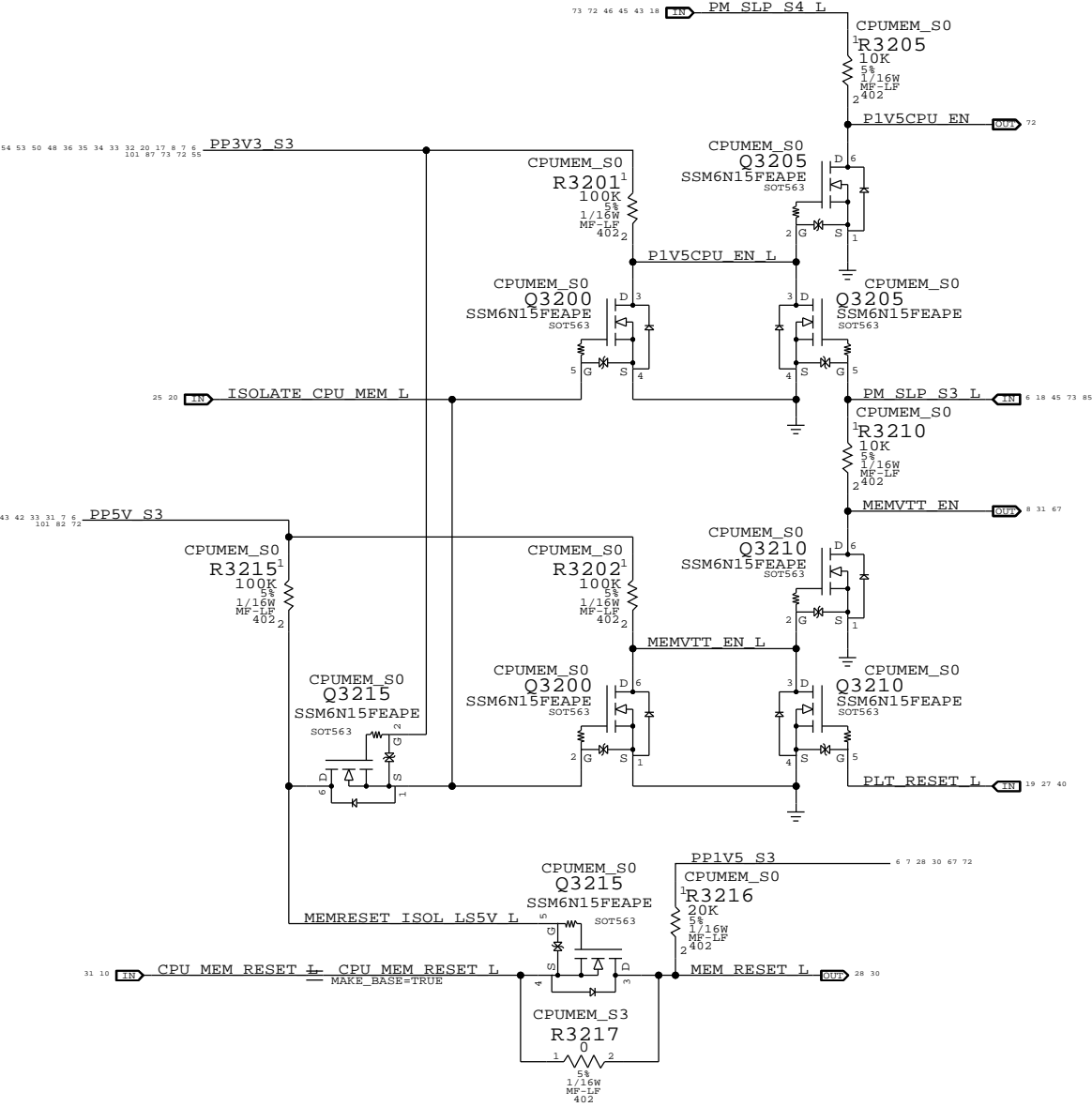
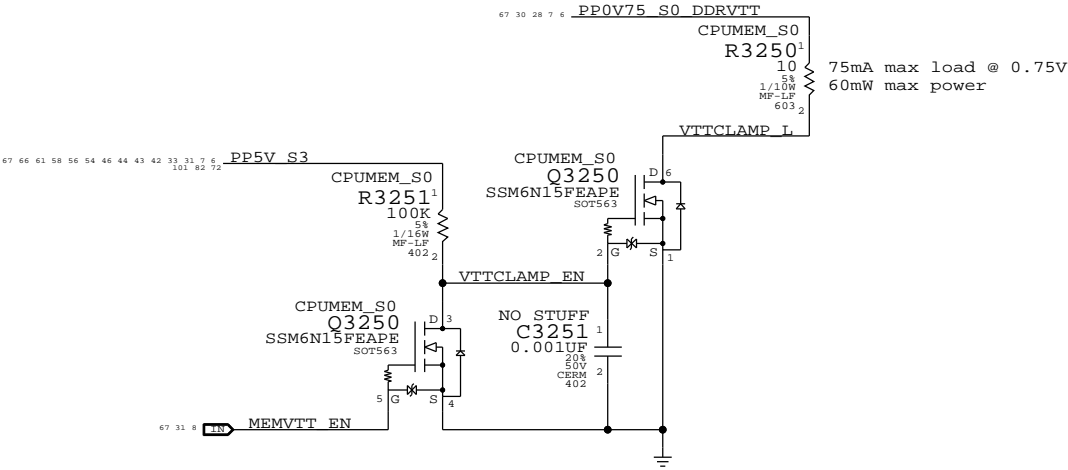
A

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp


Ensures CKE signals are held low in S3

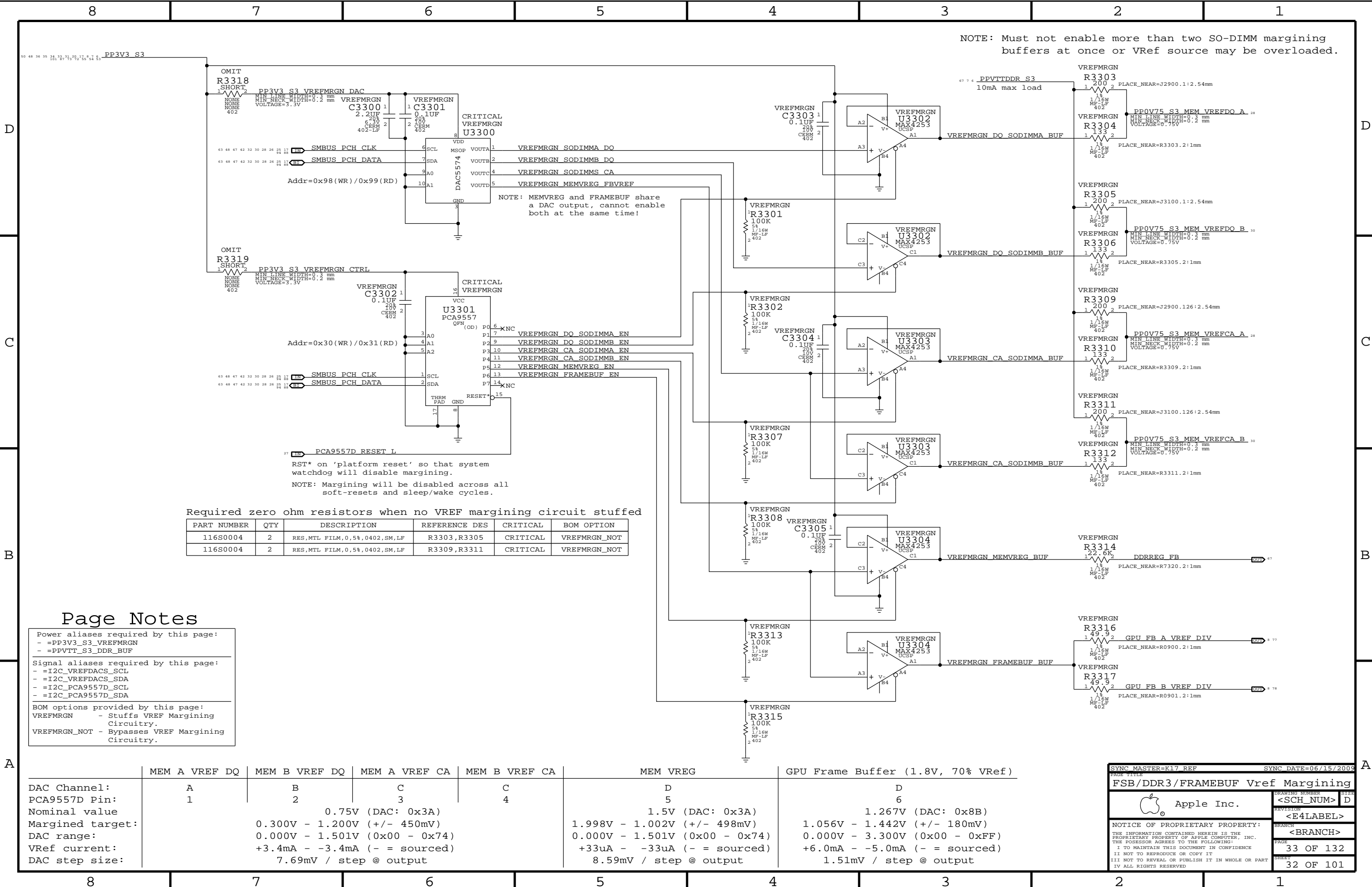


Step	ISOLATE_CPU_MEM_L	PLT_RST_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
to	1	1	1	1	1	CPU_MEM_RESET_L	1	1
S0	7							

(\*) CPU\_MEM\_RESET\_L asserts due to loss of PM\_MEM\_PWRGD, must wait for software to clear before deasserting ISOLATE\_CPU\_MEM\_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE\_CPU\_MEM\_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM\_RESET\_L will not properly assert. Software must deassert ISOLATE\_CPU\_MEM\_L and then generate a valid reset cycle on CPU\_MEM\_RESET\_L.

SYNC MASTER=K17_REF		SYNC DATE=06/15/2009	
PAGE TITLE			
CPU Memory S3 Support			
		DRAWING NUMBER	
Apple Inc.		<SCH_NUM>	
		REVISION	
		<E4LABEL>	
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		<BRANCH>	
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Page Notes

Power aliases required by this page:  
- =PP3V3\_S3\_VREFMRGN  
- =PPVTT\_S3\_DDR\_BUF

Signal aliases required by this page:  
- =I2C\_VREFDACS\_SCL  
- =I2C\_VREFDACS\_SDA  
- =I2C\_PCA9557D\_SCL  
- =I2C\_PCA9557D\_SDA

BOM options provided by this page:  
VREFMRGN - Stuffs VREF Margining Circuitry.  
VREFMRGN\_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value			0.75V (DAC: 0x3A)		1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:			0.300V - 1.200V (+/- 450mV)		1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:			0.000V - 1.501V (0x00 - 0x74)		0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
Vref current:			+3.4mA - -3.4mA (- = sourced)		+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:			7.69mV / step @ output		8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=K17 REF

SYNC DATE=06/15/2009

FSB/DDR3/FRAMBUF Vref Margining

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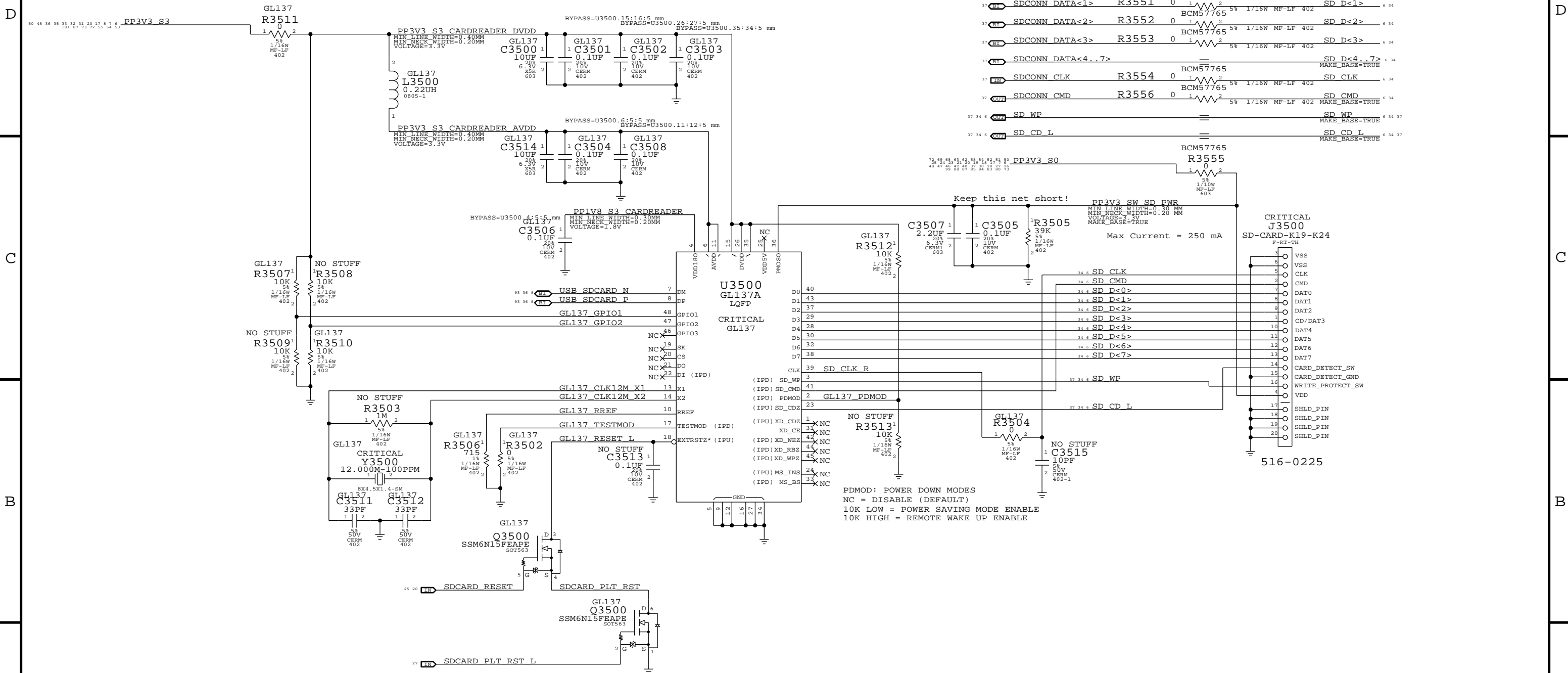
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Caesar IV Support



SYNC MASTER=T27 REF		SYNC DATE=08/26/2009	
PAGE TITLE			
SecureDigital Card Reader			
 Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	35 OF 132
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This figure shows a detailed schematic diagram of a USB HUB-1 circuit, designed by Apple Inc. The schematic includes various components such as resistors (R3604, R3697, R3698, etc.), capacitors (C3618, C3636, C3637, etc.), integrated circuits (U3600, U3614), and transistors (Q3640). It also features a Bill of Materials (BOM) table and a configuration table.

The BOM TABLE lists the following items:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U3600,U3700	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U3600,U3700	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U3600,U3700	CRITICAL	USBHUB_2061

The configuration table provides settings for SEL1, SEL0, and NON\_REM1/NON\_REM0:

SEL1	SEL0	DESCRIPTION
0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

The schematic also includes a section for HUB1\_NONREM1\_0, HUB1\_NONREM1\_1, and HUB1\_NONREM0\_0, detailing their descriptions and configurations.

Apple Inc. logo and copyright notice are present at the bottom right of the page.

[illegible][illegible][illegible][illegible]

**USB HUB-1**

This schematic diagram illustrates the internal circuitry of a USB Hub, featuring various components such as resistors (R), capacitors (C), inductors (L), and integrated circuits (U). The design includes multiple power planes (PP3V3 S3, PP3V3 S5) and ground connections. Key functional blocks include:

- Power Regulation:** Includes a voltage divider (R3640, R3641) and a reset circuit (Q3640, Q3641).
- Control Logic:** Features a microcontroller (U3600) interfaced with an EEPROM (U3614) via I2C/SMBus.
- Signal Processing:** Includes a crystal oscillator (Y3600) and various signal conditioning components.
- Connectivity:** Shows connections for USB cameras, IR receivers, and external devices (A, B, C).
- Thermal Management:** A thermal pad (THRML\_PAD) is connected to the microcontroller for temperature monitoring.

The diagram also includes a Bill of Materials (BOM) table and configuration options.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U3600,U3700	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U3600,U3700	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U3600,U3700	CRITICAL	USBHUB_2061

SEL1		SEL0		DESCRIPTION
K17/K18 configuration:	0	0	0	Internal Default with Self powered Operation
	0	1	0	SMBUS Slave Config
	1	0	0	Internal Default with Bus powered Operation
	1	1	1	EEPROM Supported

**BOM TABLE**

BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREMI_0,HUB1_NONREMO_0
HUB1_1NONREM	HUB1_NONREMI_0,HUB1_NONREMO_1
HUB1_2NONREM	HUB1_NONREMI_1,HUB1_NONREMO_0
HUB1_3NONREM	HUB1_NONREMI_1,HUB1_NONREMO_1

**Configuration Options:**

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

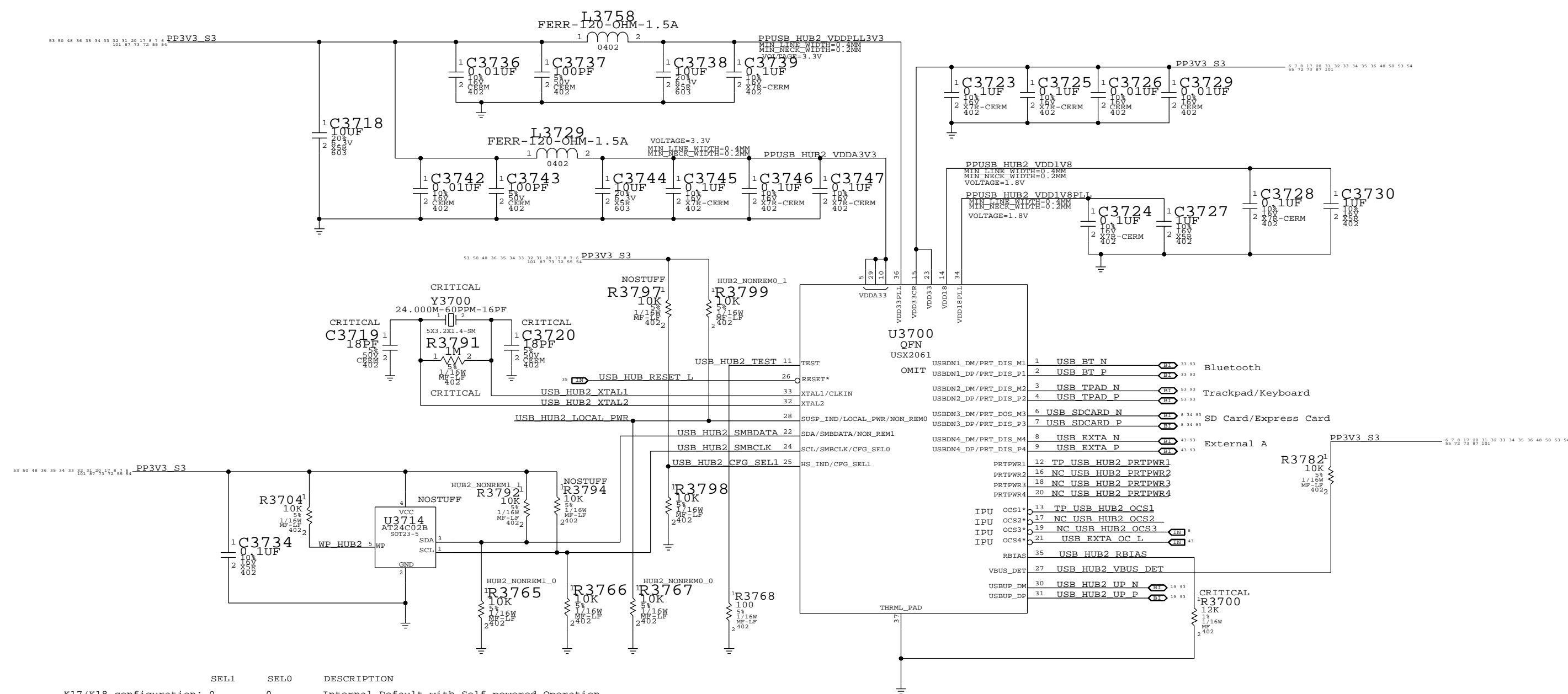
**Legend:**

- A: All ports are removable
- B: Port 1 is non removable
- C: Port 1 and 2 are non removable
- D: Port 1, 2, and 3 are non removable

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USB HUB-2



	SEL1	SEL0	DESCRIPTION
K17/K18 configuration:	0	0	Internal Default with Self powered Operation
	0	1	SMBUS Slave Config
	1	0	Internal Default with Bus powered Operation
	1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM GROUP	BOM OPTIONS
HUB2_ALLREM	HUB2_NONREM1_0, HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0, HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1, HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1, HUB2_NONREM0_1

SYNC MASTER=K23F

SYNC DATE=10/06/2009

USB HUB 2

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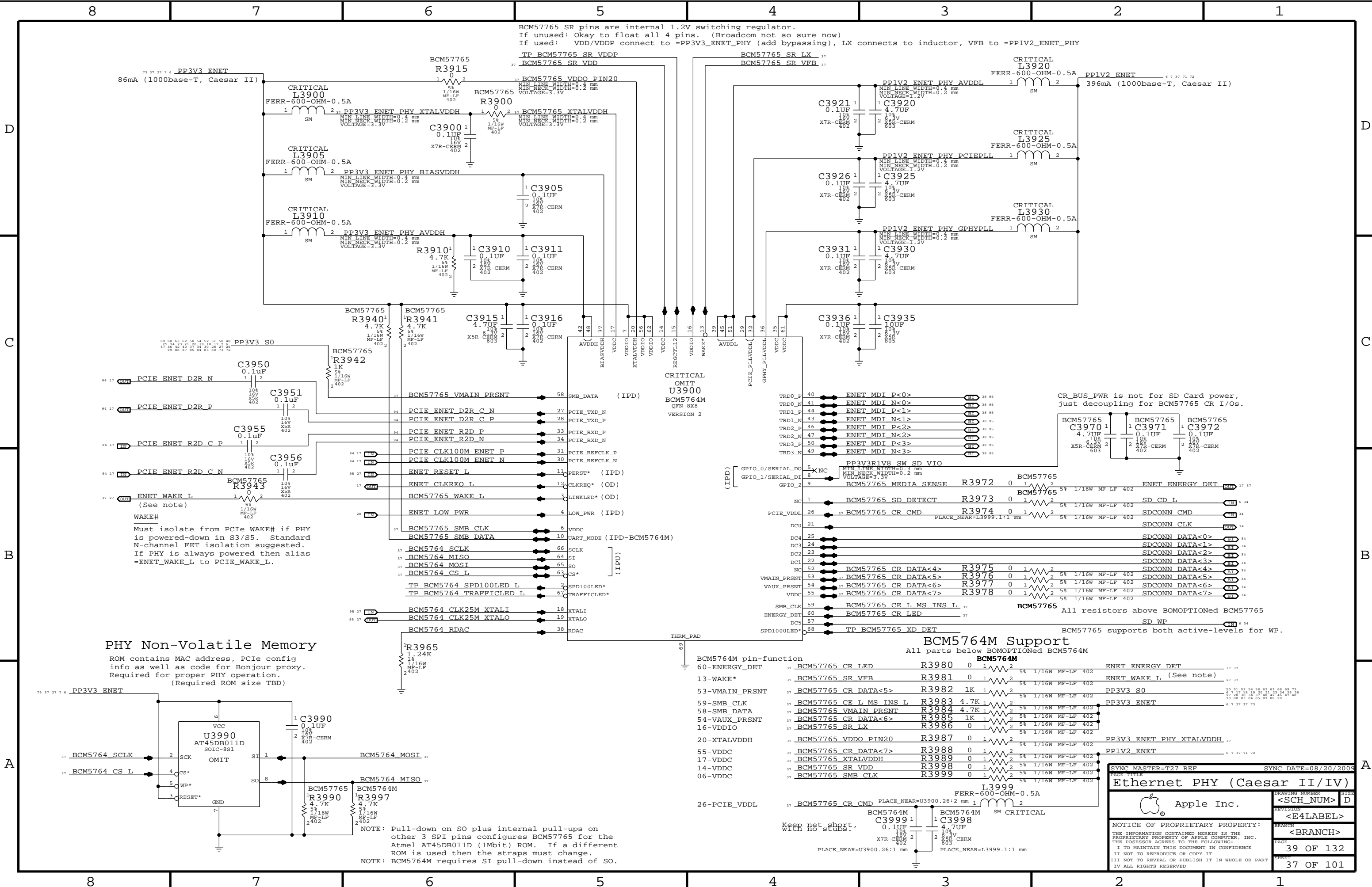
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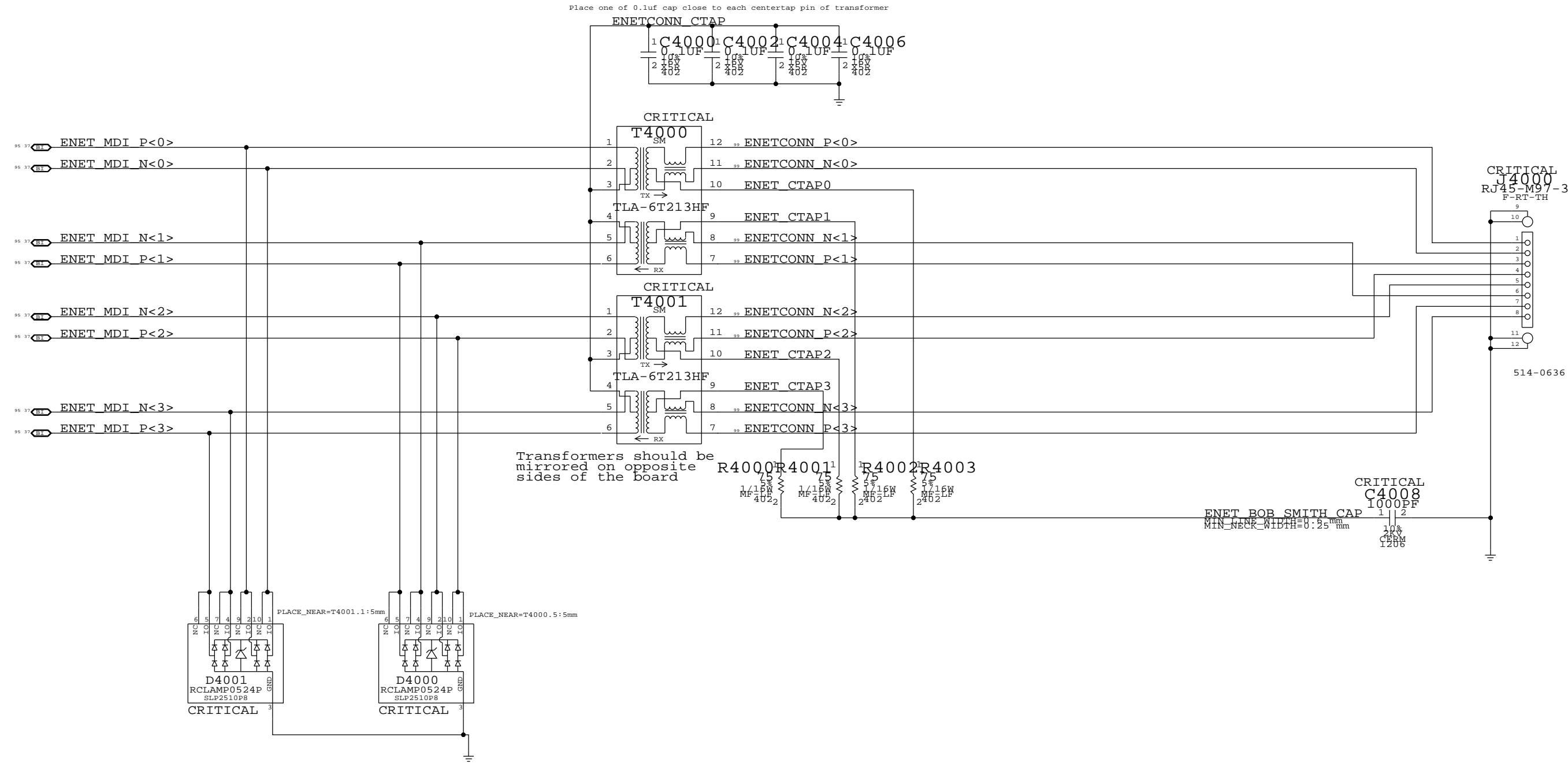



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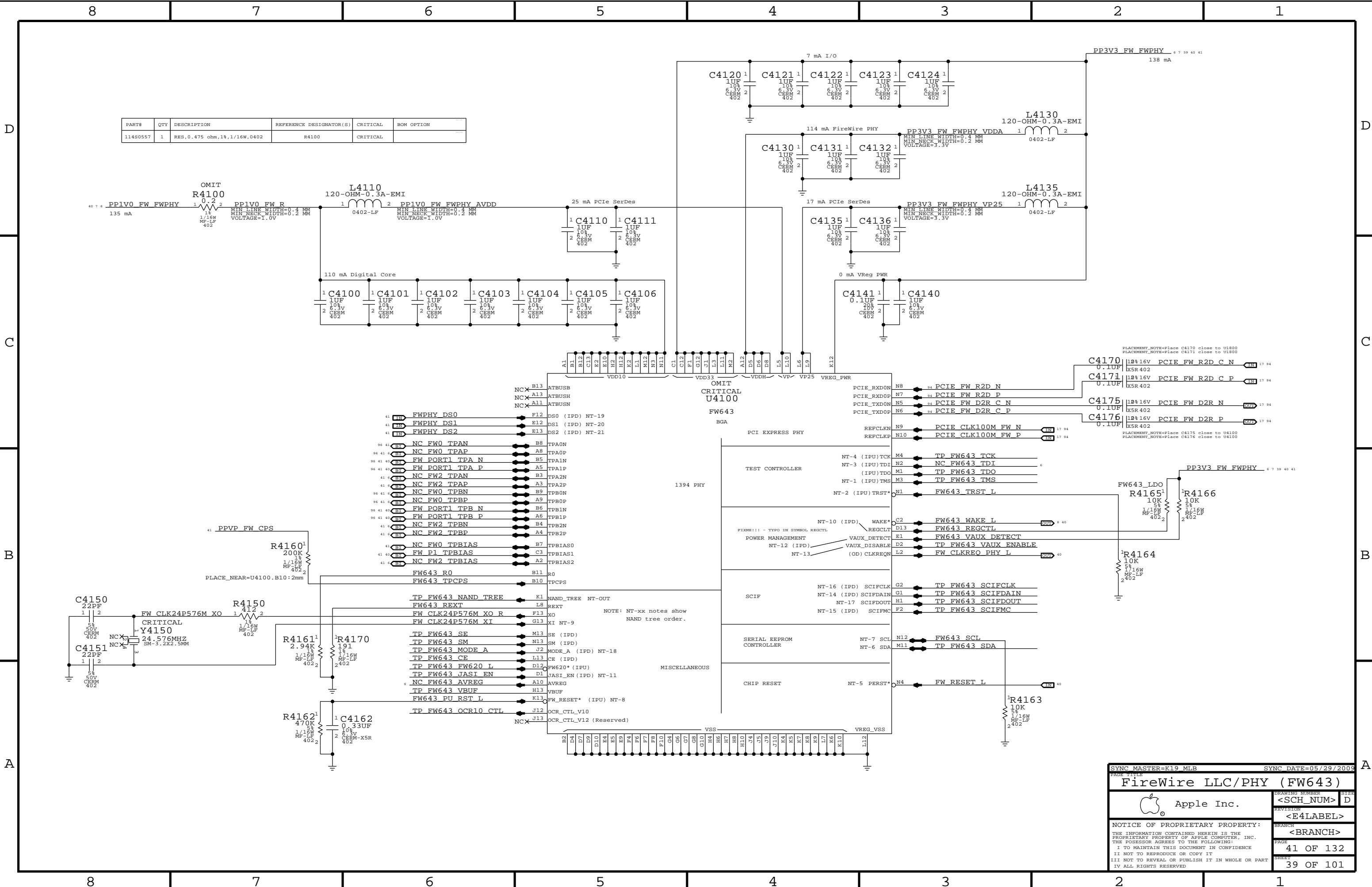
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(NONE)

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
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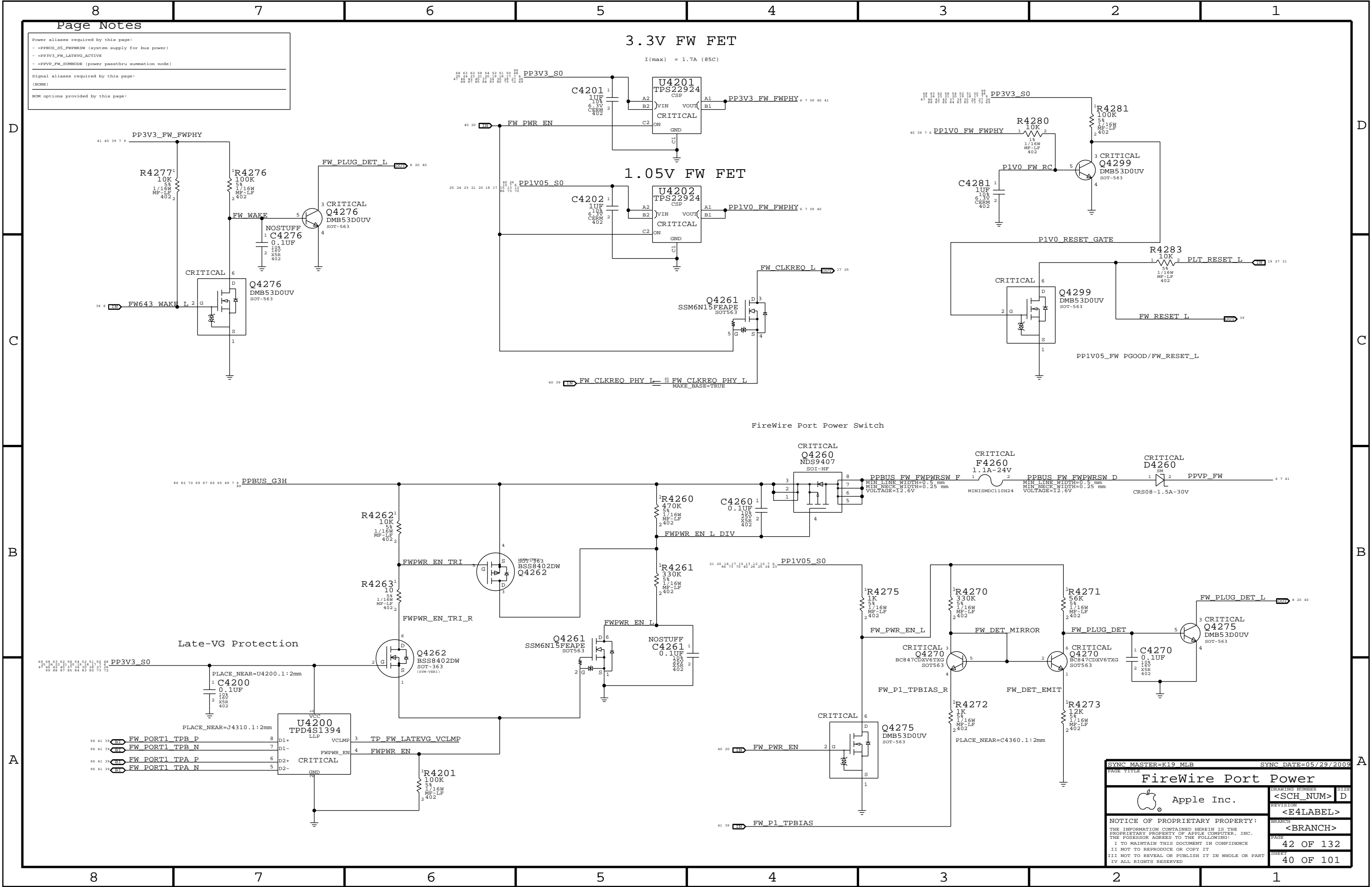
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Ethernet Connector			
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11480557	1	RES,0.475 ohm,1%,1/16W,0402	R4100	CRITICAL	

- FWPHY\_DS0
- FWPHY\_DS1
- FWPHY\_DS2
- NC FW0 TPAN
- NC FW0 TPAP
- FW PORT1 TPA N
- FW PORT1 TPA P
- NC FW2 TPAN
- NC FW2 TPAP
- NC FW0 TPBN
- NC FW0 TPBP
- FW PORT1 TPB N
- FW PORT1 TPB P
- NC FW2 TPBN
- NC FW2 TPBP
- NC FW0 TPBIAS
- FW P1 TPBIAS
- NC FW2 TPBIAS
- FW643\_R0
- FW643\_TPCPS
- TP FW643 NAND TREE
- FW643\_REXT
- FW CLK24P576M XO R
- FW CLK24P576M XI
- TP FW643 SE
- TP FW643 SM
- TP FW643 MODE\_A
- TP FW643 CE
- TP FW643 FW620 L
- TP FW643 JASI\_EN
- NC FW643 AVREG
- TP FW643 VBUF
- FW643\_PU\_RST L
- TP FW643 OCR10 CTL

SYNC MASTER=K19 MLB		SYNC DATE=05/29/2009	
PAGE TITLE			
FireWire LLC/PHY		(FW643)	
		Apple Inc.	
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		PAGE	41 OF 132
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Page Notes

Power aliases required by this page:

- =PPVP\_FW\_PORT1
- =PP3V3\_FW\_LATEVG

Signal aliases required by this page:

(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:

(NONE)

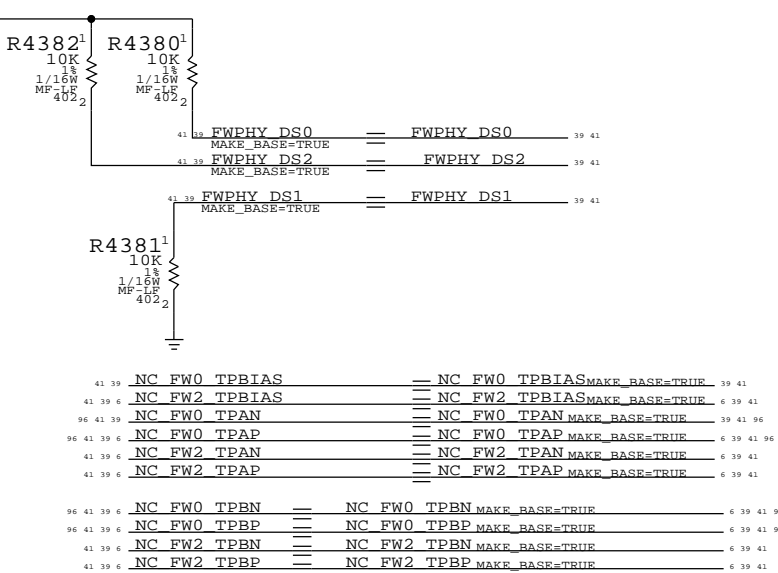
NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

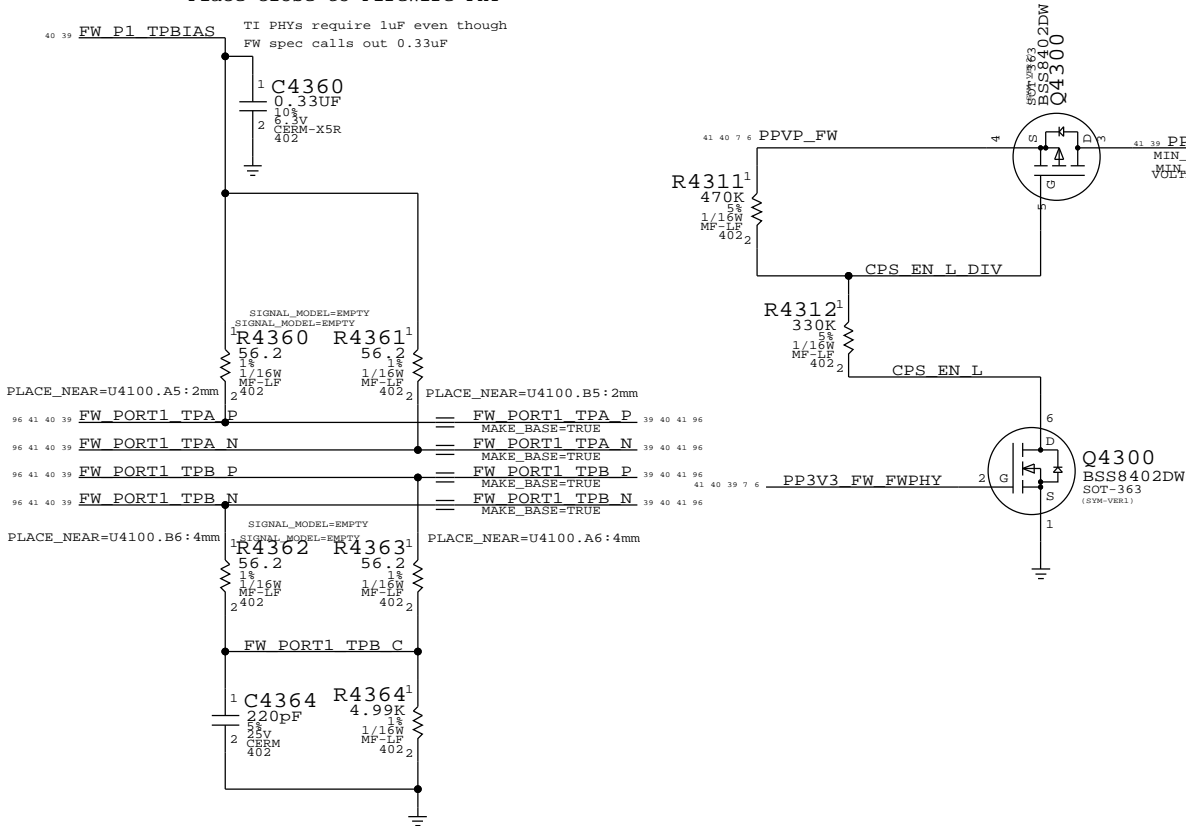
Configures PHY for:

- 1-port Portable Power Class (0)
- Port "1" Bilingual (1394B)

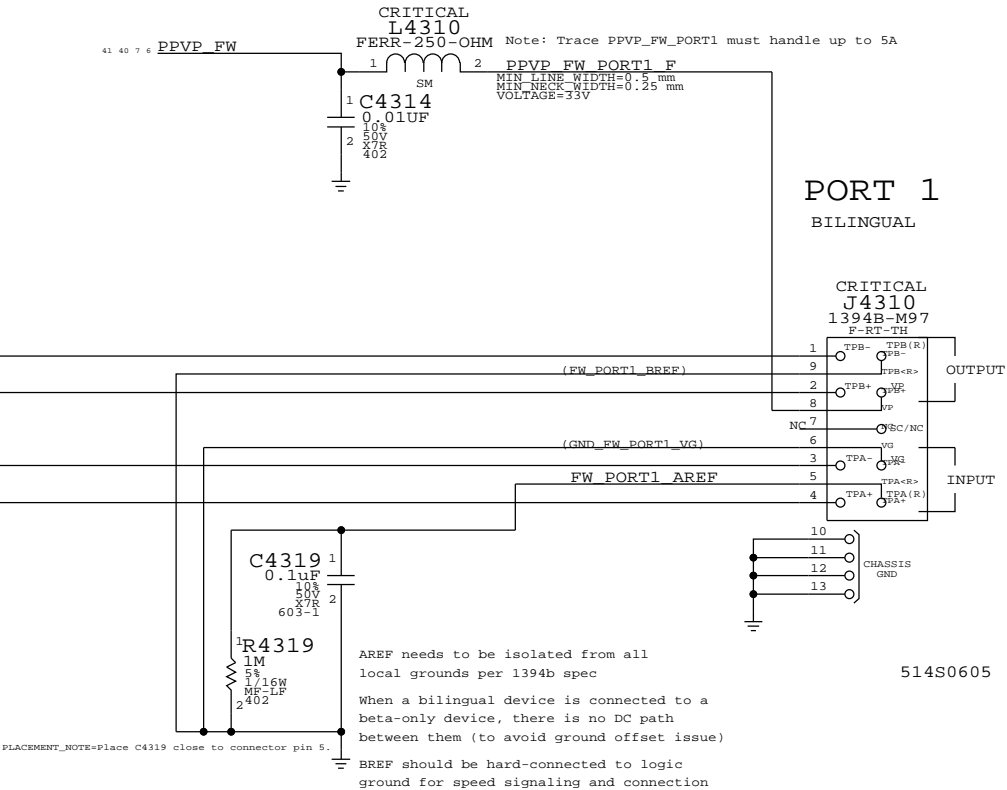


Termination

Place close to FireWire PHY

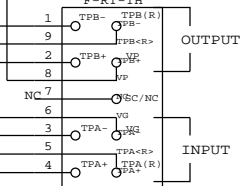


Cable Power




PORT 1  
BILINGUAL

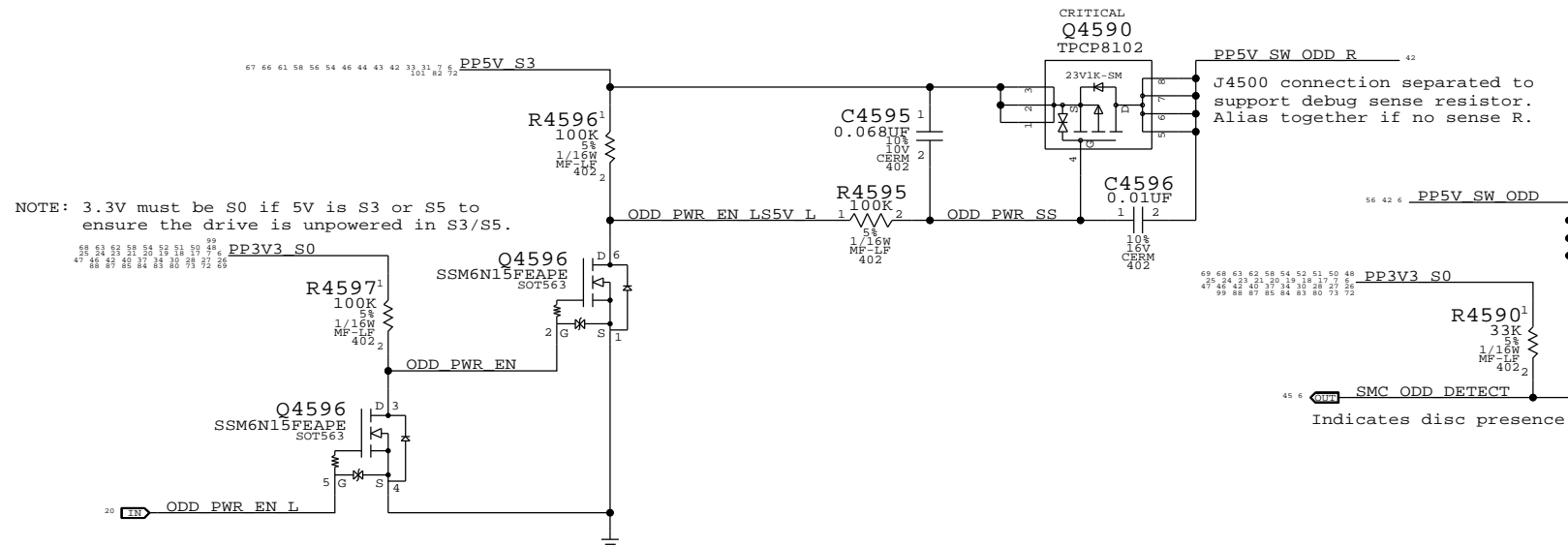
CRITICAL  
J4310  
1394B-M97  
F-RT-TH



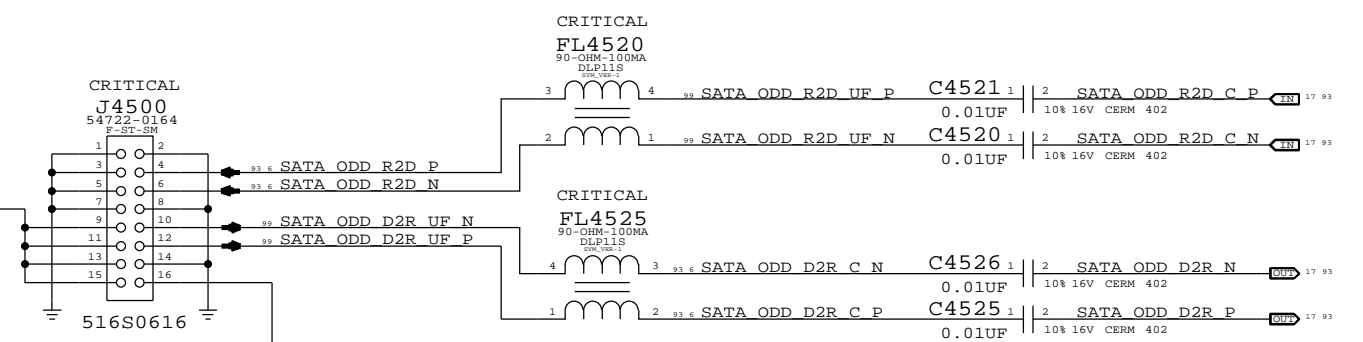
514S0605

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FireWire Ports			
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		PAGE	43 OF 132
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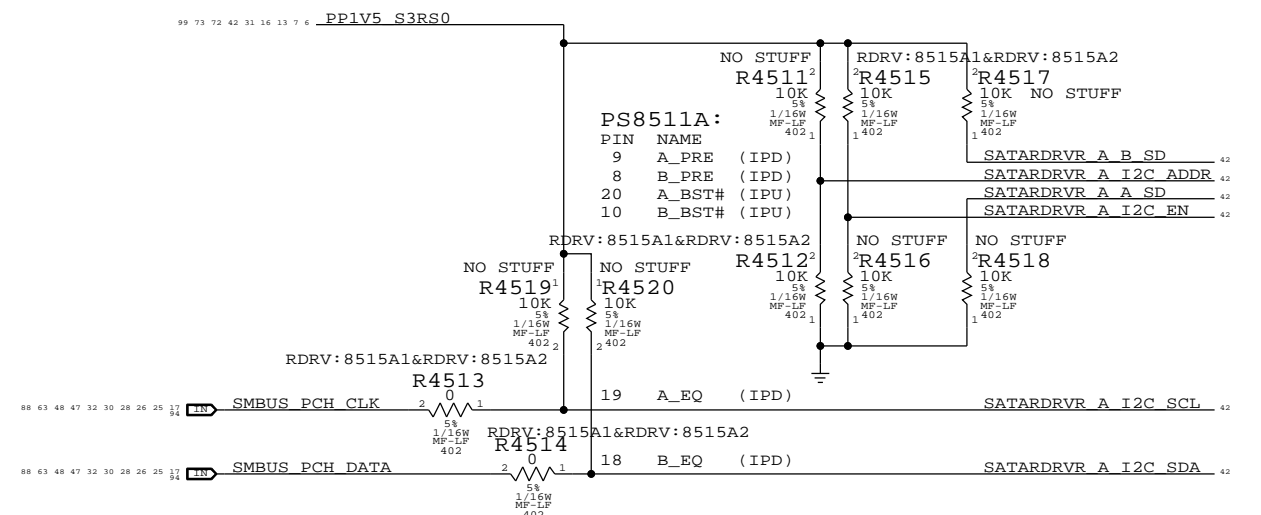
# ODD Power Control



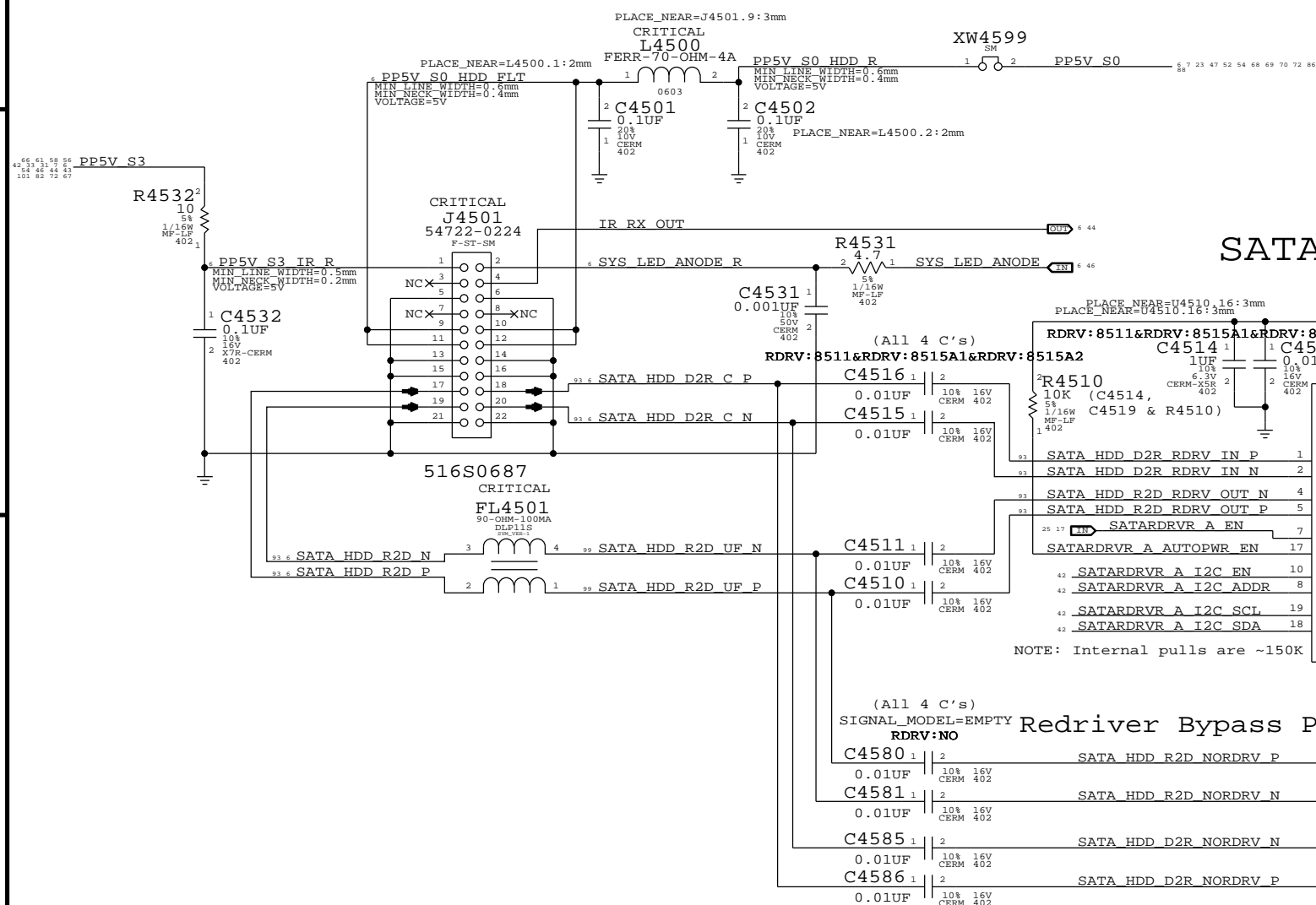
SATA ODD Connector



## PS8511A / PS8515A Straps



## SATA HDD/IR/SIL Connector

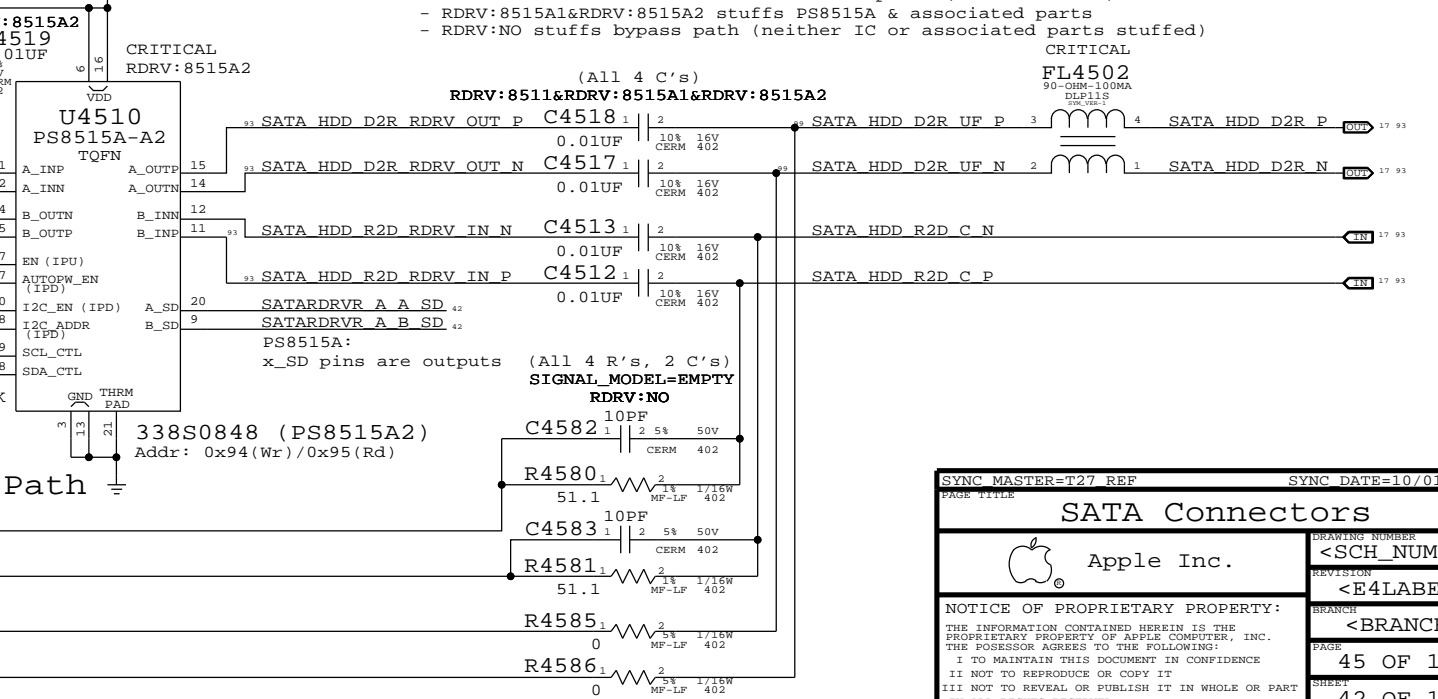



## SATA Redriver

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0769	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV:8511
338S0778	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV:8515A1

BOMOPTIONS:

- RDRV:8511 stuffs PS8511A & associated parts (STRAPS TBD!!!)
- RDRV:8515A1&RDRV:8515A2 stuffs PS8515A & associated parts
- RDRV:NO stuffs bypass path (neither IC or associated parts stuffed)




SYNCH MASTER=T27 REF		SYNCH DATE=10/01/2009	
PAGE TITLE			
SATA Connectors			
 Apple Inc.		DRAWING NUMBER	SIZE
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Port Power Switch

Left USB Port A

USB/SMC Debug Mux

Left USB Port B

SYNC MASTER=K17 REF		SYNC DATE=06/15/2009	
PAGE TITLE			
External USB Connectors			
 Apple Inc.		DRAWING NUMBER	SIZE
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		<BRANCH>	
		PAGE	46 OF 132
		SHEET	43 OF 101

8 7 6 5 4 3 2 1

D

C

B

A

8 7 6 5 4 3 2 1

IR SUPPORT

PP5V\_S3

C4801 0.1UF

U4800 CY7C63803-LQXC

USB\_IR\_P

USB\_IR\_N

IR VREF FILTER

C4803 1UF

IR RX OUT RC

R4800 100

C4804 0.001UF

IR RX OUT

CRITICAL OMIT

THRM1 PAD

VSS

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Front Flex Support

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SYNC MASTER=K19\_MLB SYNC DATE=05/29/2009

PAGE TITLE

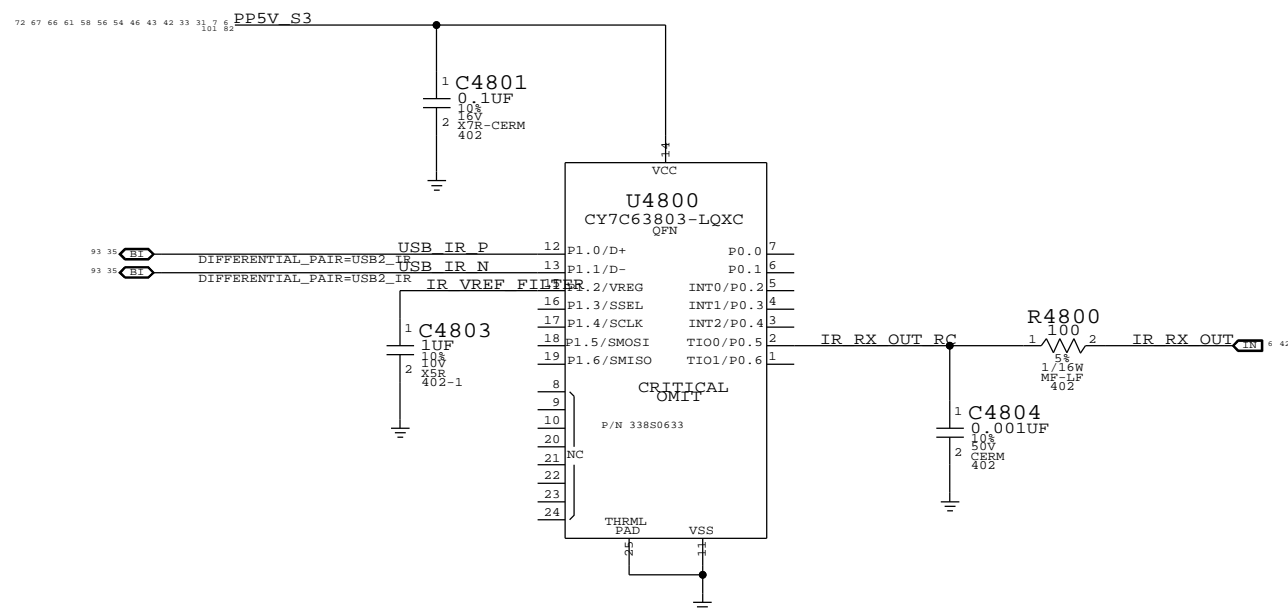
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
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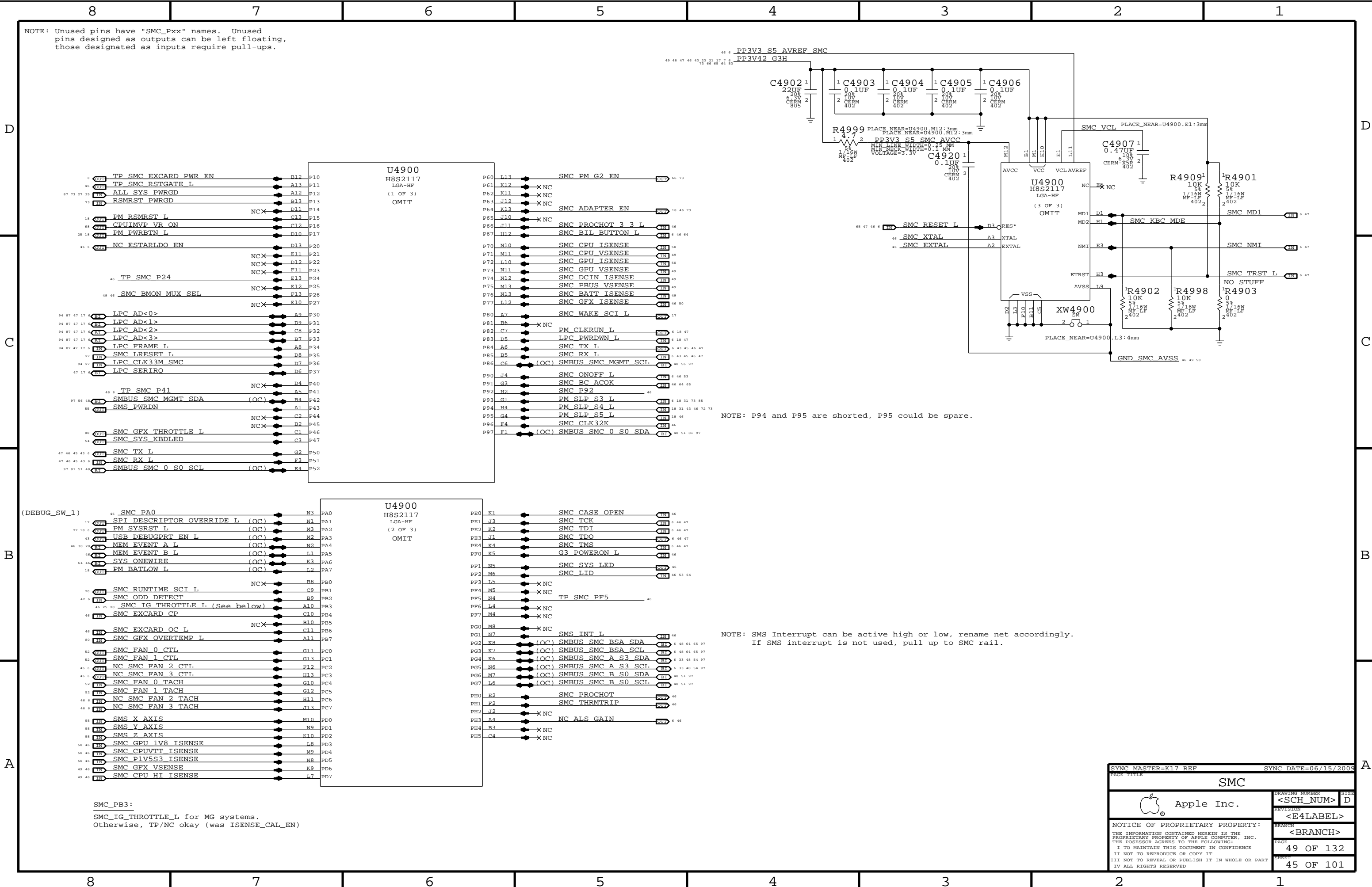
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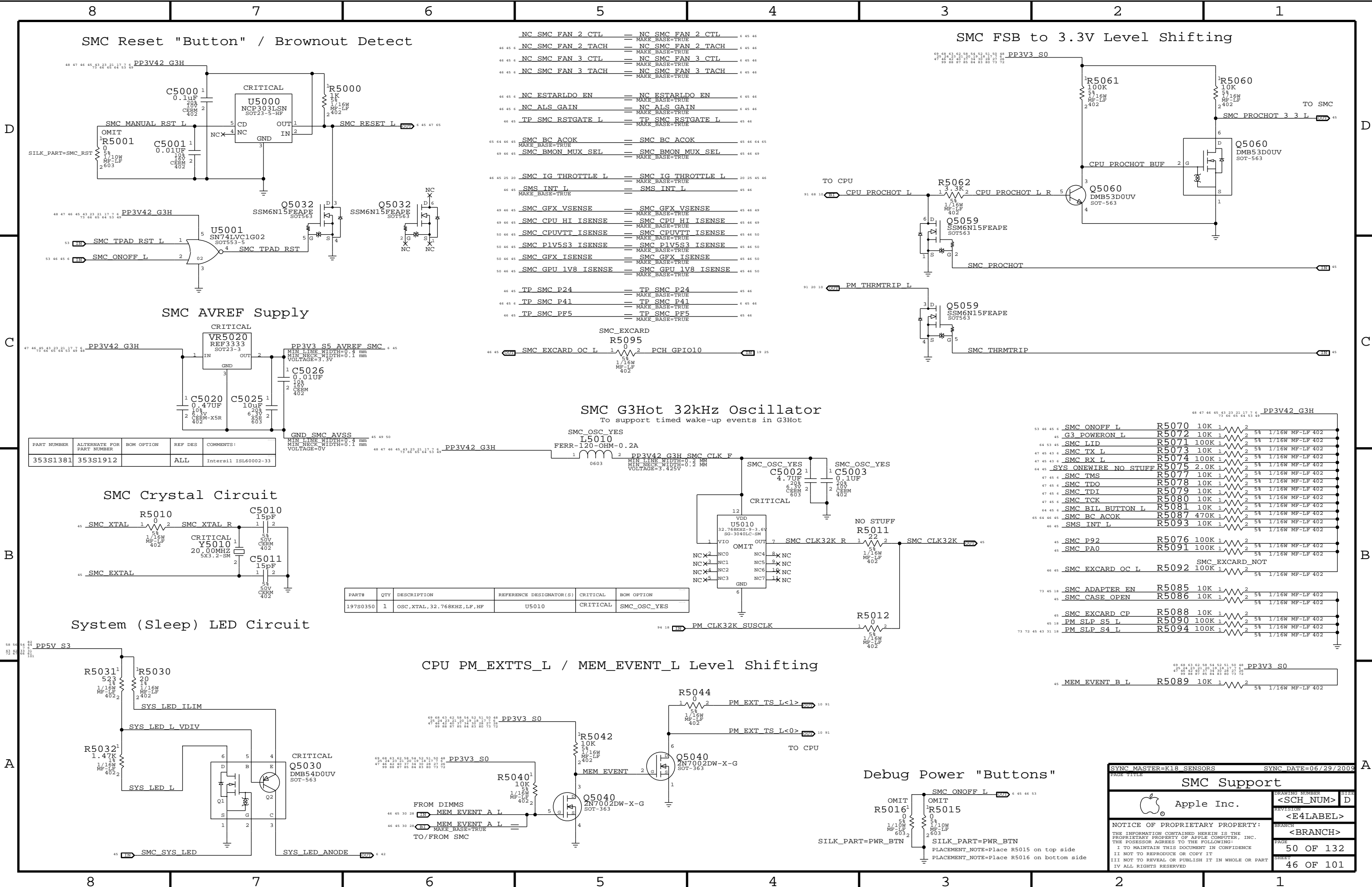
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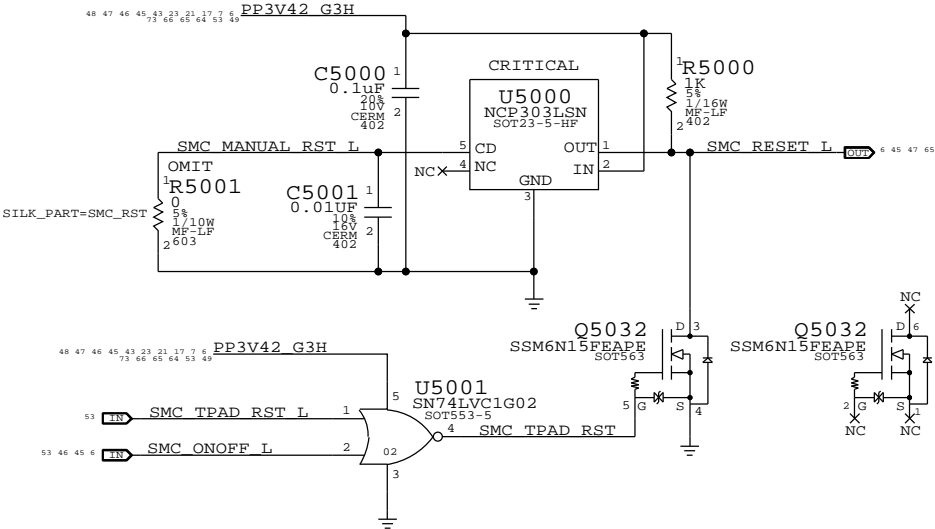
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			48		OF 132
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			44		OF 101



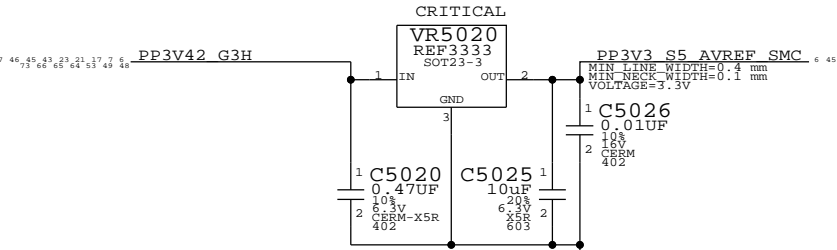




SMC Reset "Button" / Brownout Detect

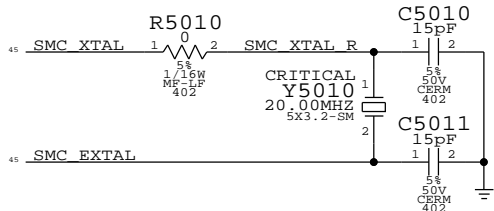


SMC AVREF Supply

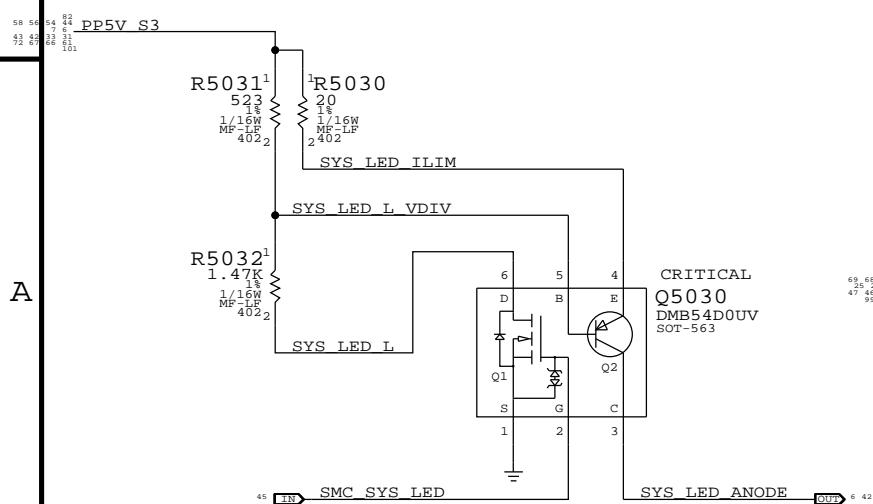


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Interall ISL60002-33

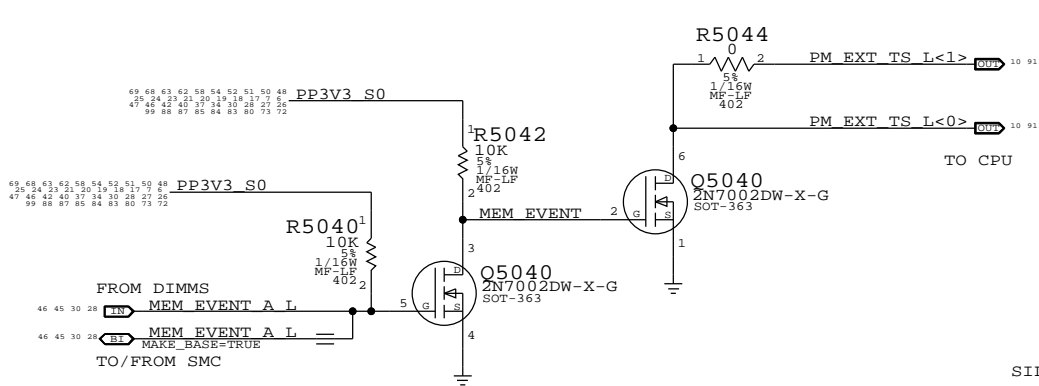
SMC Crystal Circuit



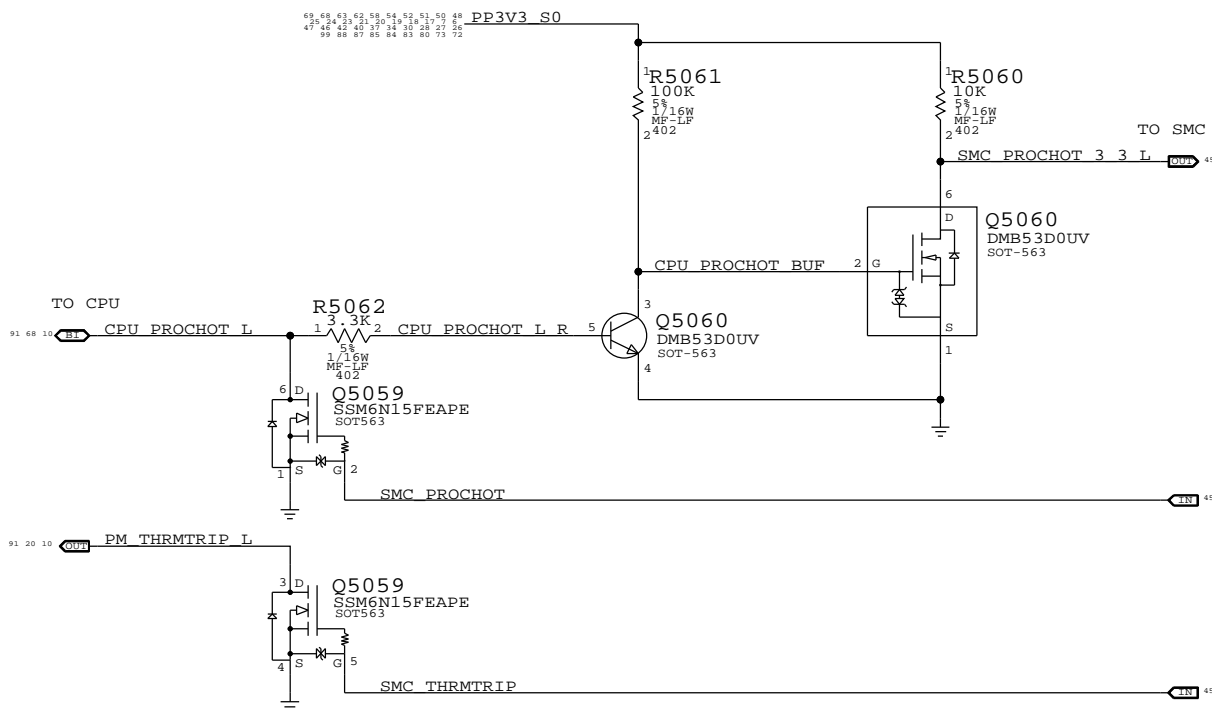
System (Sleep) LED Circuit



CPU PM\_EXTTS\_L / MEM\_EVENT\_L Level Shifting

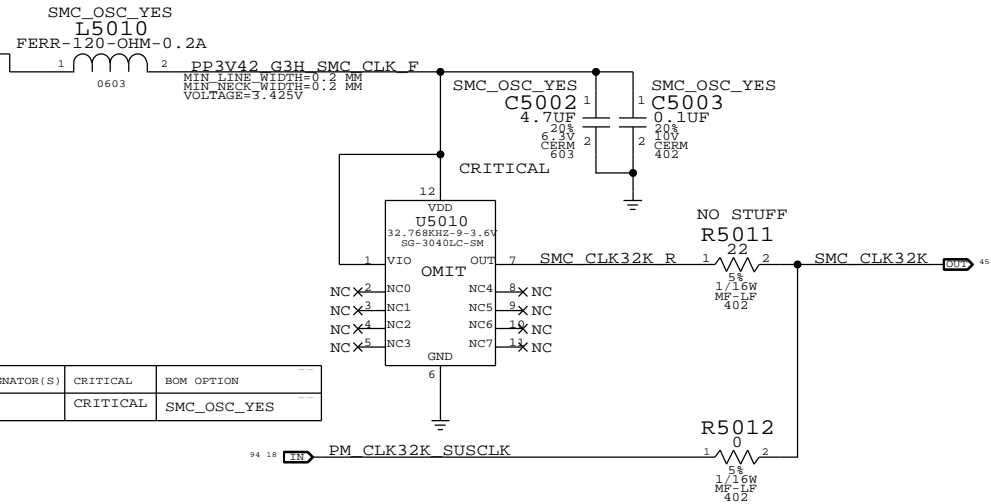


SMC FSB to 3.3V Level Shifting



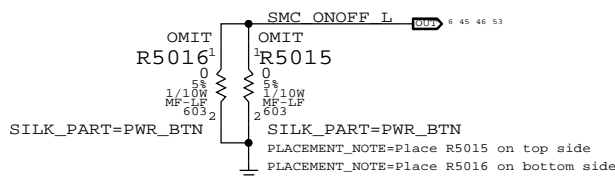
SMC G3Hot 32kHz Oscillator

To support timed wake-up events in G3Hot



SMC ONOFF L	R5070	10K	1	2	5%	1/16W MF-LF 402
G3 POWERON L	R5072	10K	1	2	5%	1/16W MF-LF 402
SMC LID	R5071	100K	1	2	5%	1/16W MF-LF 402
SMC TX L	R5073	10K	1	2	5%	1/16W MF-LF 402
SMC RX L	R5074	100K	1	2	5%	1/16W MF-LF 402
SYS ONEWIRE NO STUFF	R5075	2.0K	1	2	5%	1/16W MF-LF 402
SMC TMS	R5077	10K	1	2	5%	1/16W MF-LF 402
SMC TDO	R5078	10K	1	2	5%	1/16W MF-LF 402
SMC TDI	R5079	10K	1	2	5%	1/16W MF-LF 402
SMC TCK	R5080	10K	1	2	5%	1/16W MF-LF 402
SMC BIL BUTTON L	R5081	10K	1	2	5%	1/16W MF-LF 402
SMC BC ACOK	R5087	470K	1	2	5%	1/16W MF-LF 402
SMS INT L	R5093	10K	1	2	5%	1/16W MF-LF 402
SMC P92	R5076	100K	1	2	5%	1/16W MF-LF 402
SMC PA0	R5091	100K	1	2	5%	1/16W MF-LF 402
SMC EXCARD OC L	R5092	100K	1	2	5%	1/16W MF-LF 402
SMC ADAPTER EN	R5085	10K	1	2	5%	1/16W MF-LF 402
SMC CASE OPEN	R5086	10K	1	2	5%	1/16W MF-LF 402
SMC EXCARD CP	R5088	10K	1	2	5%	1/16W MF-LF 402
PM SLP S5 L	R5090	100K	1	2	5%	1/16W MF-LF 402
PM SLP S4 L	R5094	100K	1	2	5%	1/16W MF-LF 402

Debug Power "Buttons"



SYNC MASTER=K18 SENSORS      SYNC DATE=06/29/2009

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## D



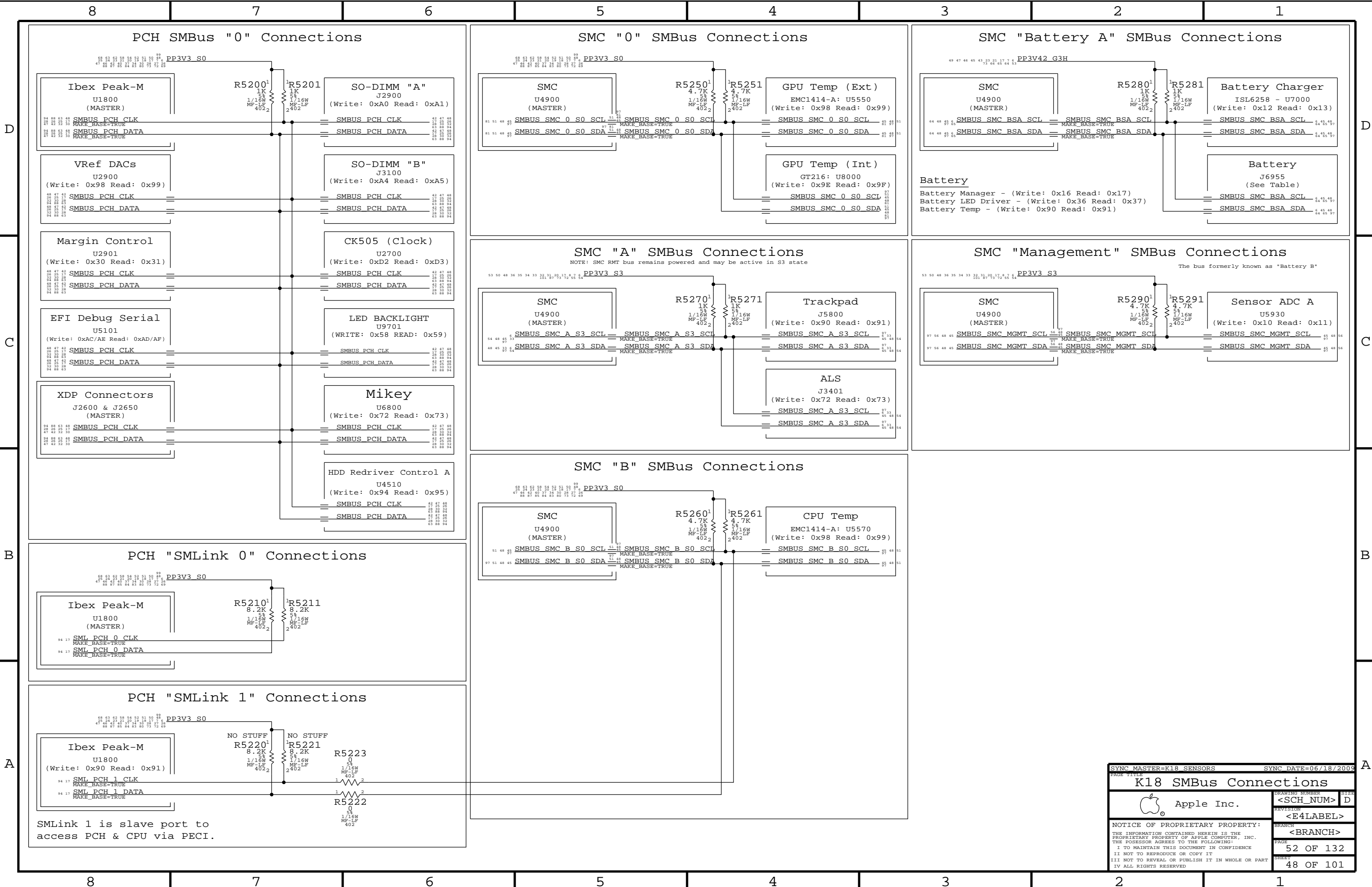
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## A

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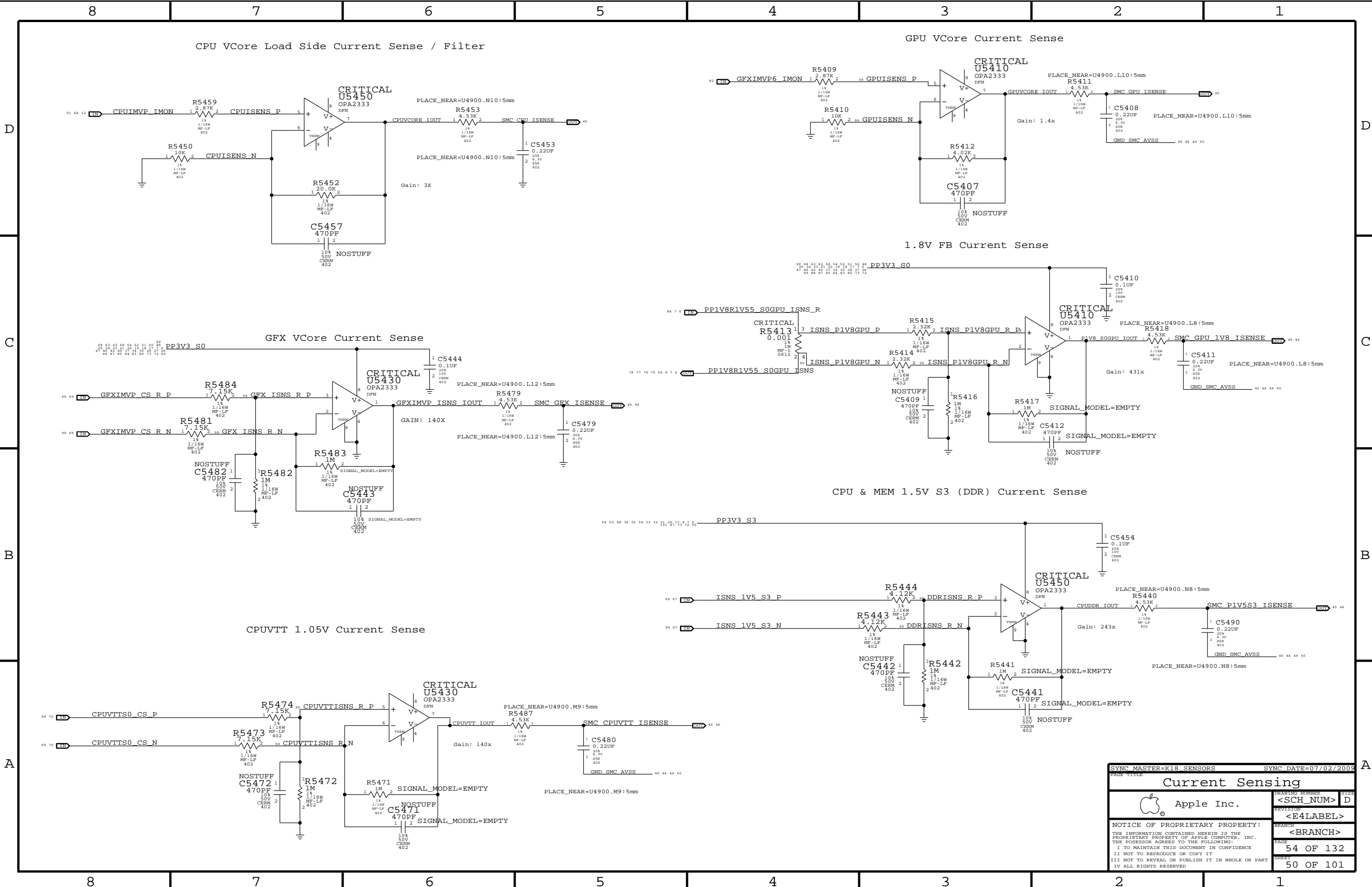
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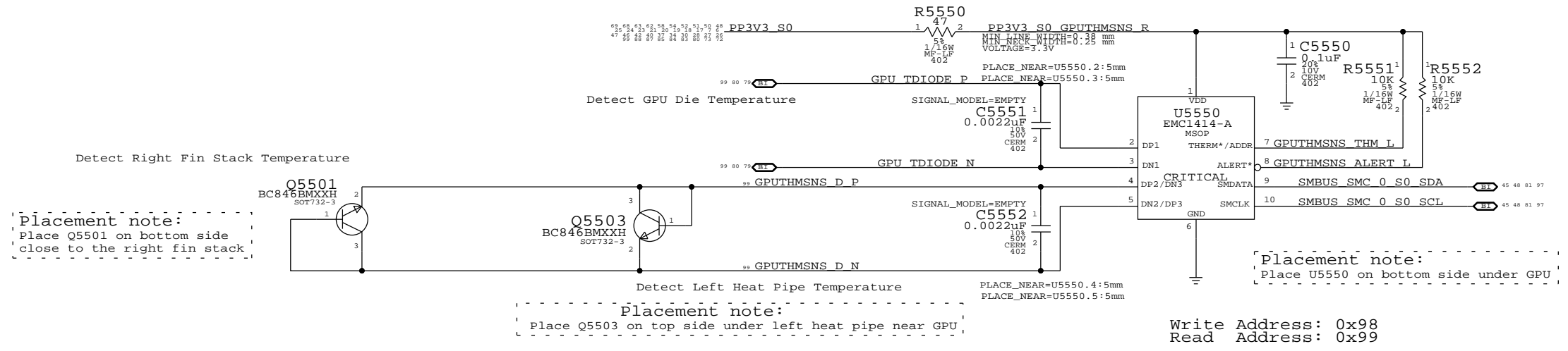




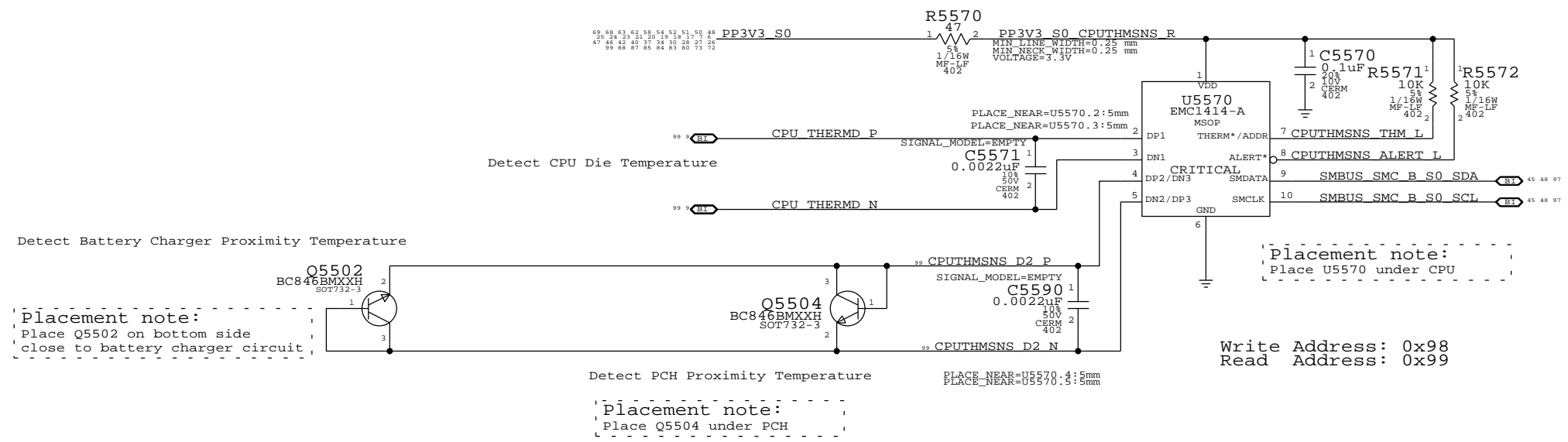


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		SHEET	50 OF 101


GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack

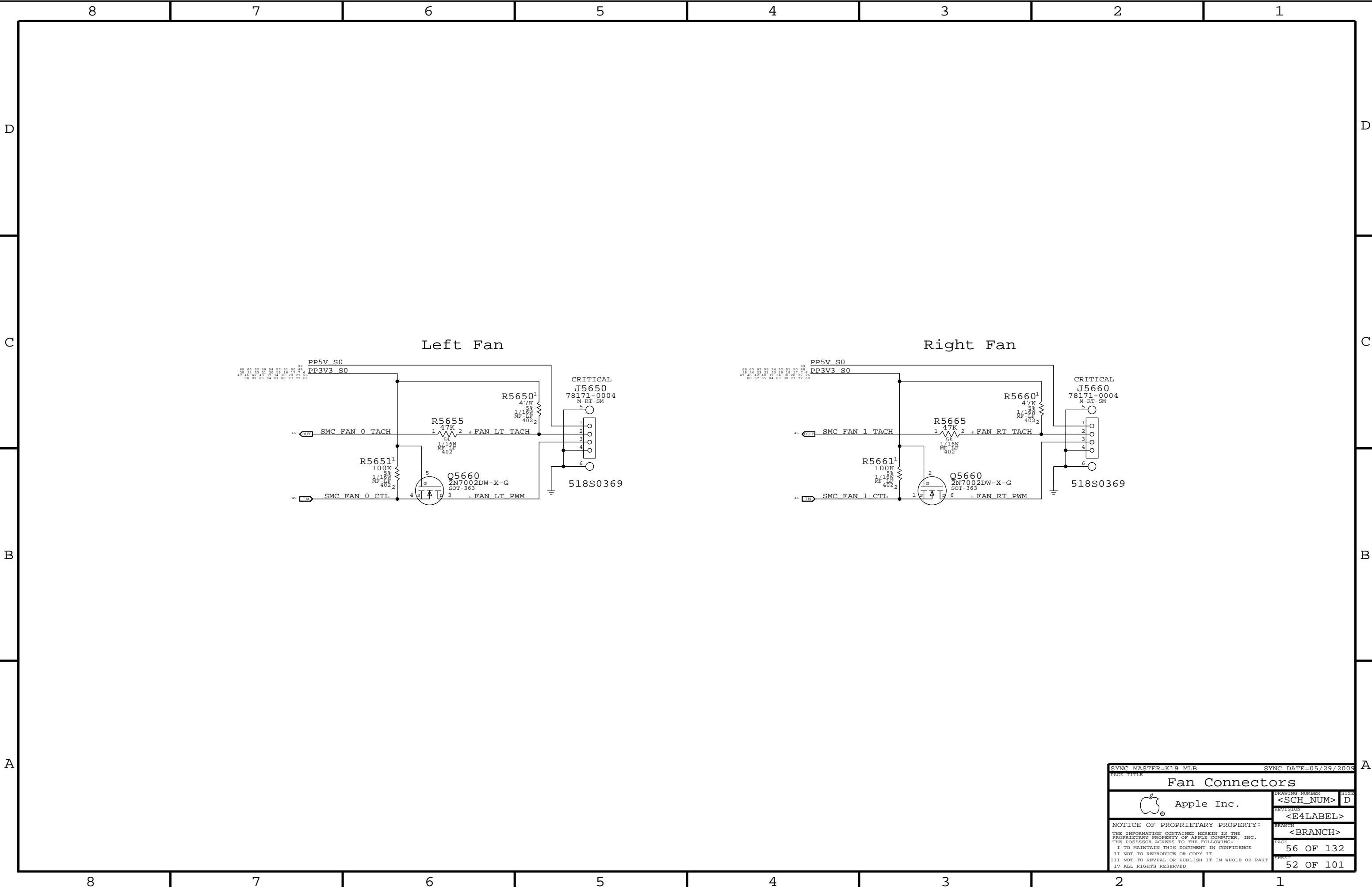


CPU Proximity/CPU Die/PCH Proximity/Battery Charger Proximity



Note: EMC1414 can perform Beta Compensation for External Diode 1 only


SYNC MASTER=K18_SENSORS		SYNC DATE=06/18/2009	
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SYNC MASTER=K19 MLB

SYNC DATE=05/29/2009

Fan Connectors

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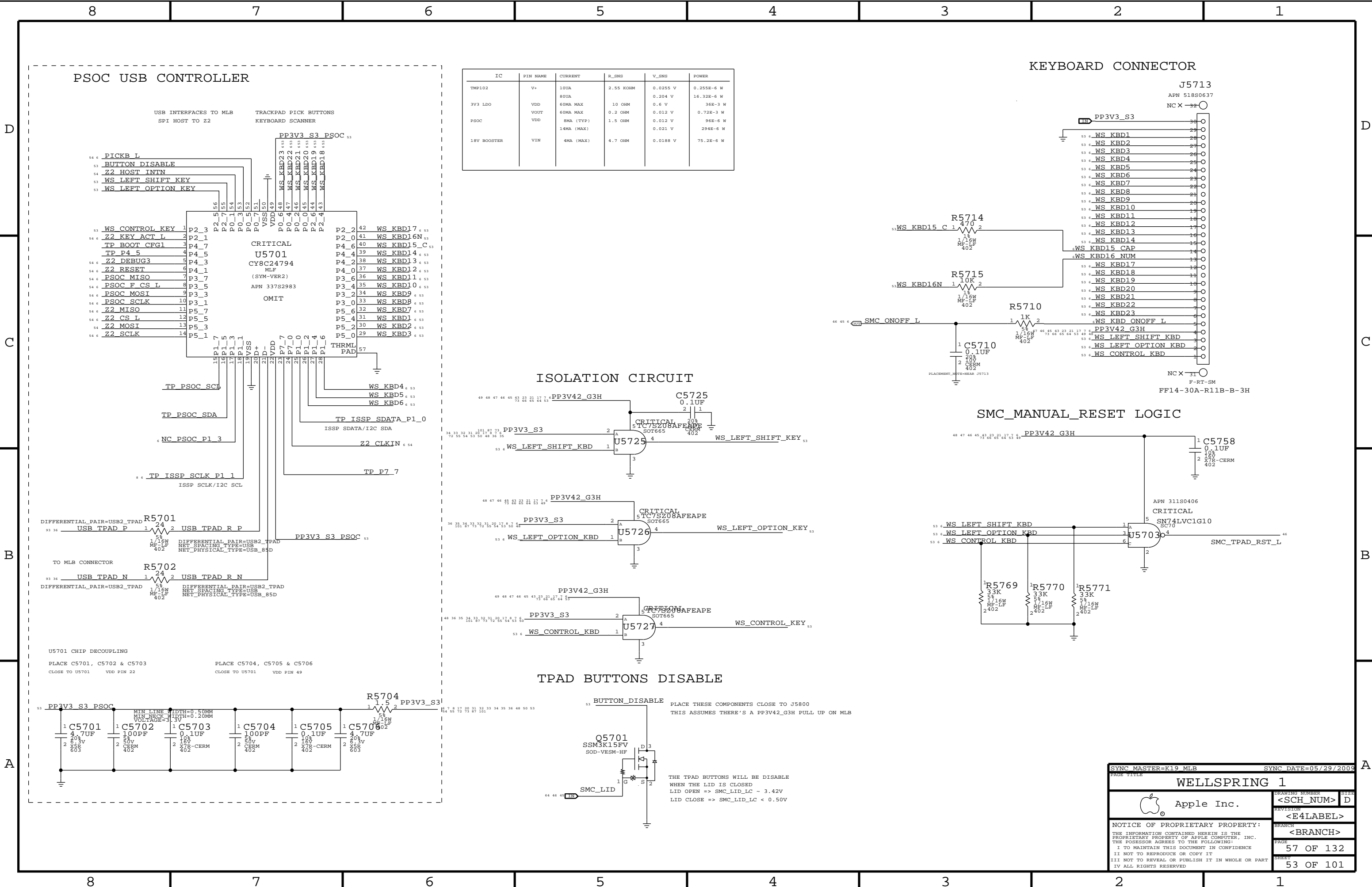
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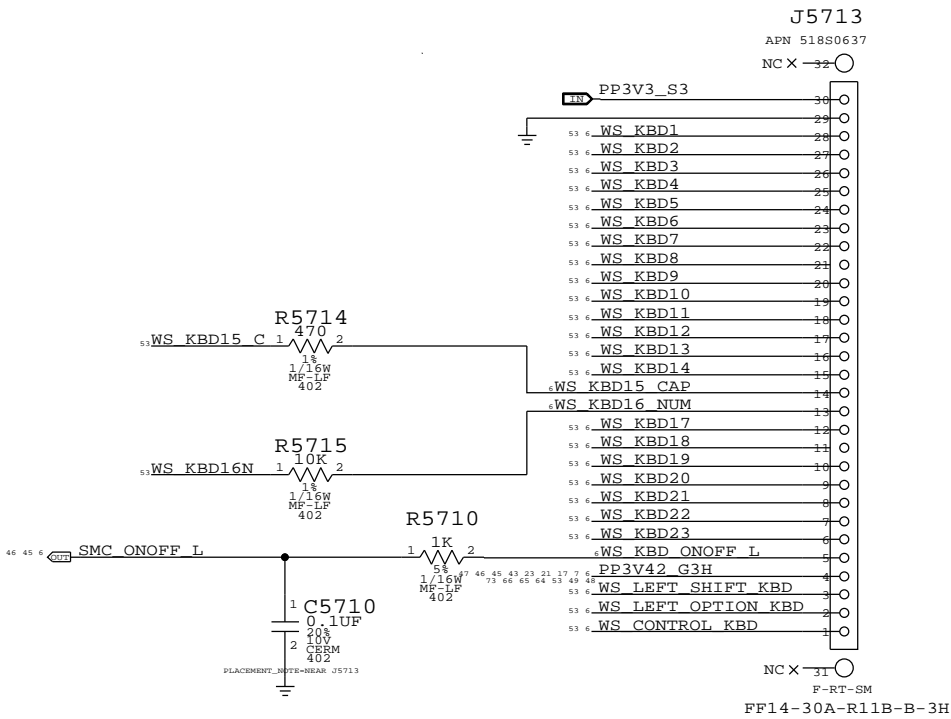
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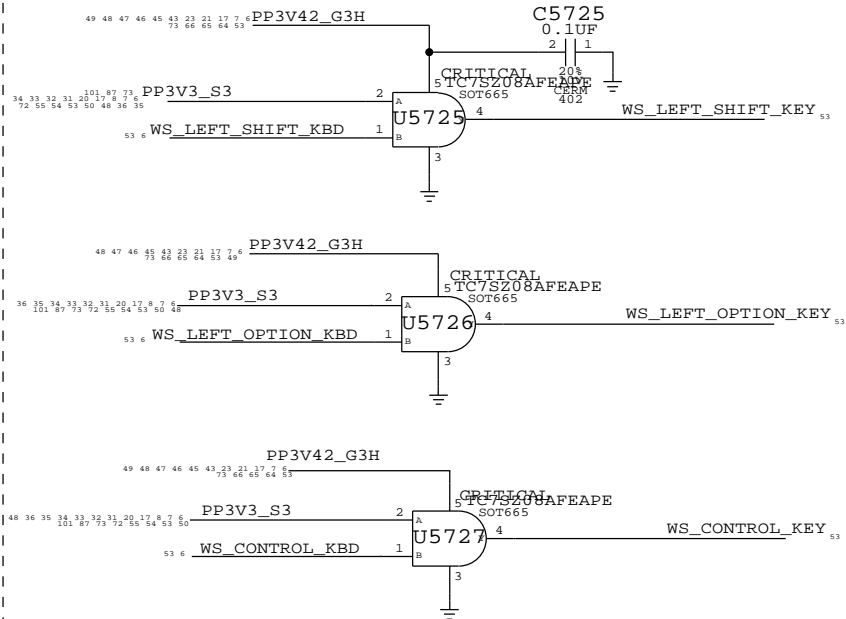


IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	100A	2.55 KOHM	0.0255 V	0.255E-6 W
3V3 LDO	VDD	800A	10 OHM	0.204 V	16.32E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TVP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
1.8V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

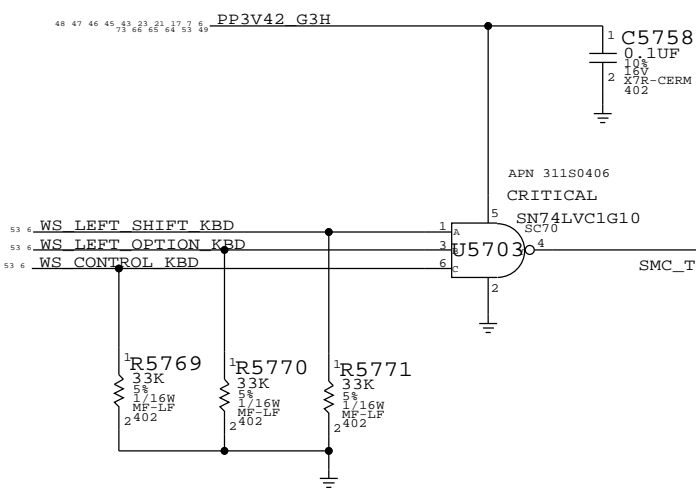
KEYBOARD CONNECTOR



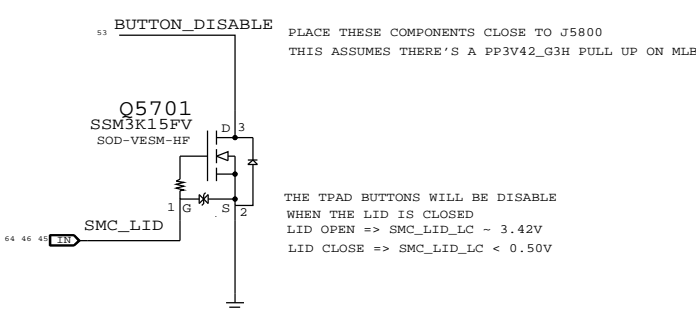
ISOLATION CIRCUIT



SMC\_MANUAL\_RESET LOGIC



TPAD BUTTONS DISABLE



SYNC MASTER=K19\_MLB

SYNC DATE=05/29/2009

WELLSPRING 1

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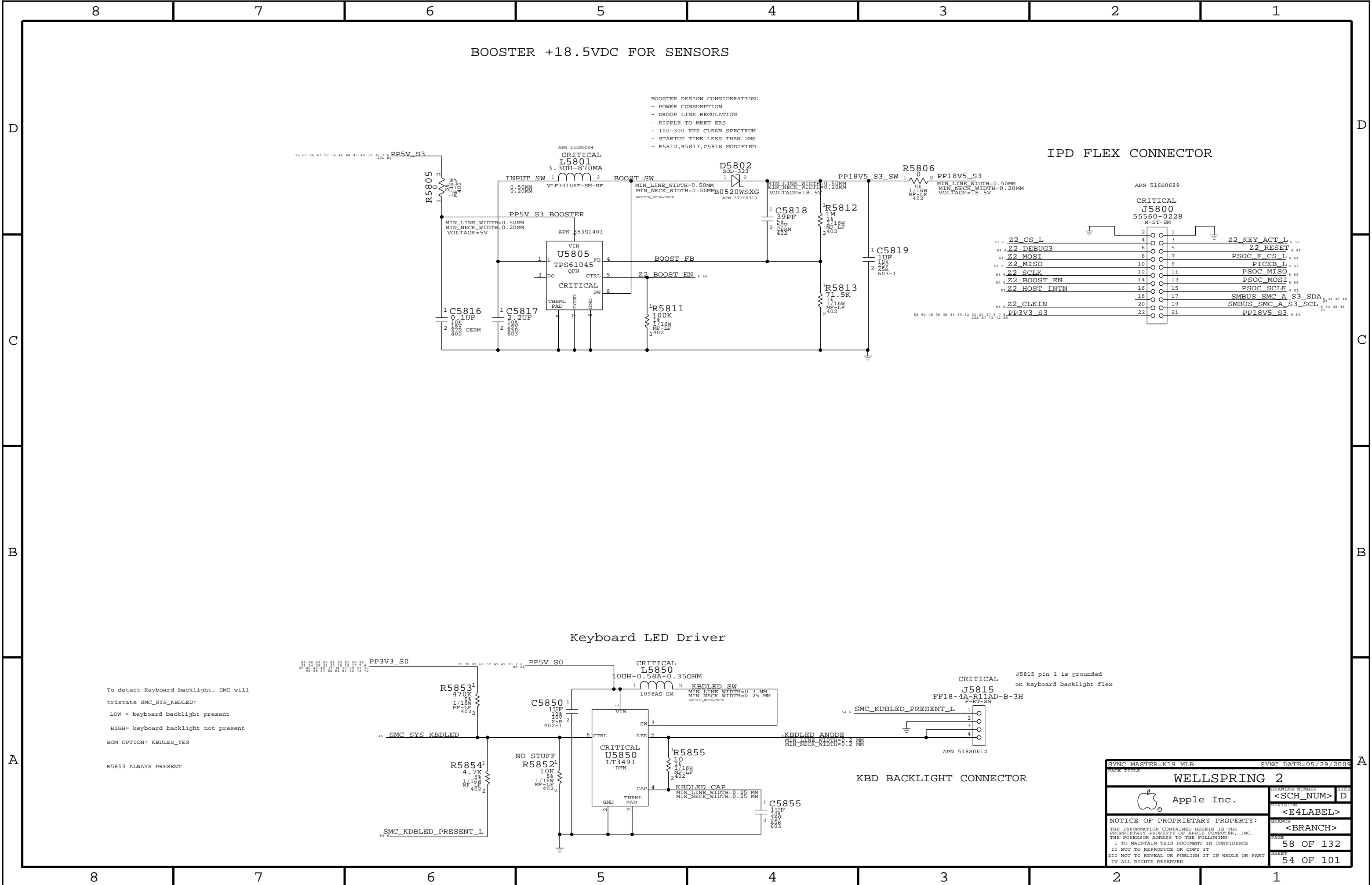
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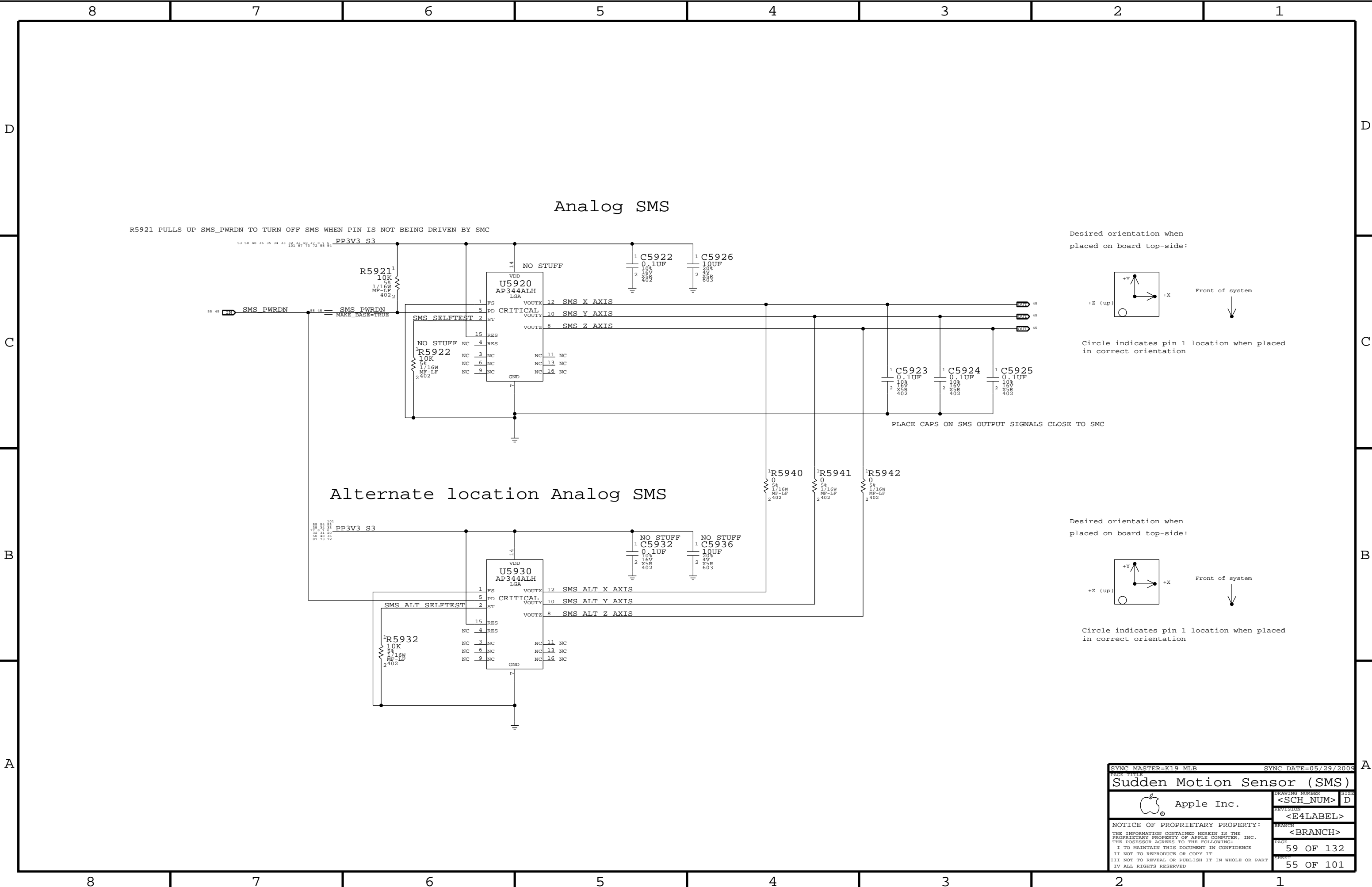
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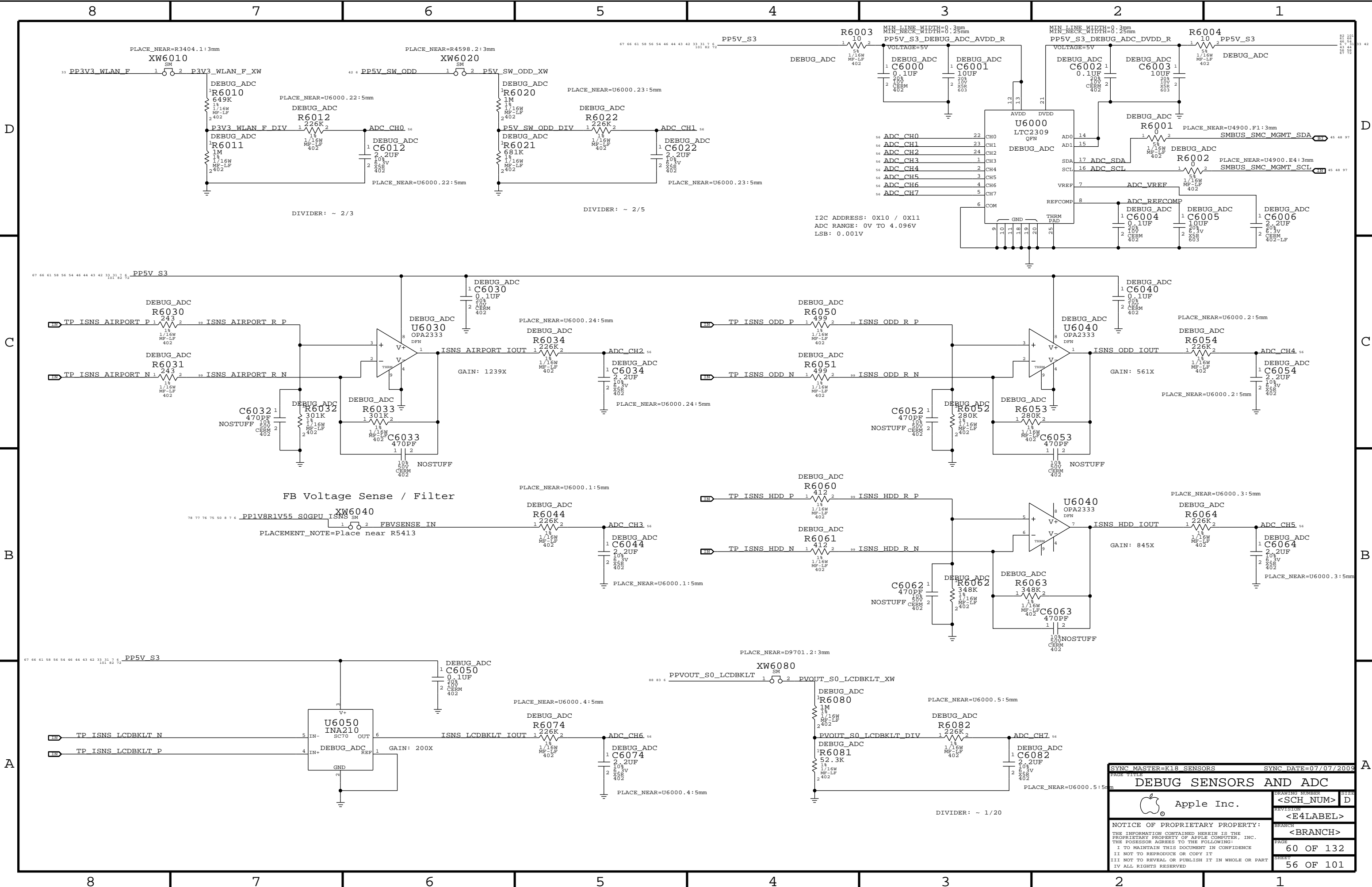
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
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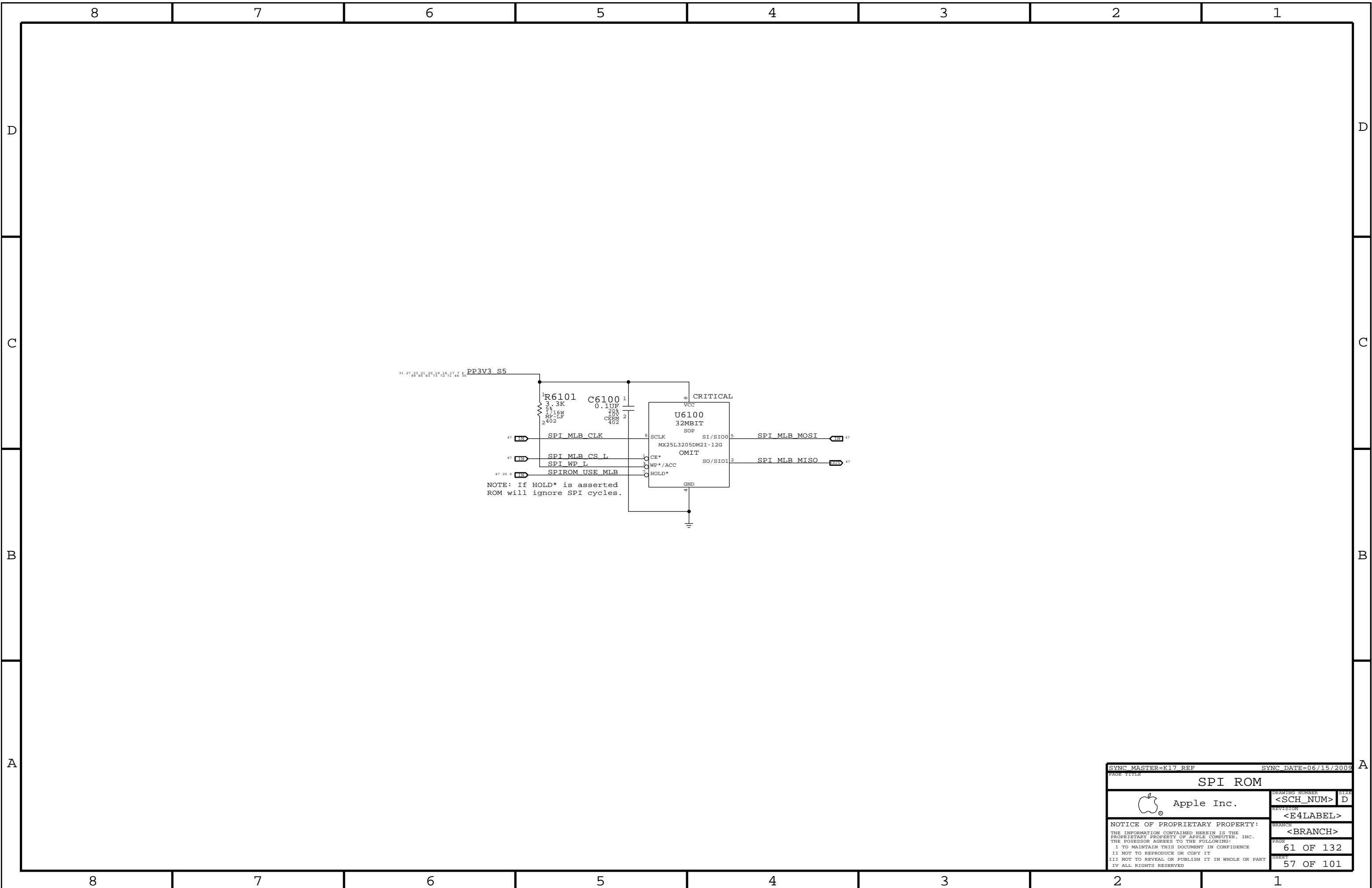





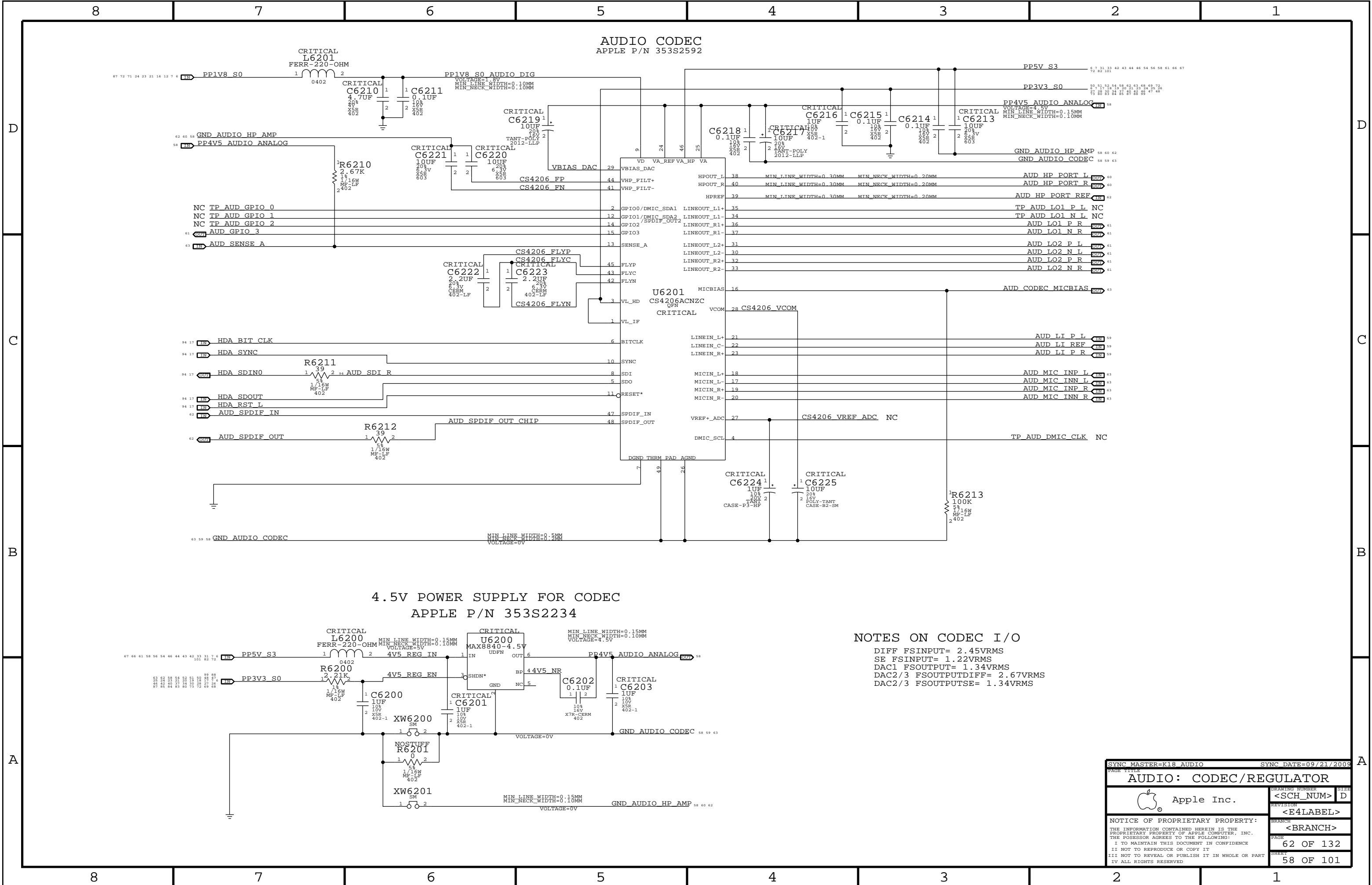


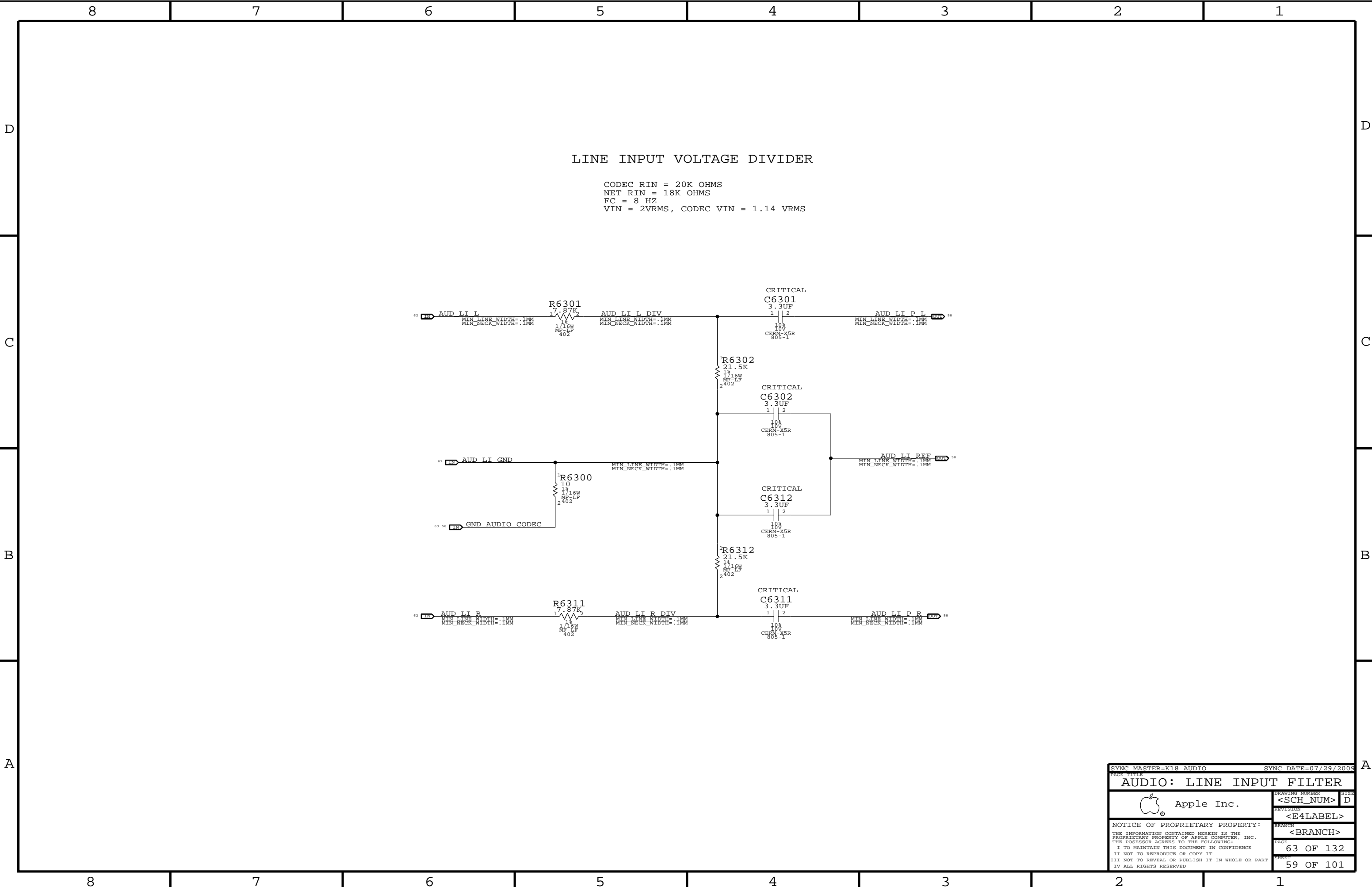
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DEBUG SENSORS AND ADC			
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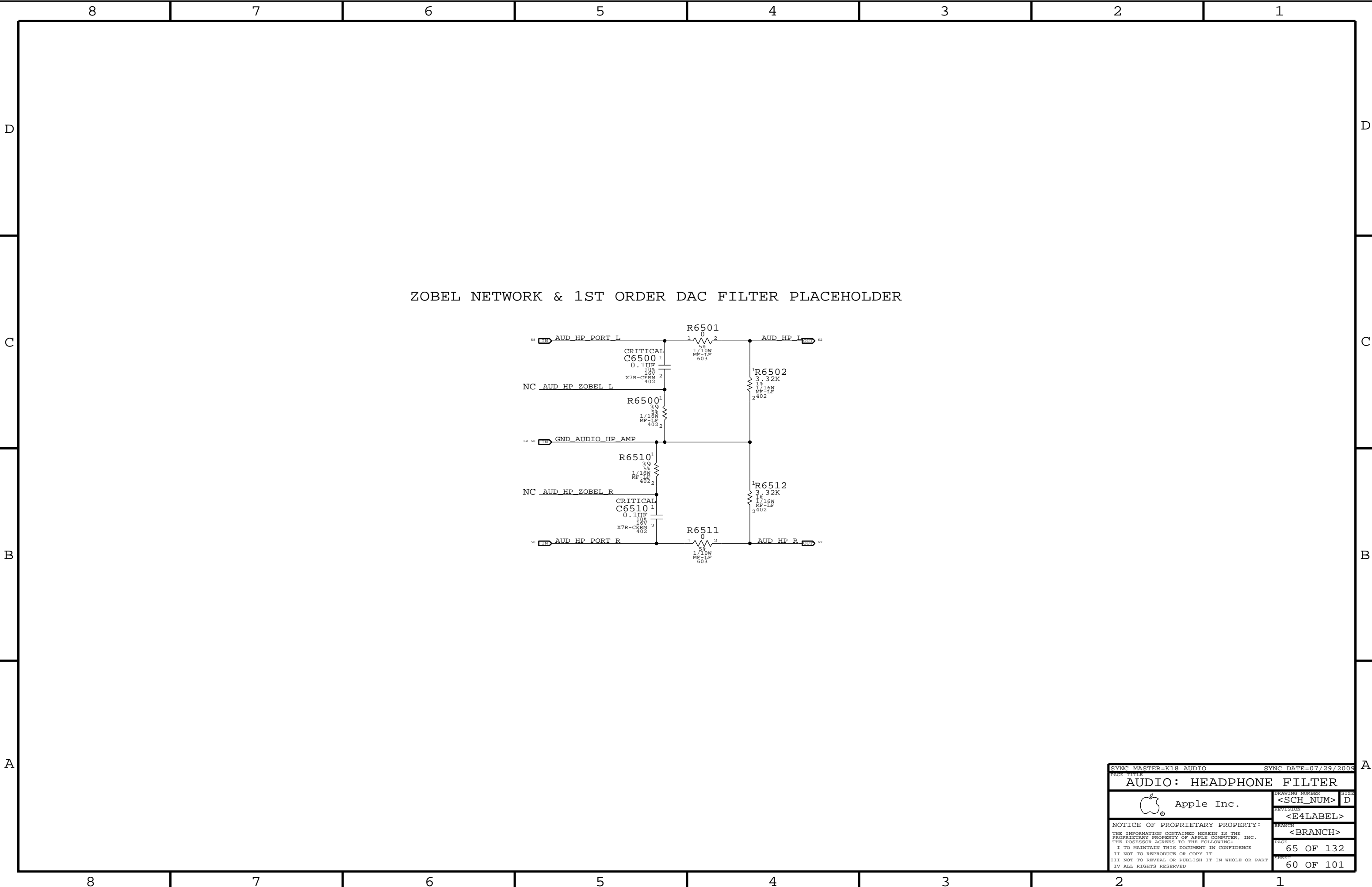



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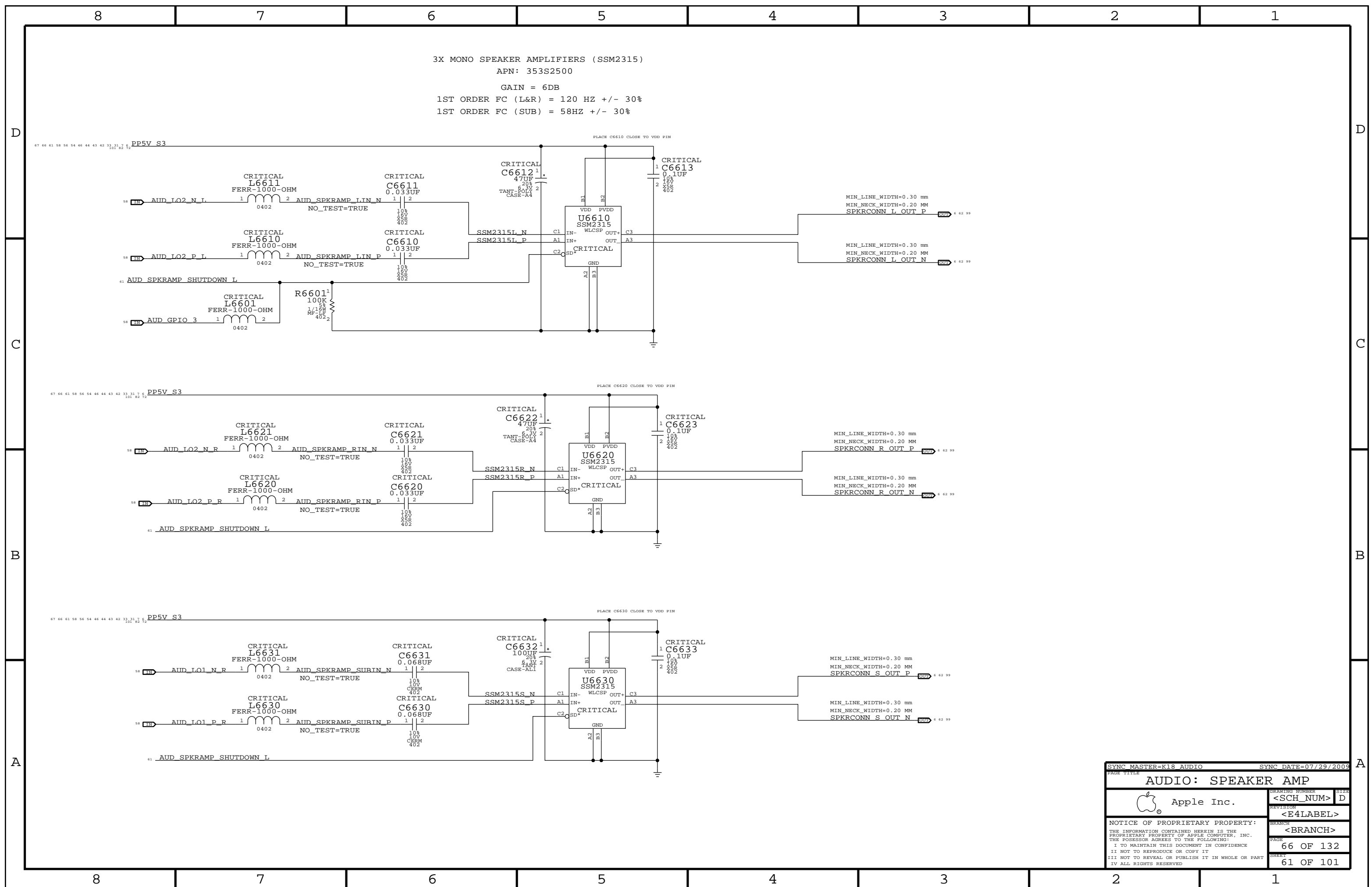




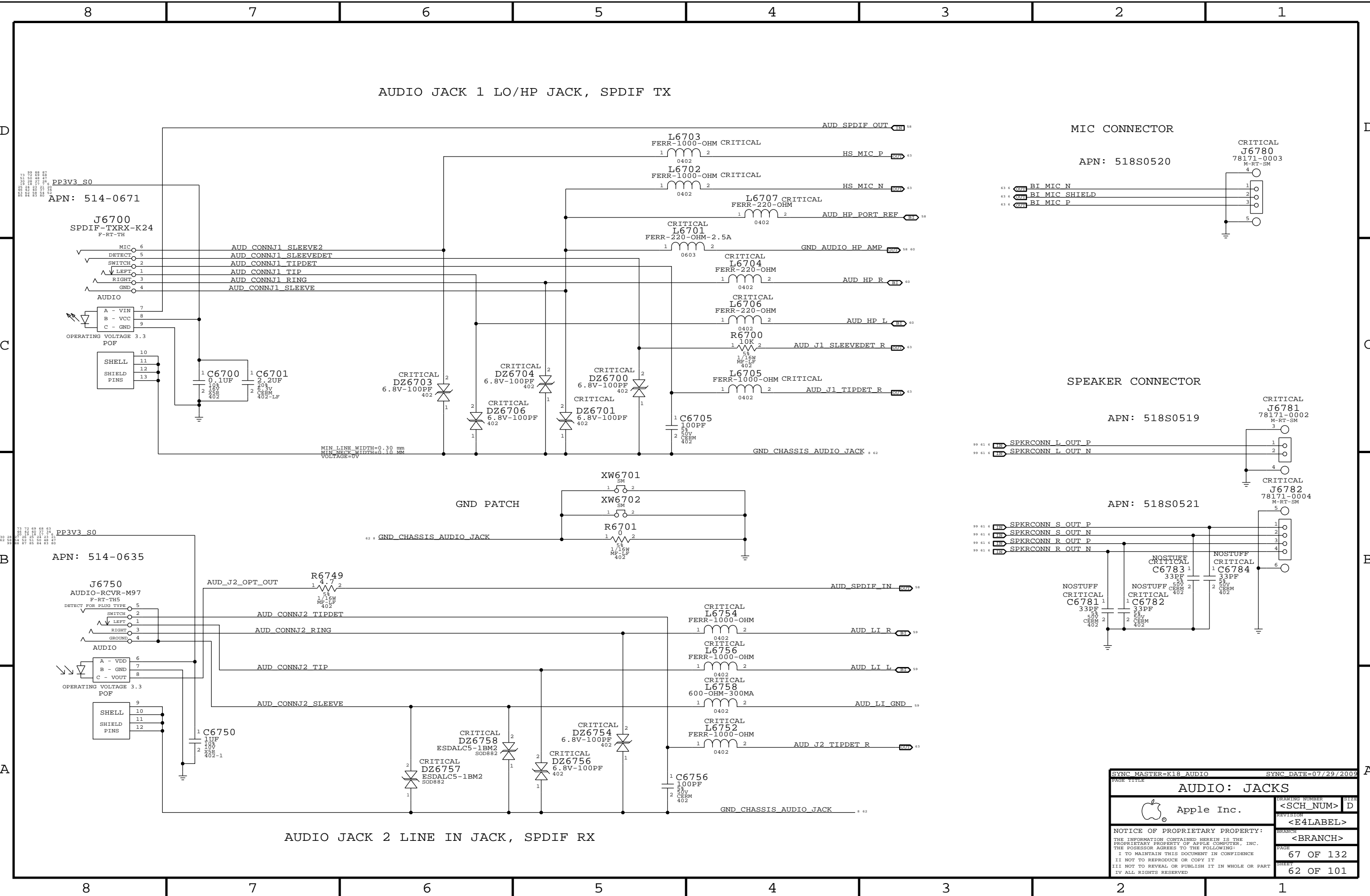
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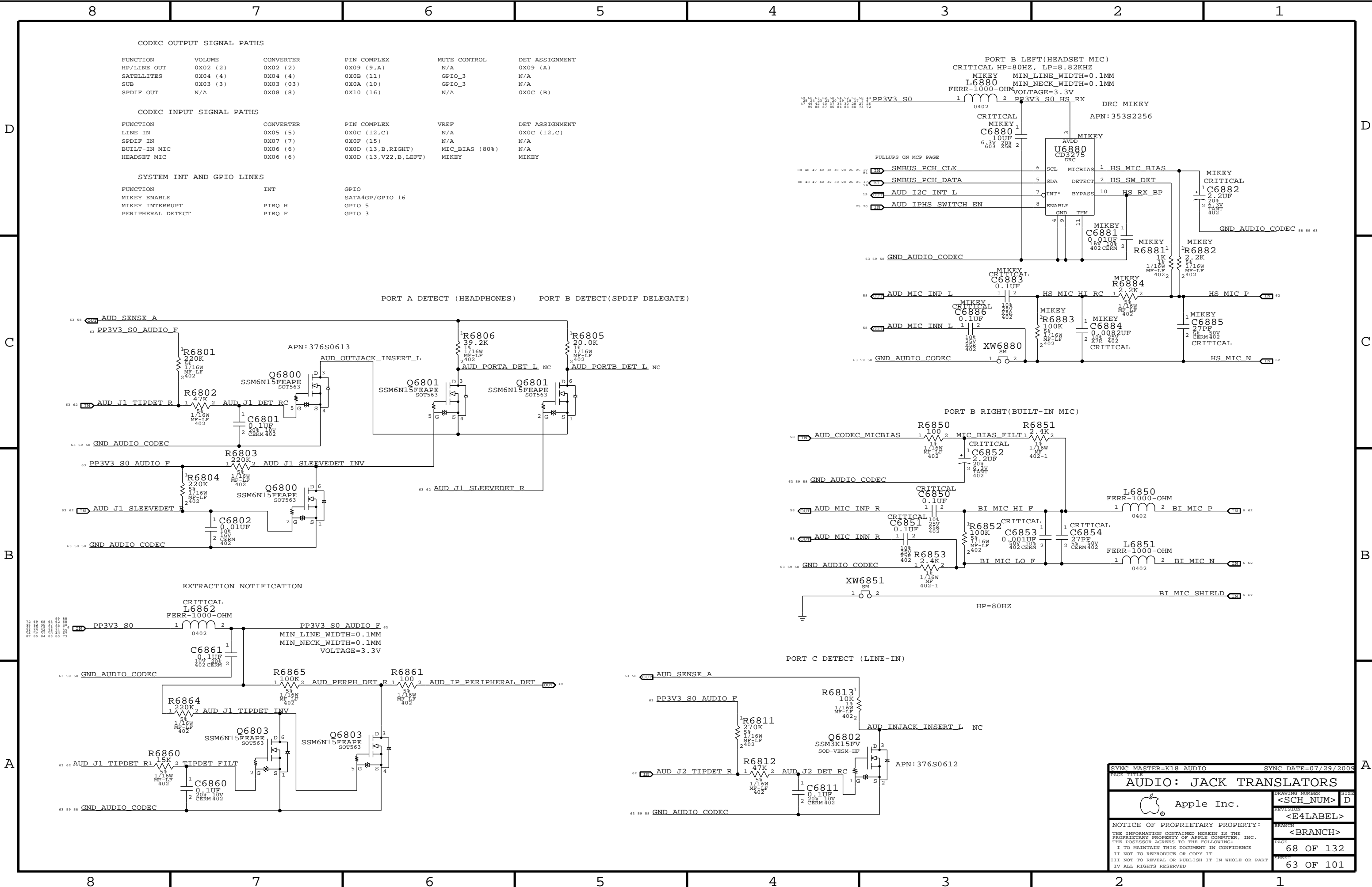
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		PAGE	67 OF 132
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3


PORT A DETECT (HEADPHONES) PORT B DETECT (SPDIF DELEGATE)

PORT B LEFT(HEADSET MIC)  
CRITICAL HP=80HZ, LP=8.82KHZ  
MIKEY MIN\_LINE\_WIDTH=0.1MM  
L6880 MIN\_NECK\_WIDTH=0.1MM  
FERR-1000-OHM VOLTAGE=3.3V

DRC MIKEY  
APN:353S2256

PORT B RIGHT (BUILT-IN MIC)

PORT C DETECT (LINE-IN)

SYNC MASTER=K18 AUDIO		SYNC DATE=07/29/2009	
PAGE TITLE			
AUDIO: JACK TRANSLATORS			
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## D



C

## C



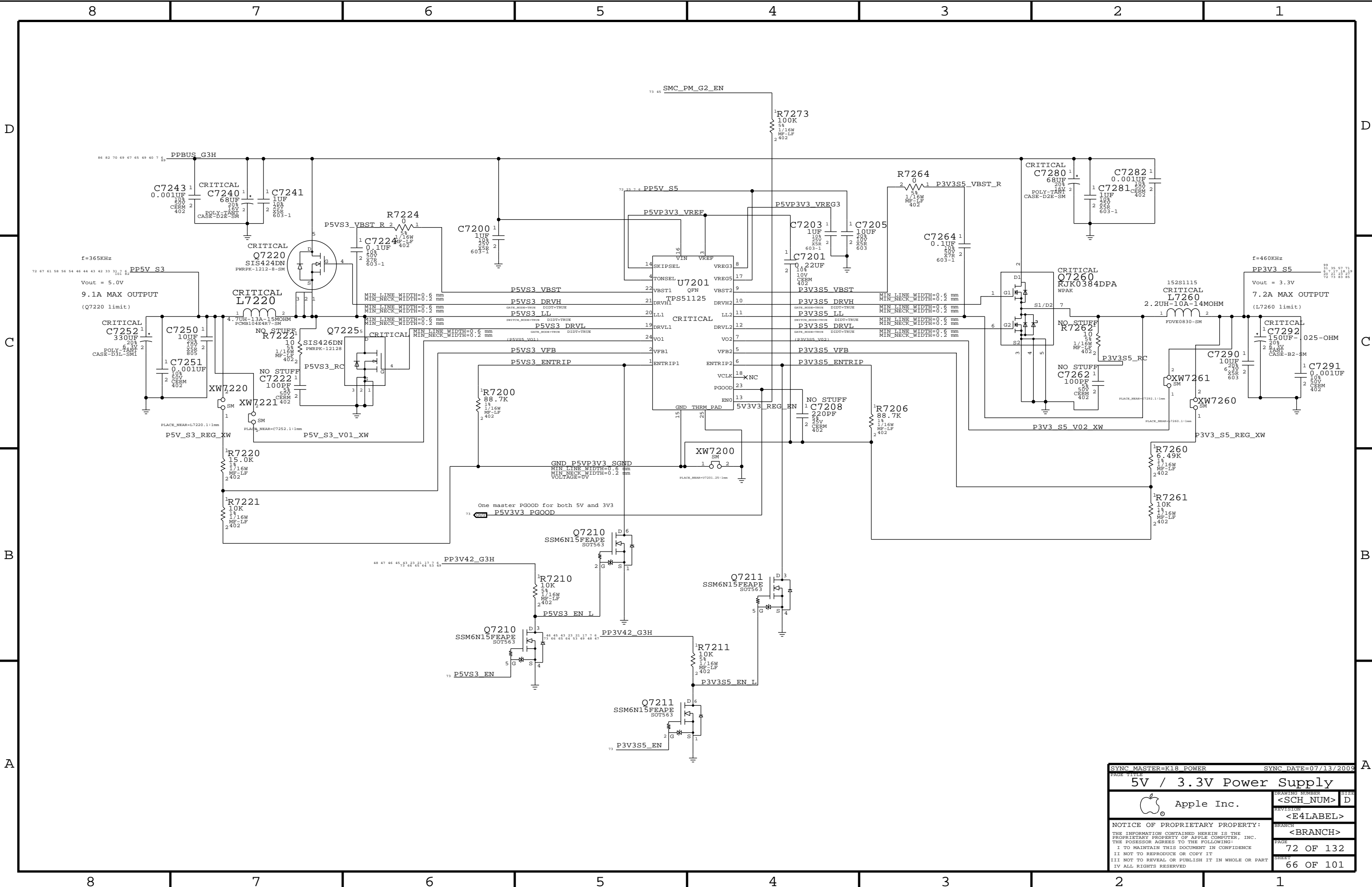
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A



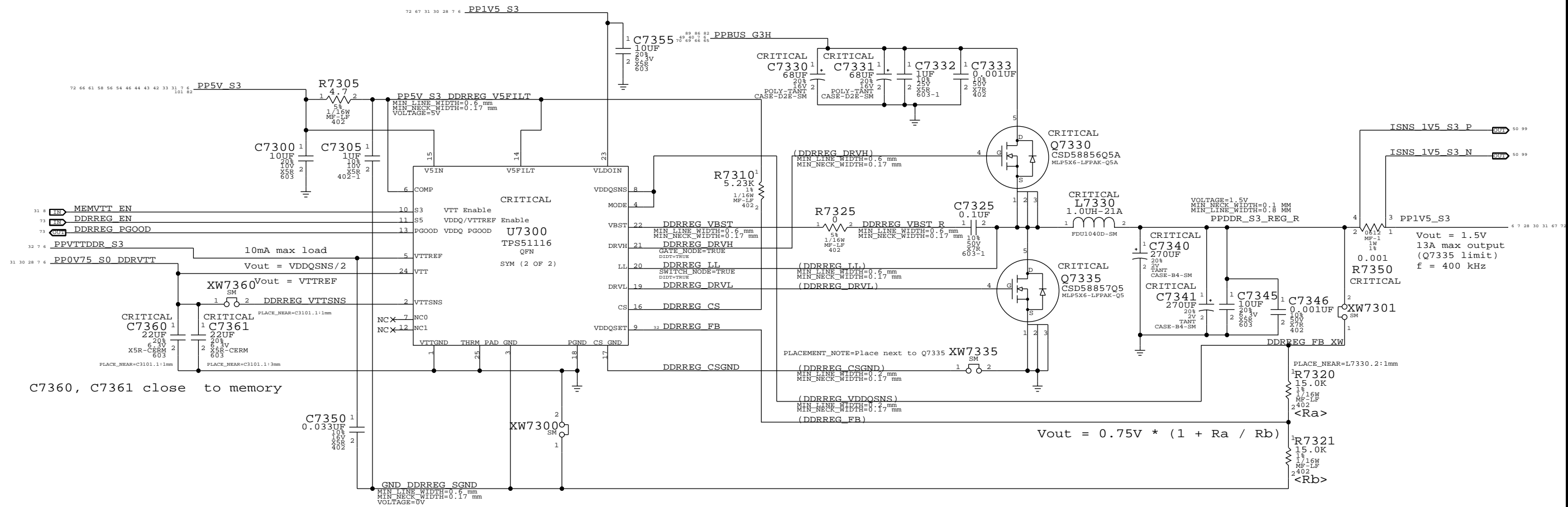
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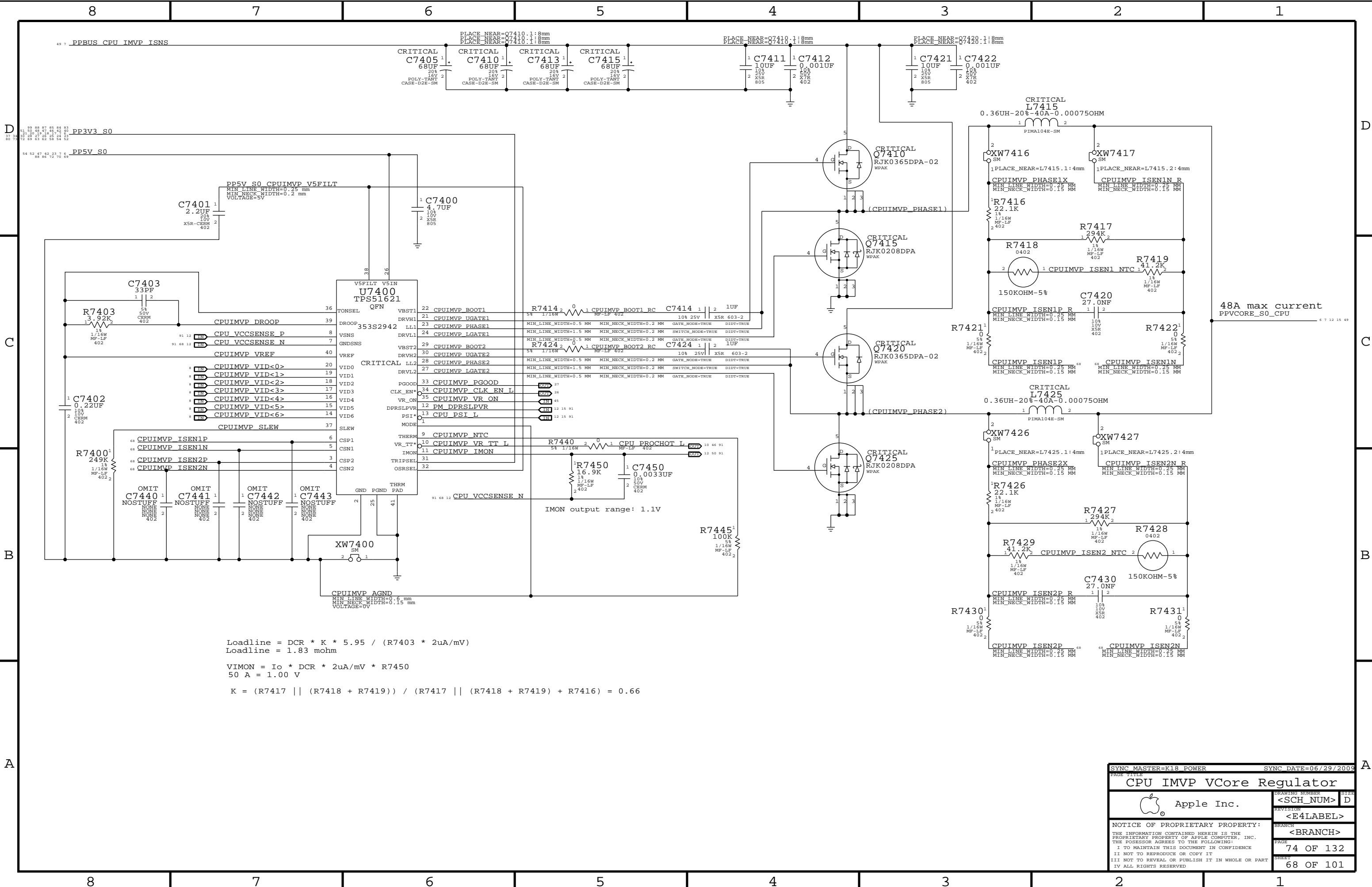


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5V / 3.3V Power Supply			
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1.5V DDR3 Supply			
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Loadline =  $DCR * K * 5.95 / (R7403 * 2uA/mV)$   
Loadline = 1.83 mohm

VIMON =  $I_o * DCR * 2uA/mV * R7450$   
50 A = 1.00 V

$K = (R7417 || (R7418 + R7419)) / (R7417 || (R7418 + R7419) + R7416) = 0.66$

SYNC MASTER=K18 POWER		SYNC DATE=06/29/2009	
PAGE TITLE			
CPU IMVP VCore Regulator			
 Apple Inc.		DRAWING NUMBER	SIZE
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## D



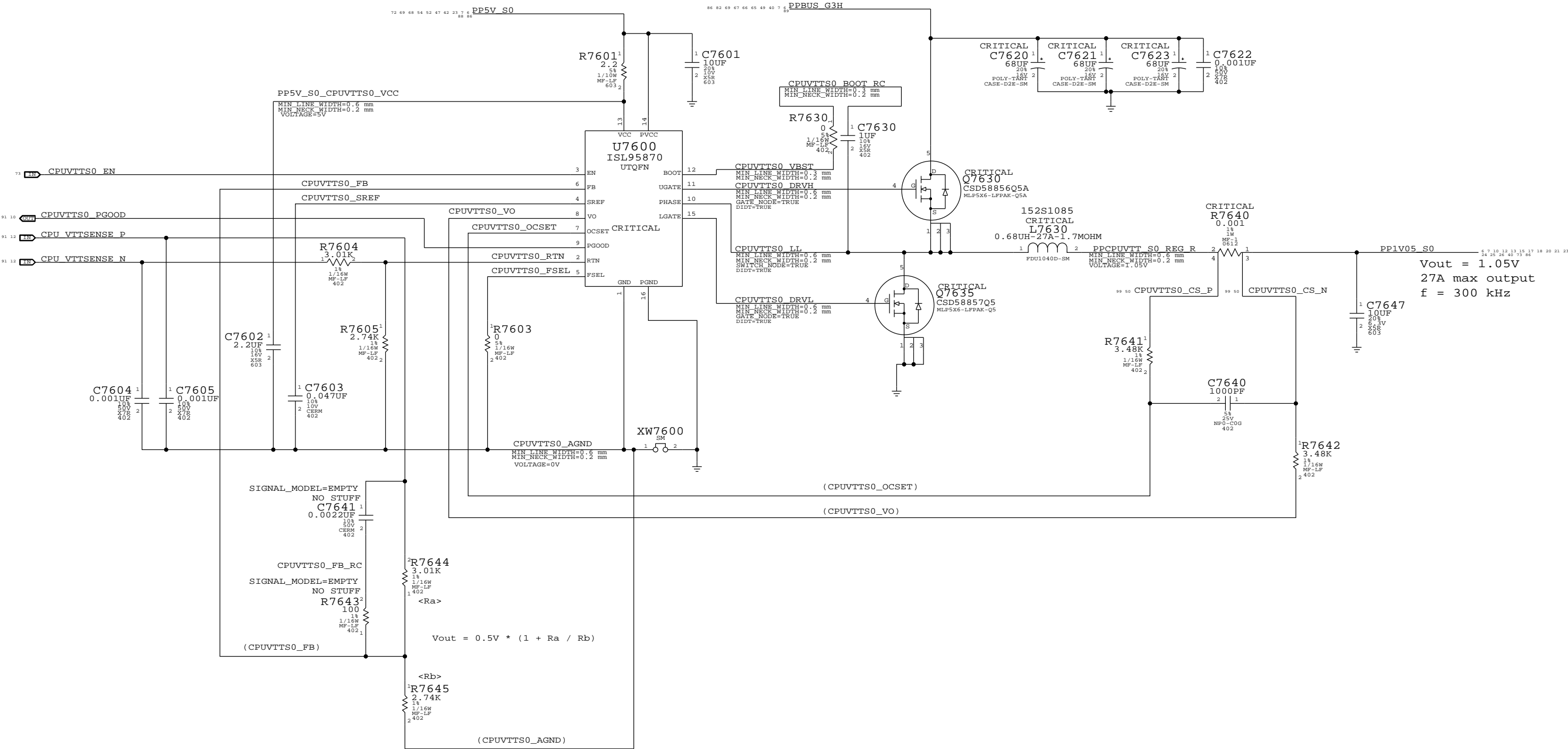
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A

A

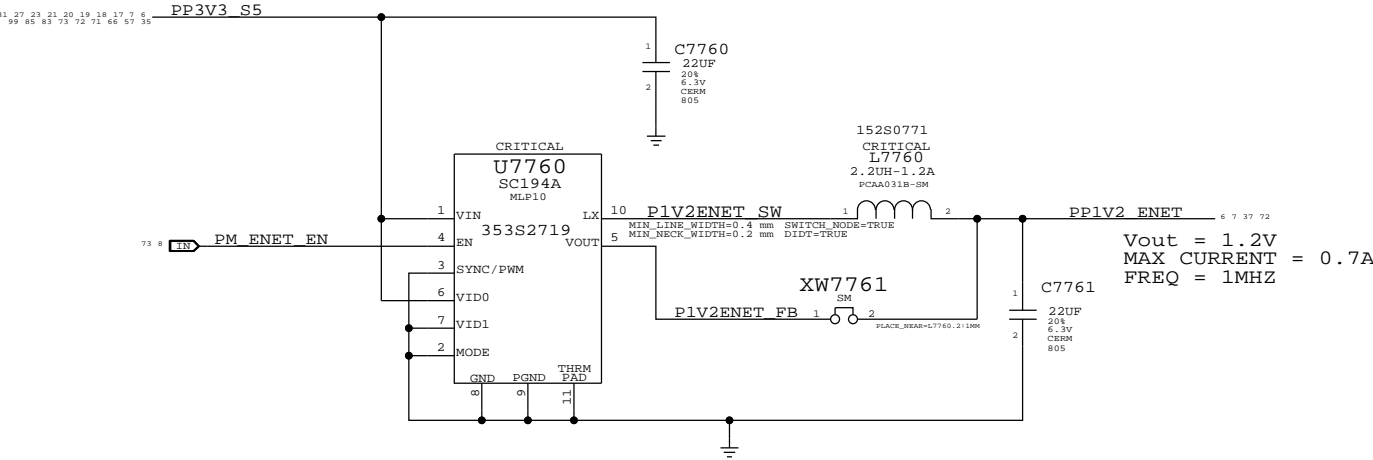
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CPU VTT (1.05V S0) Regulator



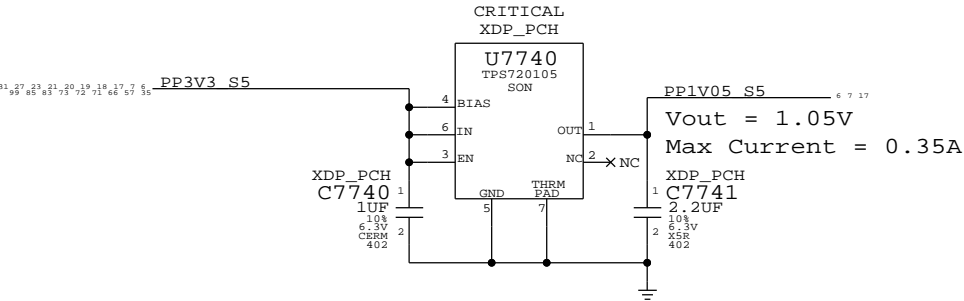
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CPUVTT (1.05V) Power Supply			
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1.2V S3 Regulator

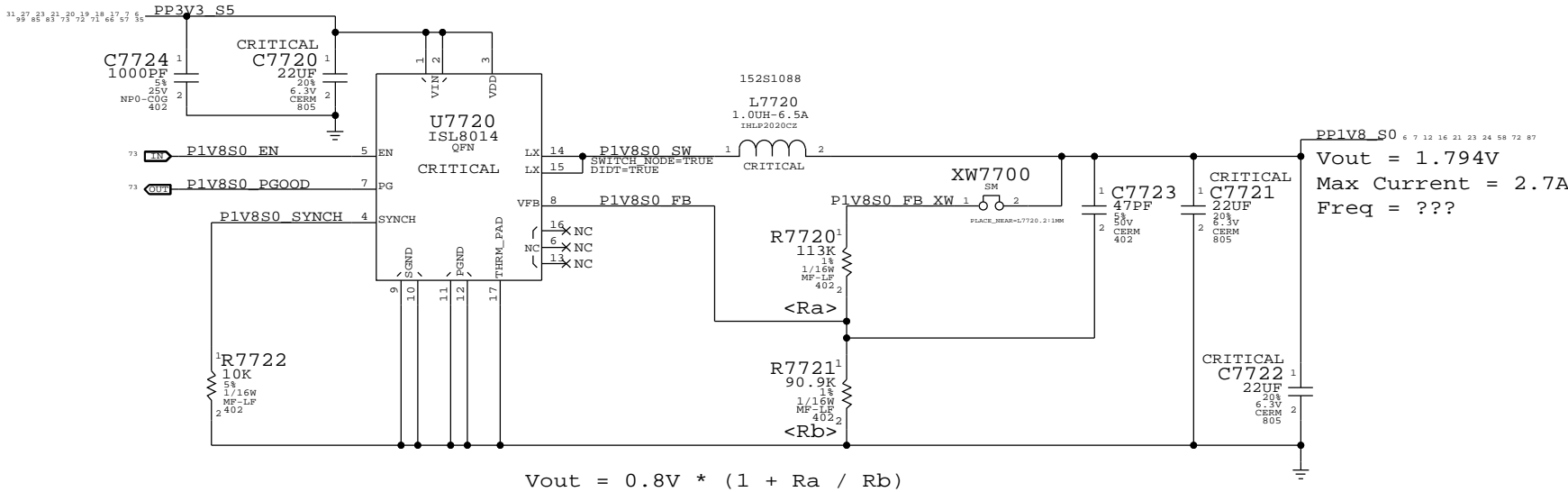


1.05V S5 LDO


Ibex Peak-M requires JTAG pull-ups to be powered at 1.05V in S5. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



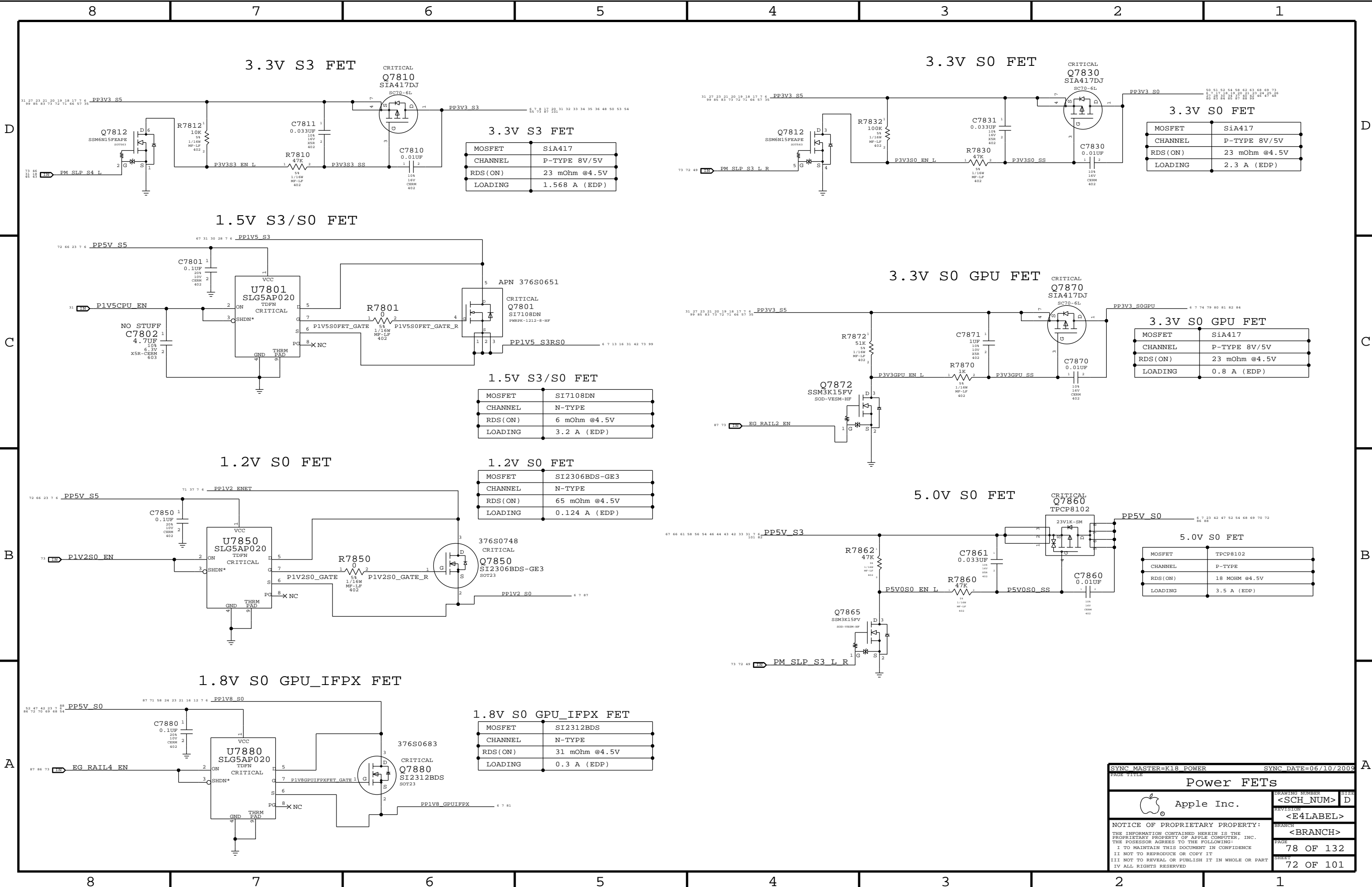
1.8V S0 Regulator



$$V_{out} = 0.8V * (1 + R_a / R_b)$$

SYNC MASTER=K18 POWER		SYNC DATE=06/29/2009	
PAGE TITLE			
Misc Power Supplies			
 Apple Inc.		DRAWING NUMBER	SIZE
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SYNC MASTER=K18 POWER

SYNC DATE=06/10/2009

Power FETs

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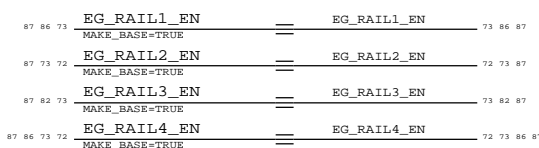
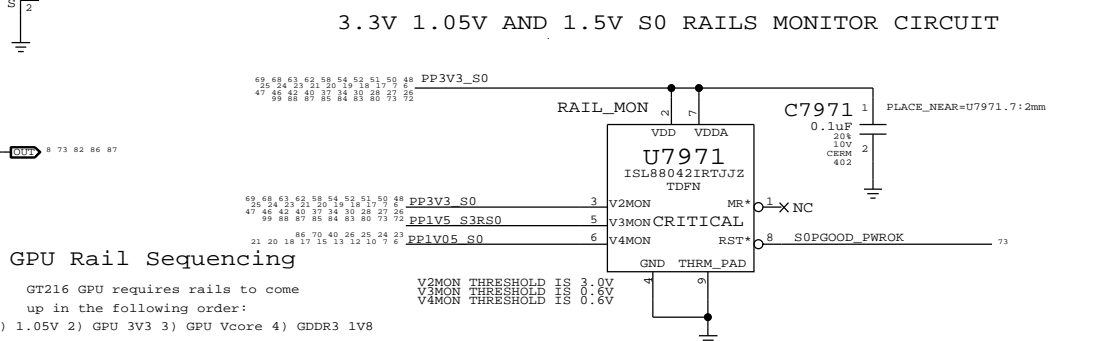
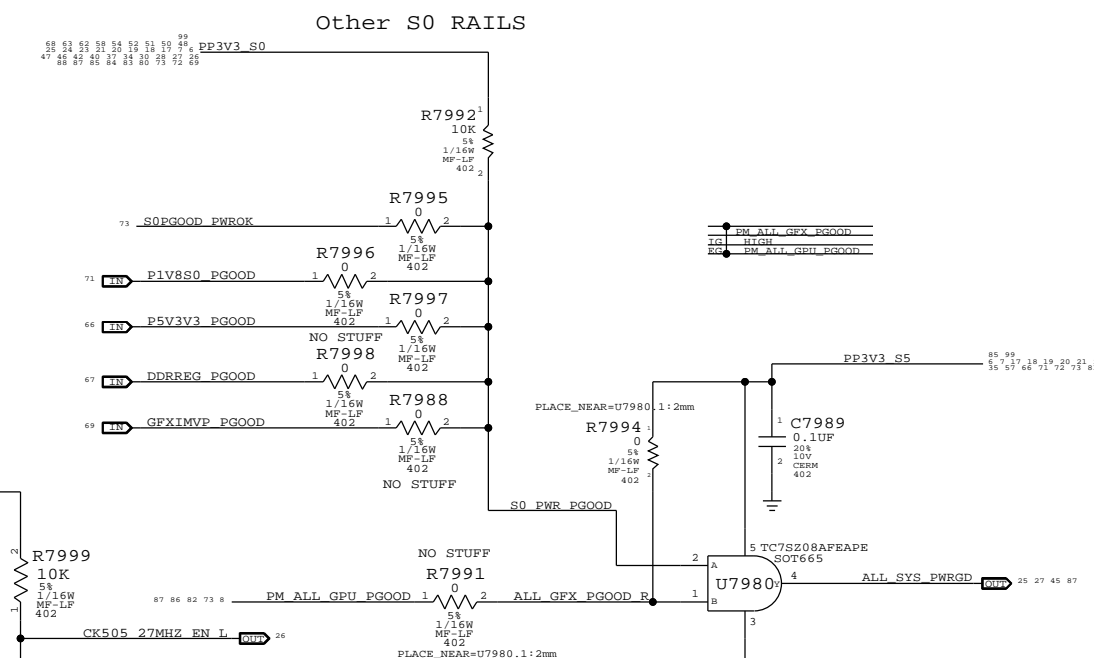
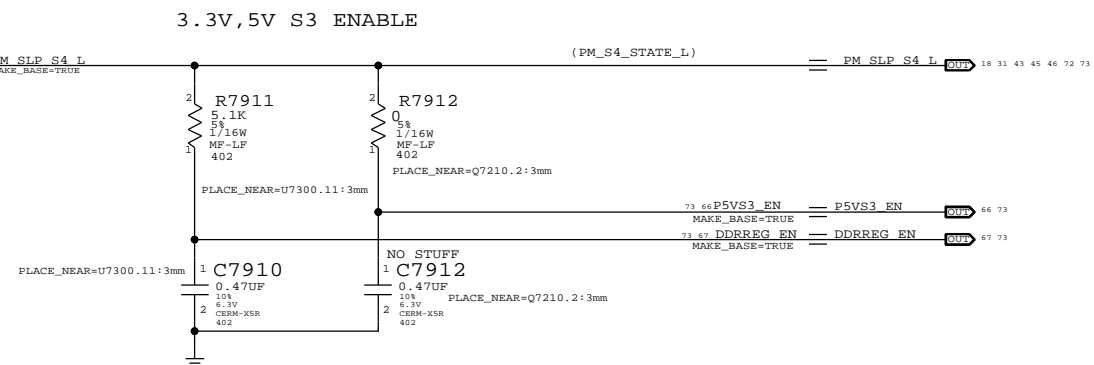
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
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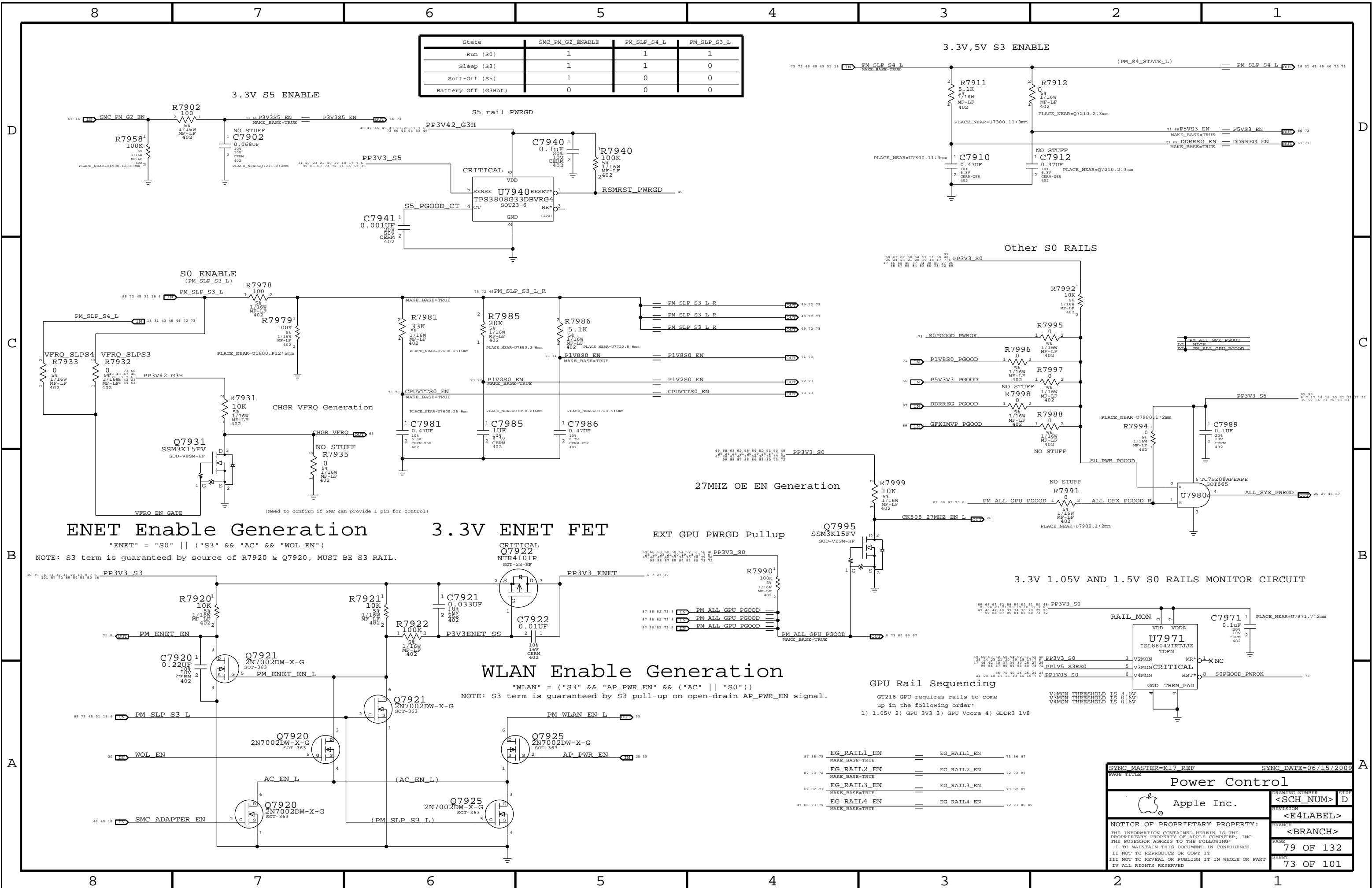
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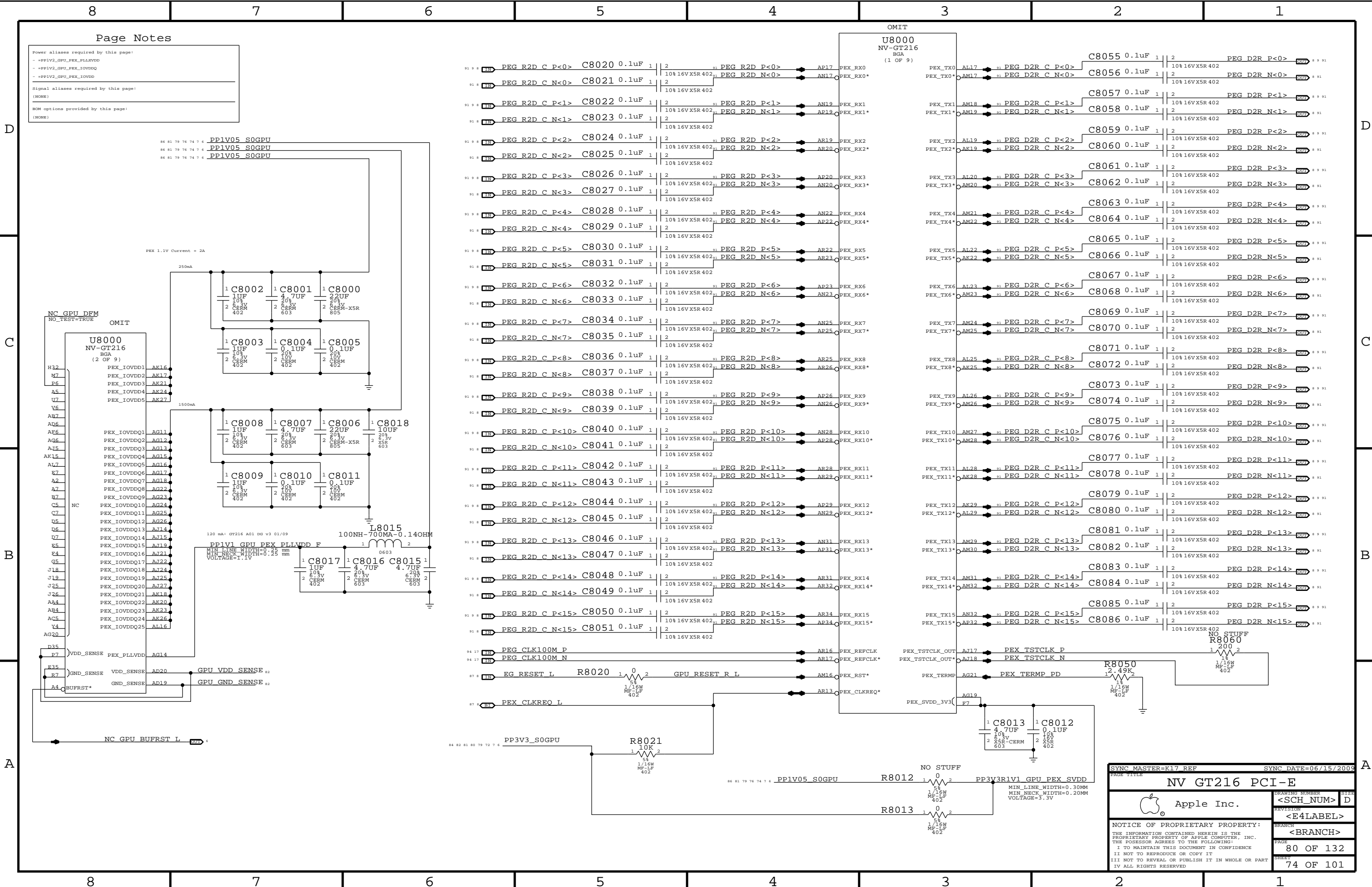
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State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

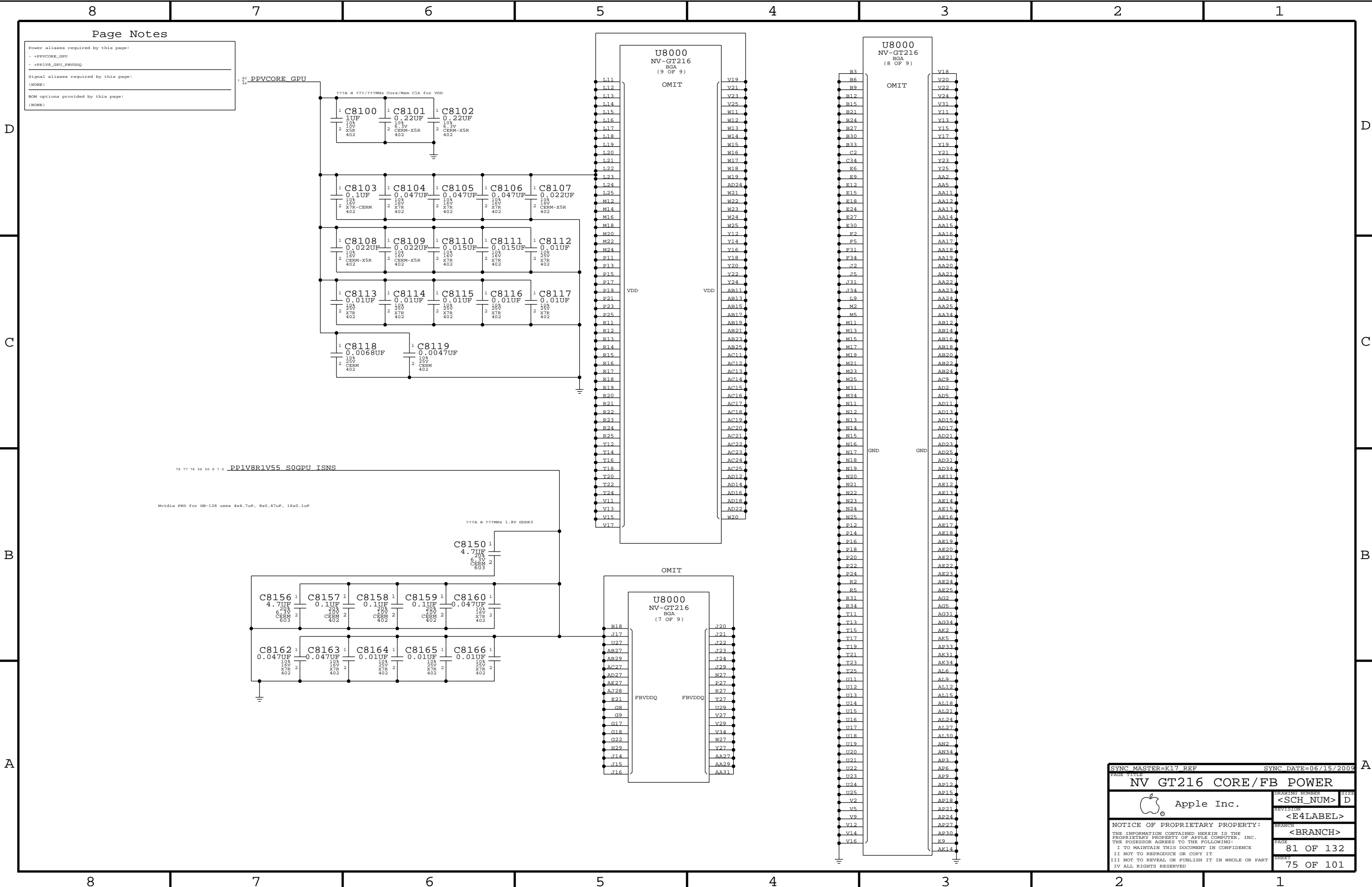


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Power Control			
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SYNC MASTER=K17 REF		SYNC DATE=06/15/2009	
PAGE TITLE		NV GT216 PCI-E	
Apple Inc.		DRAWING NUMBER	<SCH_NUM> D
		REVISION	<E4LABEL>
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Page Notes

Power aliases required by this page:

- =PPVCORE\_GPU
- =PP1V8\_GPU\_FBVDDQ

Signal aliases required by this page:

(NONE)


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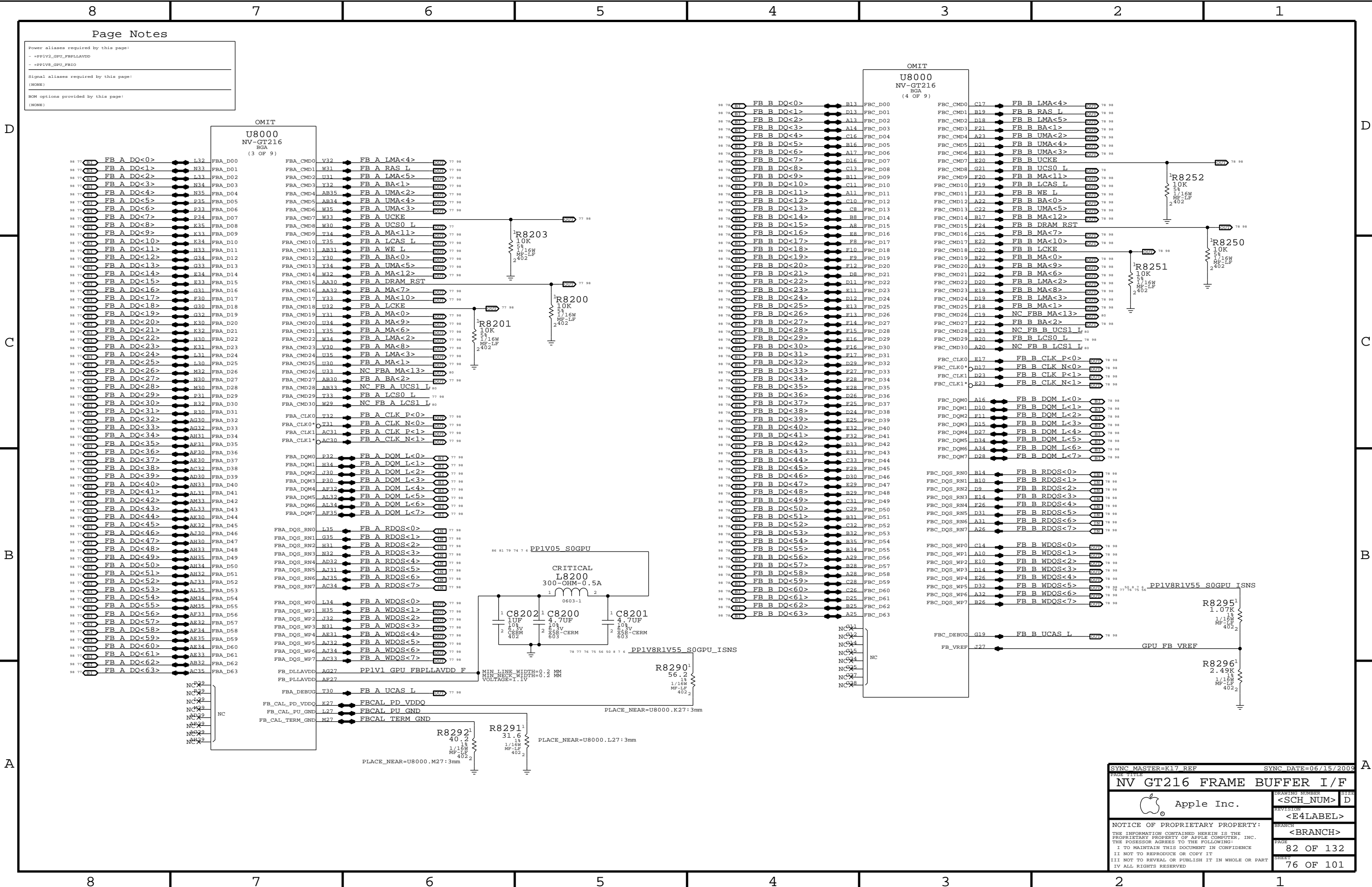
PP1V8R1V55 S0GPU ISNS

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???MHz 1.8V GDDR3

SYNC MASTER=K17 REF		SYNC DATE=06/15/2009	
PAGE TITLE			
NV GT216 CORE/FB POWER			
 Apple Inc.		DRAWING NUMBER	SIZE
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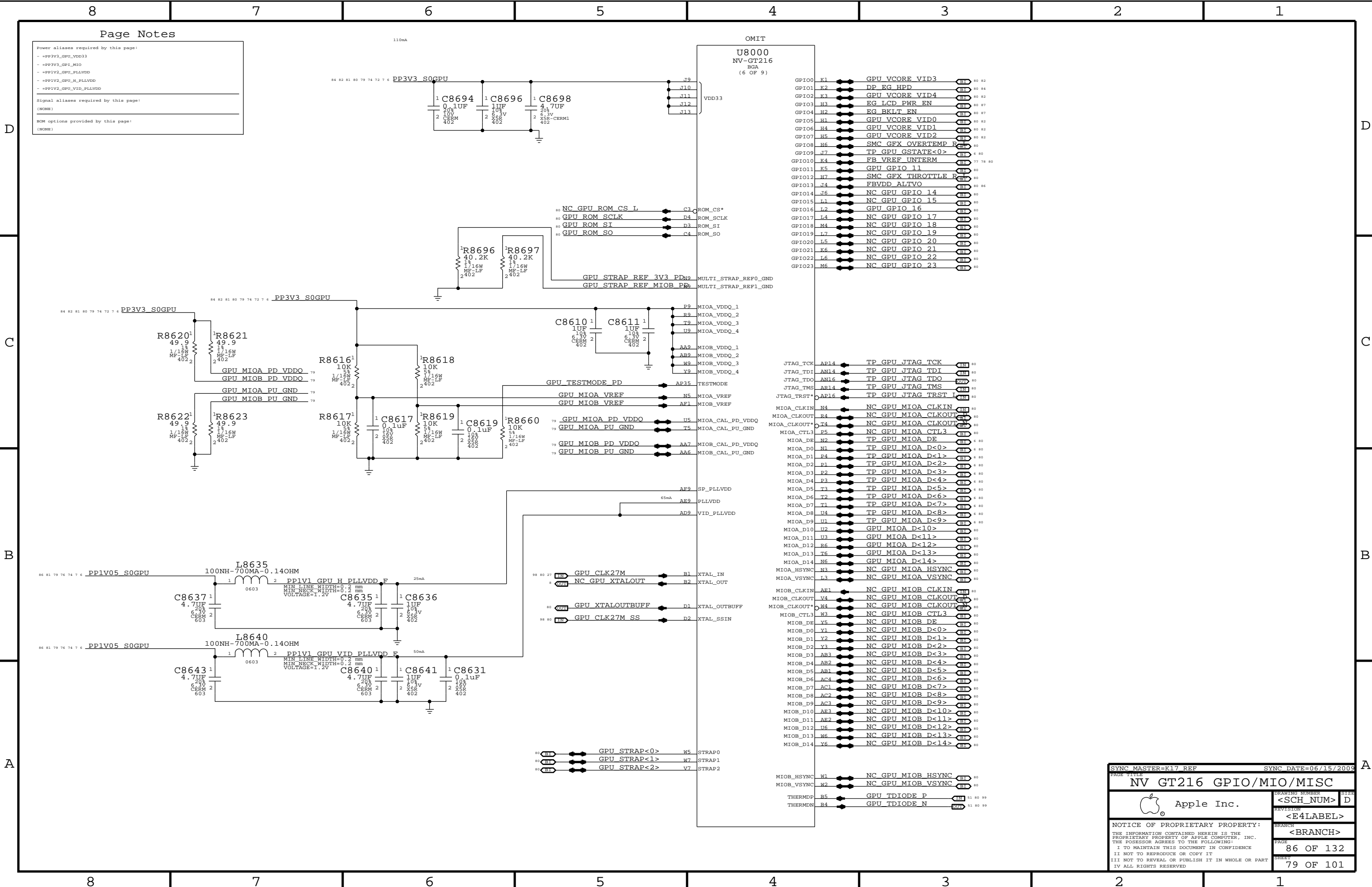












Page Notes

Power aliases required by this page:

- =PP3V3\_GPU\_VDD33
- =PP3V3\_GPU\_MIO
- =PP1V2\_GPU\_PLLVDD
- =PP1V2\_GPU\_M\_PLLVDD
- =PP1V2\_GPU\_VID\_PLLVDD

Signal aliases required by this page:


(NONE)

ROM options provided by this page:

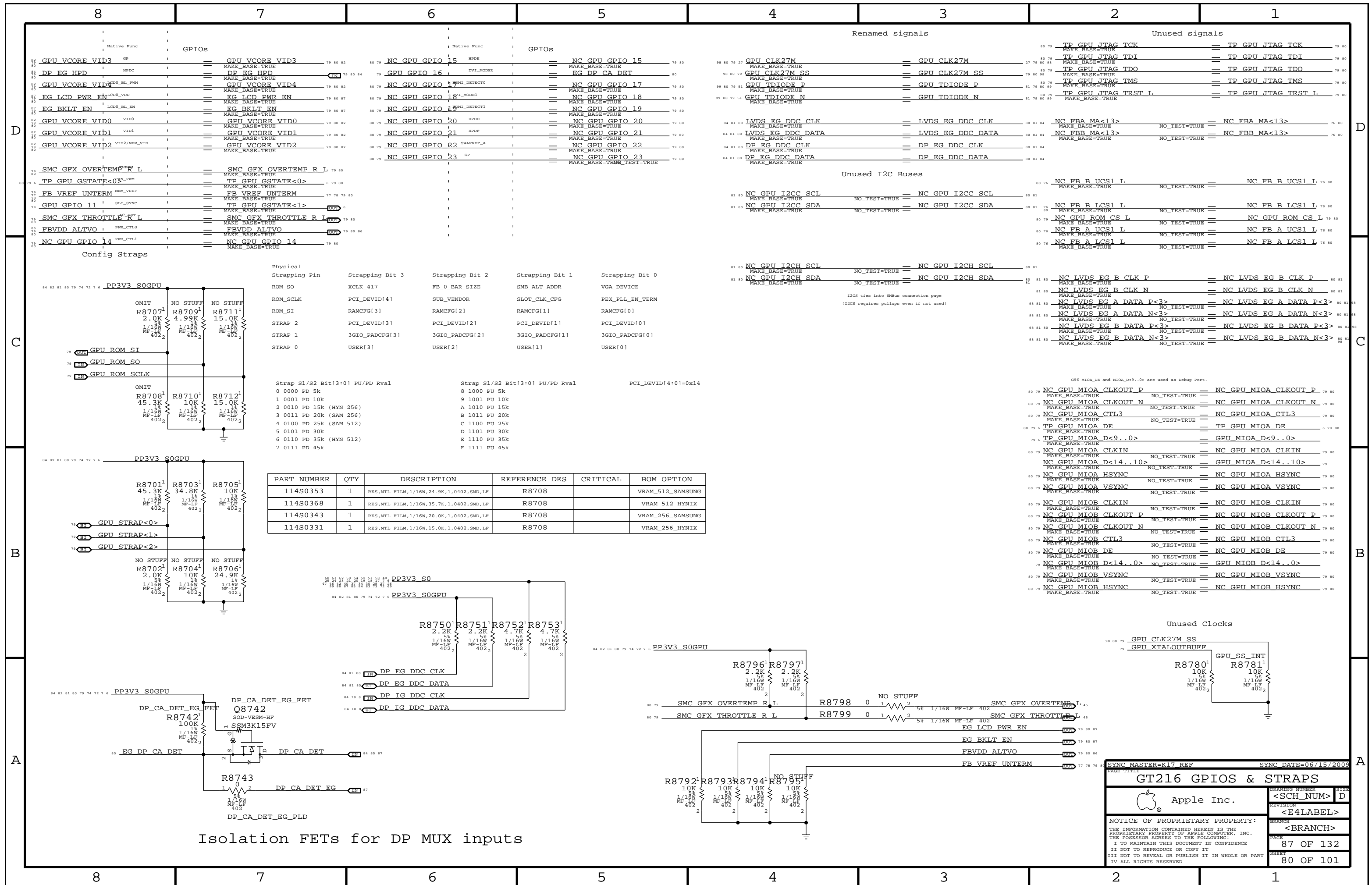
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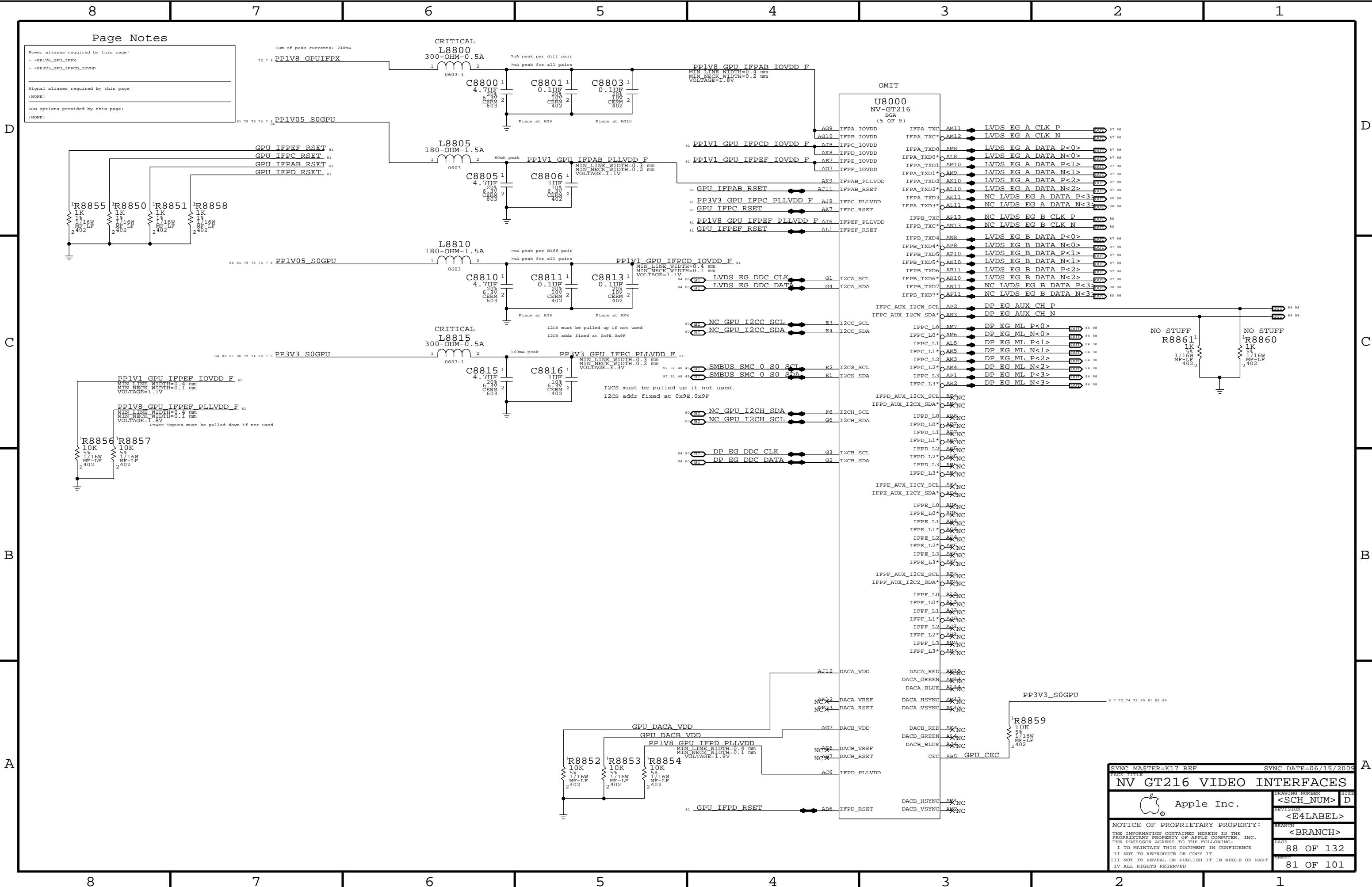
GPIO0	K1	GPU VCORE VID3	80	82
GPIO1	K2	DP EG HPD	80	84
GPIO2	K3	GPU VCORE VID4	80	82
GPIO3	H3	EG LCD PWR EN	80	87
GPIO4	H2	EG BKLT EN	80	87
GPIO5	H1	GPU VCORE VID0	80	82
GPIO6	H4	GPU VCORE VID1	80	82
GPIO7	H5	GPU VCORE VID2	80	82
GPIO8	H6	SMC GFX OVERTEMP R	80	80
GPIO9	J7	TP GPU GSTATE<0>	80	80
GPIO10	K4	FB VREF UNTERM	80	80
GPIO11	K5	GPU GPIO 11	80	80
GPIO12	H7	SMC GFX THROTTLE P	80	80
GPIO13	J4	FBVDD ALTVO	80	86
GPIO14	J6	NC GPU GPIO 14	80	80
GPIO15	L1	NC GPU GPIO 15	80	80
GPIO16	L2	GPU GPIO 16	80	80
GPIO17	L4	NC GPU GPIO 17	80	80
GPIO18	M4	NC GPU GPIO 18	80	80
GPIO19	L7	NC GPU GPIO 19	80	80
GPIO20	L5	NC GPU GPIO 20	80	80
GPIO21	K6	NC GPU GPIO 21	80	80
GPIO22	L6	NC GPU GPIO 22	80	80
GPIO23	M6	NC GPU GPIO 23	80	80

JTAG_TCK	AP14	TP GPU JTAG TCK	80	80
JTAG_TDI	AN14	TP GPU JTAG TDI	80	80
JTAG_TDO	AN16	TP GPU JTAG TDO	80	80
JTAG_TMS	AR14	TP GPU JTAG TMS	80	80
JTAG_TRST*	AP16	TP GPU JTAG TRST	80	80
MIOA_CLKIN	N4	NC GPU MIOA CLKIN	80	80
MIOA_CLKOUT	R4	NC GPU MIOA CLKOUT	80	80
MIOA_CLKOUT*	T4	NC GPU MIOA CLKOUT	80	80
MIOA_CTL3	P5	NC GPU MIOA CTL3	80	80
MIOA_DE	N2	TP GPU MIOA DE	80	80
MIOA_D0	N1	TP GPU MIOA D<0>	80	80
MIOA_D1	P4	TP GPU MIOA D<1>	80	80
MIOA_D2	P1	TP GPU MIOA D<2>	80	80
MIOA_D3	P2	TP GPU MIOA D<3>	80	80
MIOA_D4	P3	TP GPU MIOA D<4>	80	80
MIOA_D5	T3	TP GPU MIOA D<5>	80	80
MIOA_D6	T2	TP GPU MIOA D<6>	80	80
MIOA_D7	T1	TP GPU MIOA D<7>	80	80
MIOA_D8	U4	TP GPU MIOA D<8>	80	80
MIOA_D9	U1	TP GPU MIOA D<9>	80	80
MIOA_D10	U2	GPU MIOA D<10>	80	80
MIOA_D11	U3	GPU MIOA D<11>	80	80
MIOA_D12	R6	GPU MIOA D<12>	80	80
MIOA_D13	T6	GPU MIOA D<13>	80	80
MIOA_D14	N6	GPU MIOA D<14>	80	80
MIOA_HSYNC	N3	NC GPU MIOA HSYNC	80	80
MIOA_VSYNC	L3	NC GPU MIOA VSYNC	80	80
MIOB_CLKIN	AE1	NC GPU MIOB CLKIN	80	80
MIOB_CLKOUT	V4	NC GPU MIOB CLKOUT	80	80
MIOB_CLKOUT*	M4	NC GPU MIOB CLKOUT	80	80
MIOB_CTL3	M3	NC GPU MIOB CTL3	80	80
MIOB_DE	Y5	NC GPU MIOB DE	80	80
MIOB_D0	Y1	NC GPU MIOB D<0>	80	80
MIOB_D1	Y2	NC GPU MIOB D<1>	80	80
MIOB_D2	Y3	NC GPU MIOB D<2>	80	80
MIOB_D3	AB3	NC GPU MIOB D<3>	80	80
MIOB_D4	AB2	NC GPU MIOB D<4>	80	80
MIOB_D5	AB1	NC GPU MIOB D<5>	80	80
MIOB_D6	AC4	NC GPU MIOB D<6>	80	80
MIOB_D7	AC1	NC GPU MIOB D<7>	80	80
MIOB_D8	AC2	NC GPU MIOB D<8>	80	80
MIOB_D9	AC3	NC GPU MIOB D<9>	80	80
MIOB_D10	AE3	NC GPU MIOB D<10>	80	80
MIOB_D11	AE2	NC GPU MIOB D<11>	80	80
MIOB_D12	U6	NC GPU MIOB D<12>	80	80
MIOB_D13	M6	NC GPU MIOB D<13>	80	80
MIOB_D14	Y6	NC GPU MIOB D<14>	80	80

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NV GT216 GPIO/MIO/MISC			
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		REVISION	
		<E4LABEL>	
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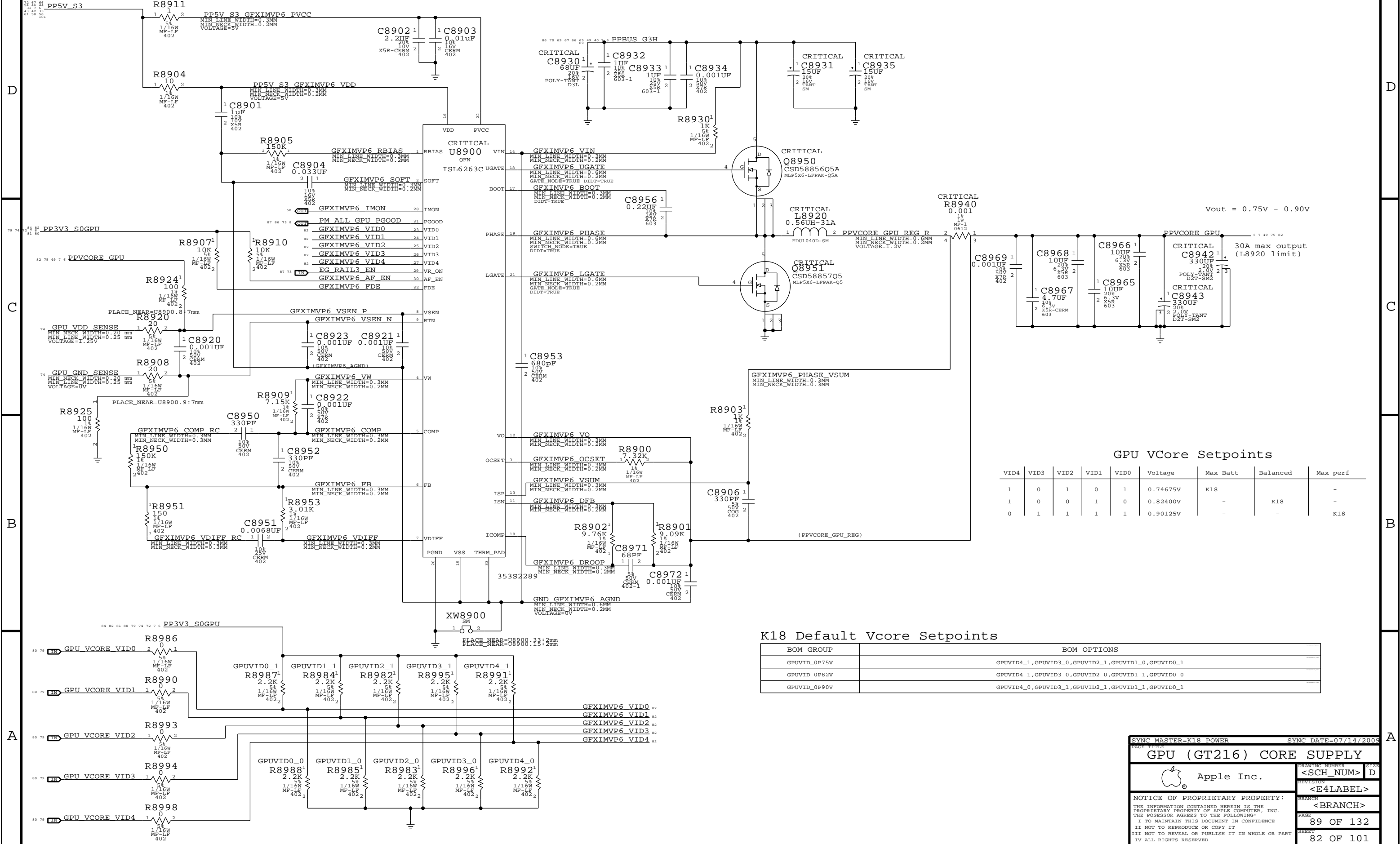








GPU VCore Regulator



D

C

B

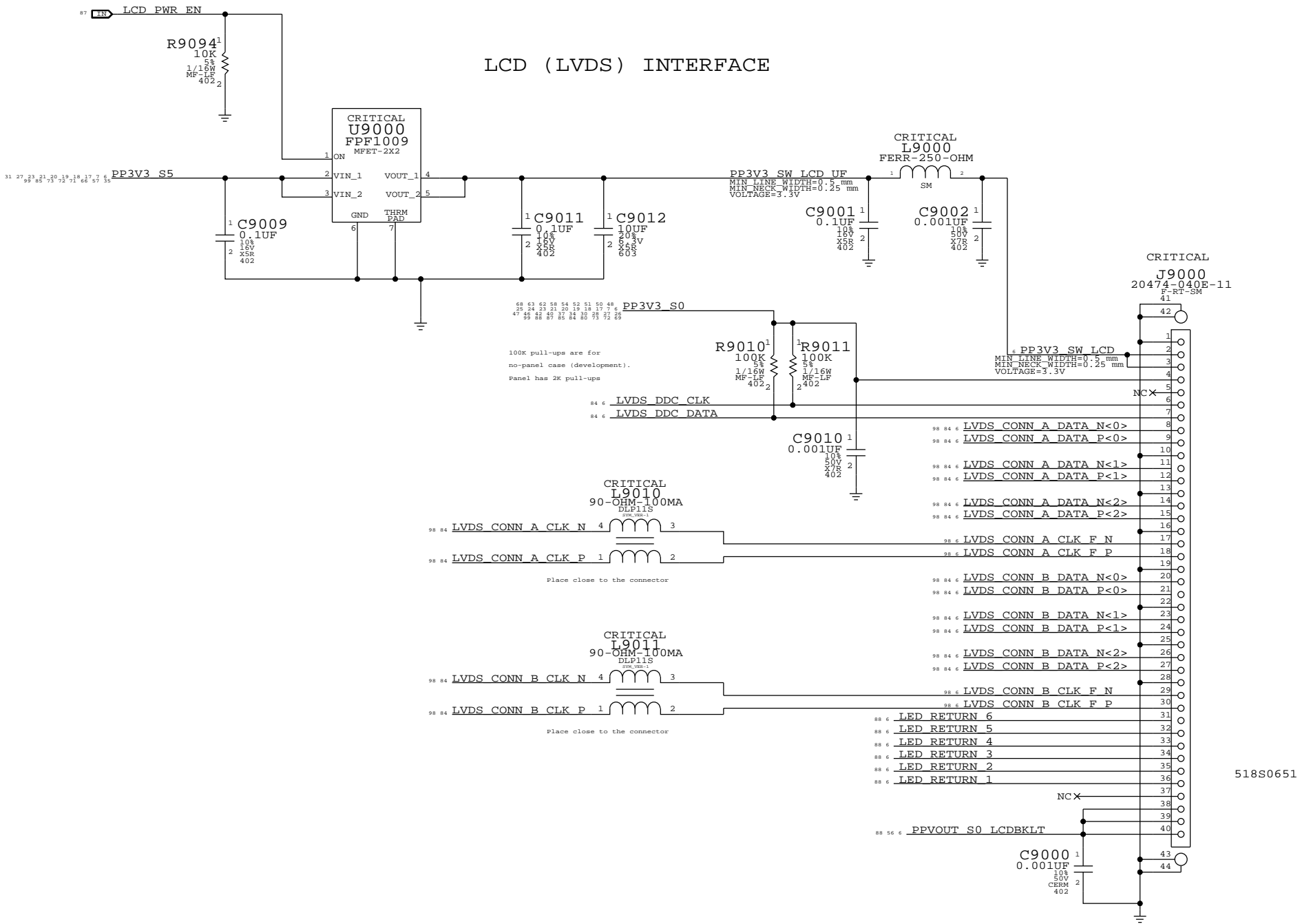
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D


C

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A



518S0651

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LVDS Display Connector				
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	REVISION		<E4LABEL>	
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PAGE		90 OF 132		
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## D

C



## D

A

# Port Power Switch

D

C

B

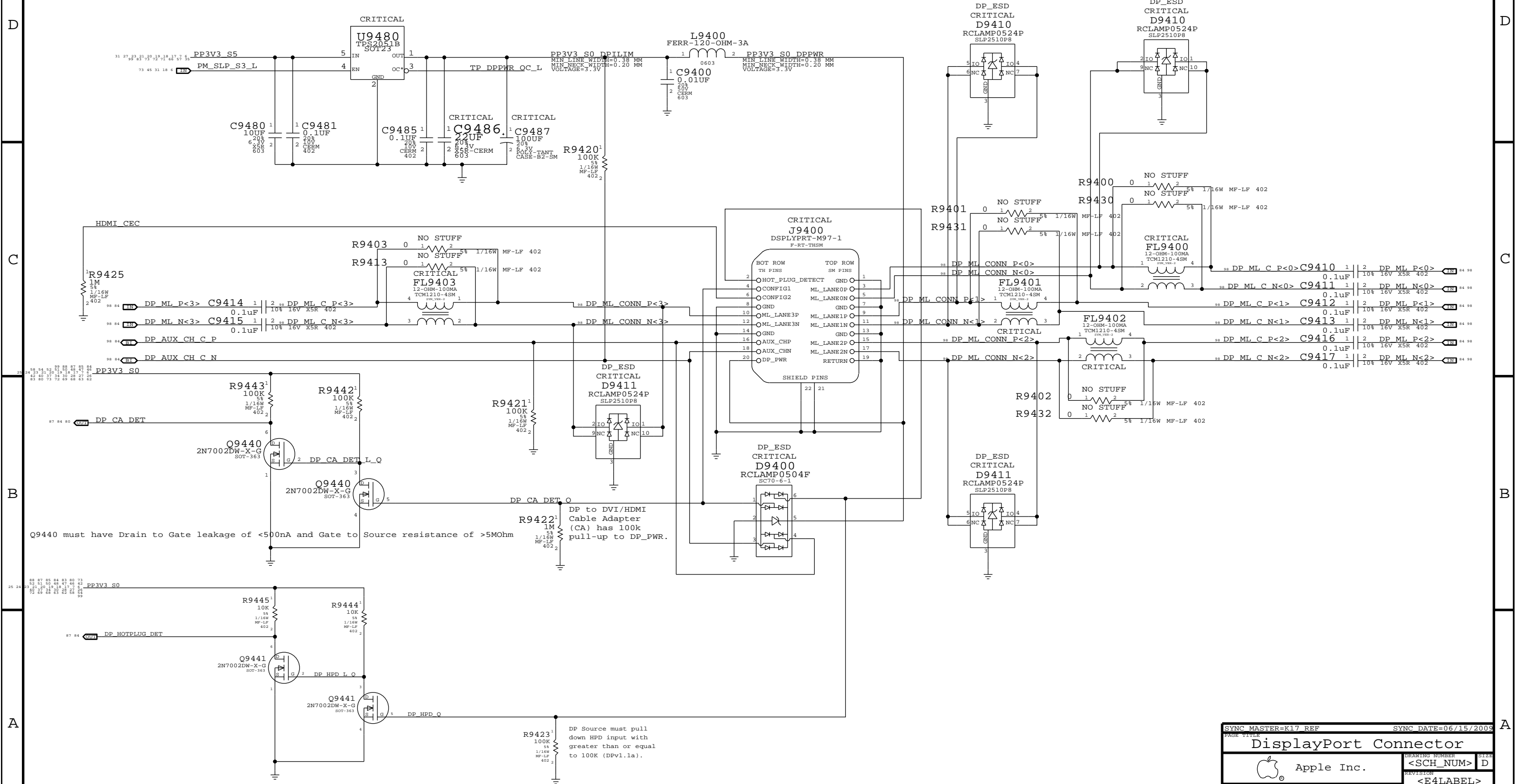
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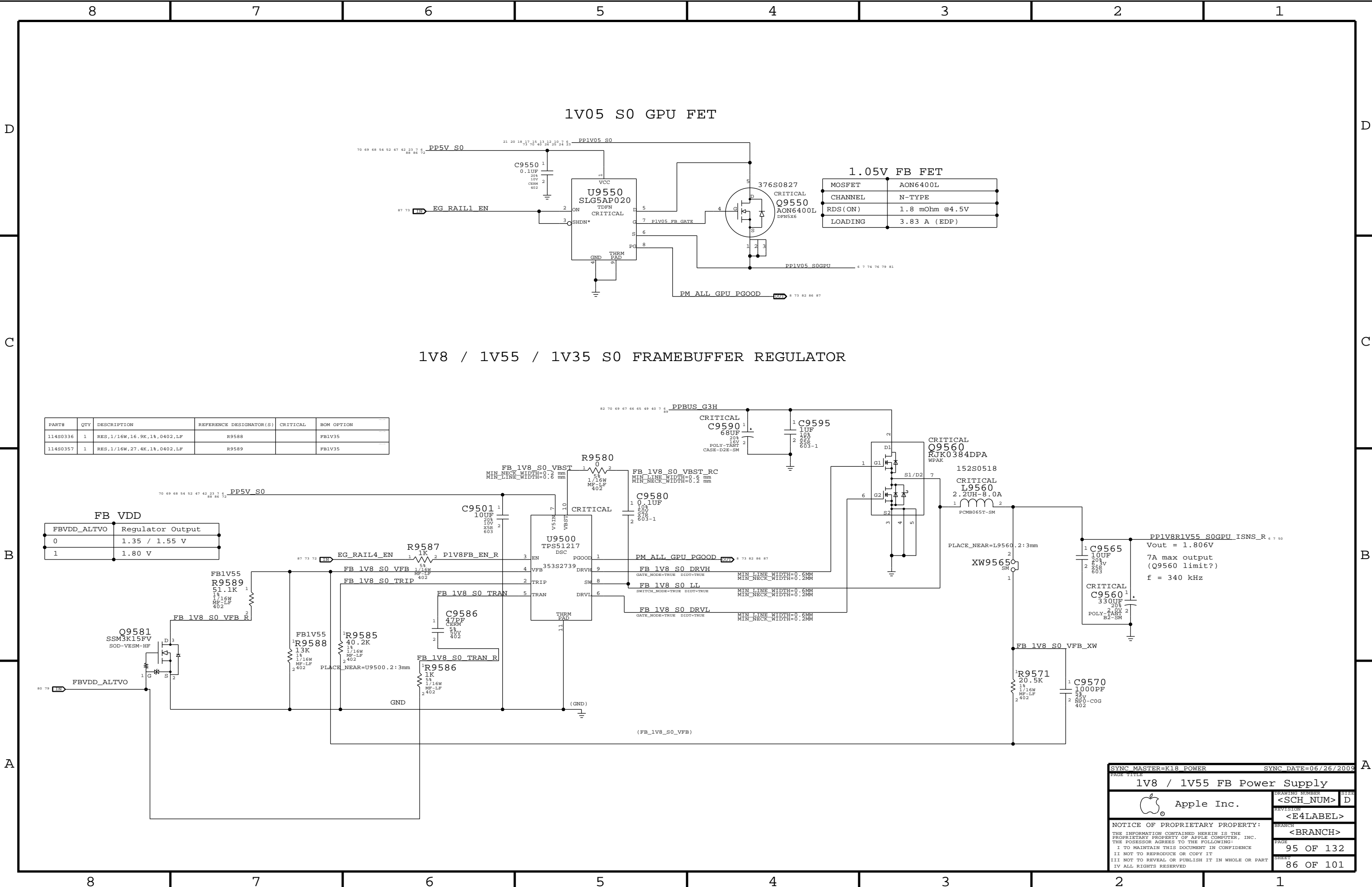
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B

A




SYNC MASTER=K17 REF		SYNC DATE=06/15/2009	
PAGE TITLE			
DisplayPort Connector			
 Apple Inc.		DRAWING NUMBER	SIZE
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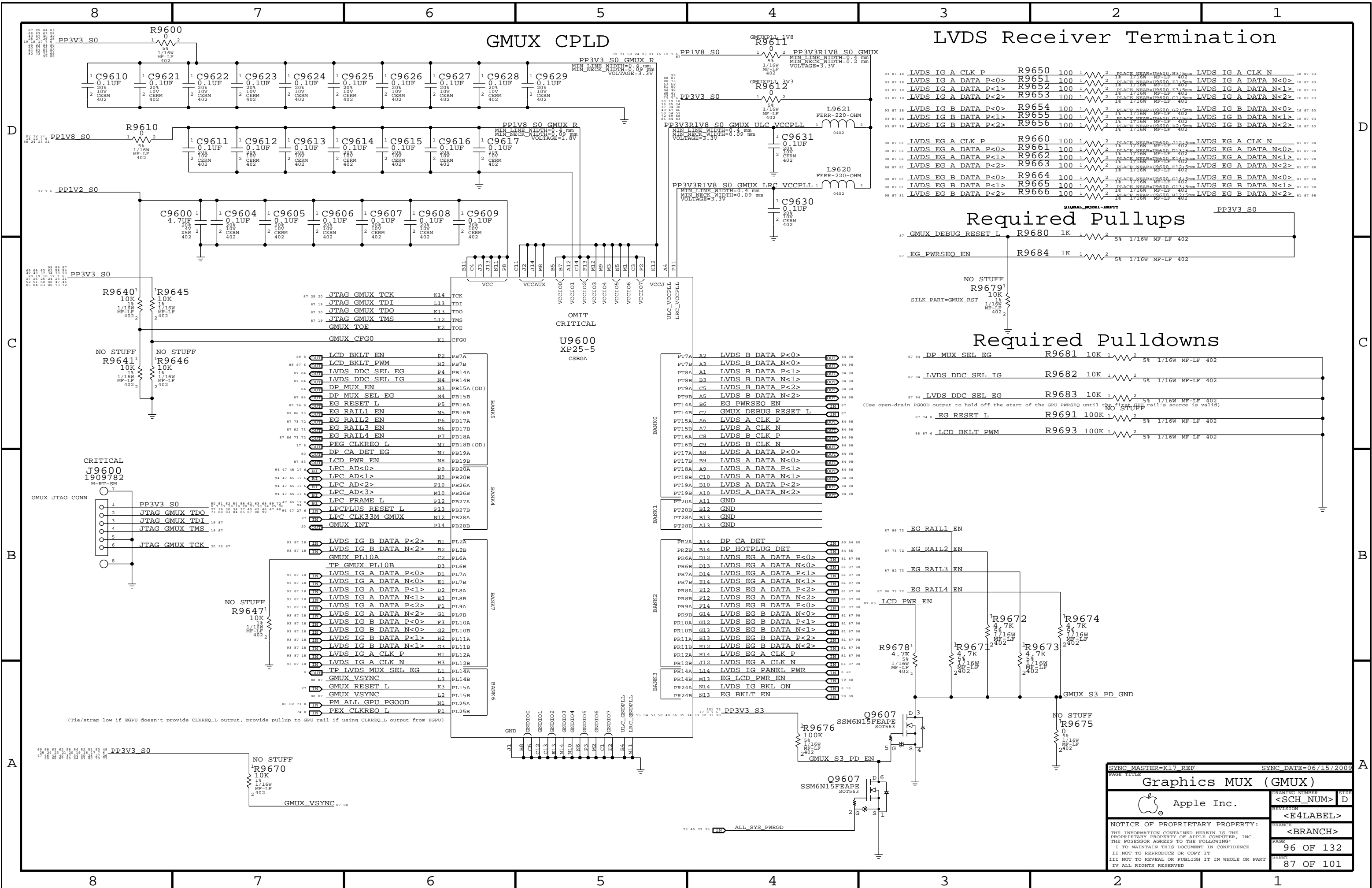


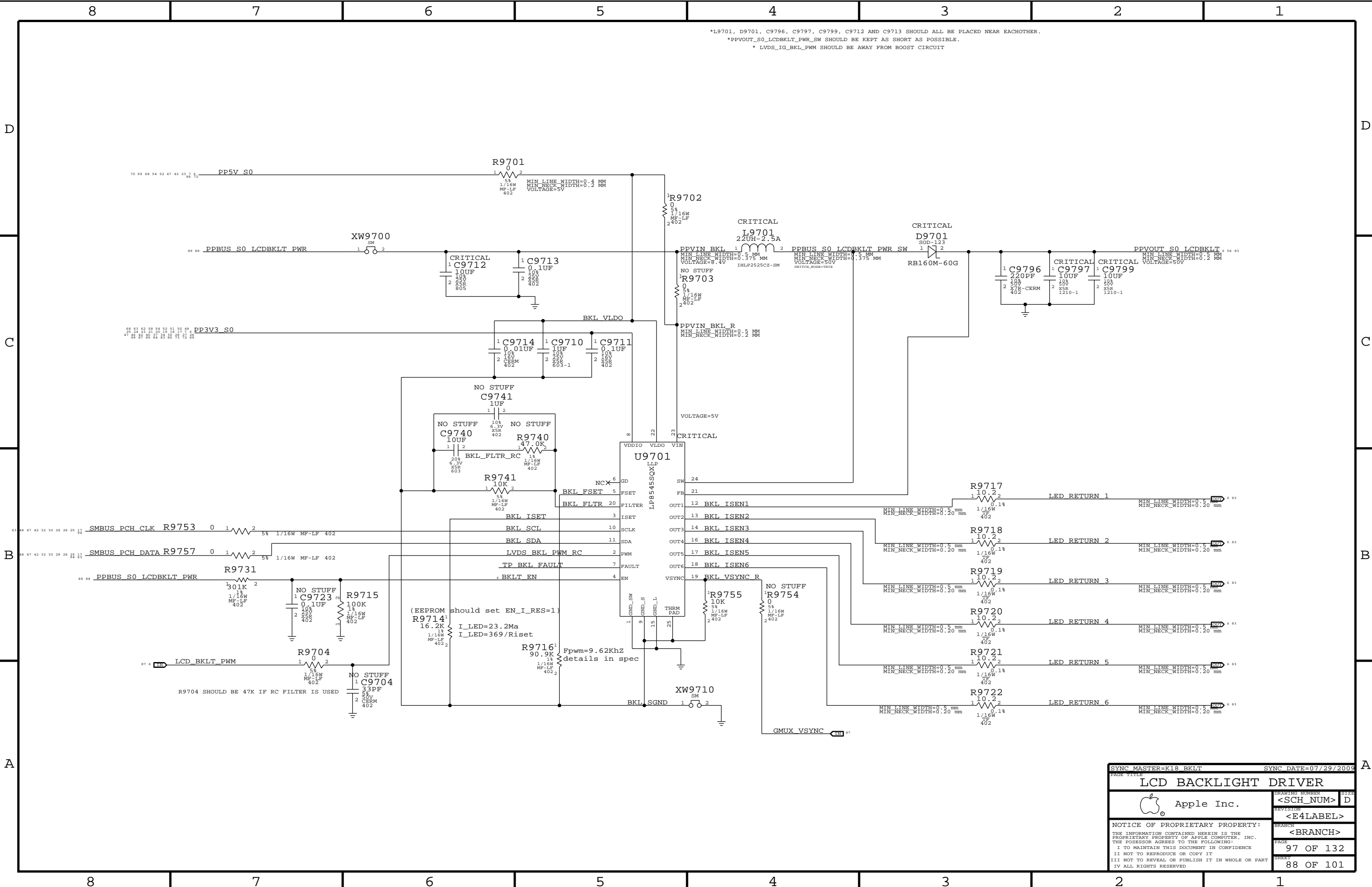
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11480336	1	RES,1/16W,16.9K,1%,0402,LF	R9588		FB1V35
11480357	1	RES,1/16W,27.4K,1%,0402,LF	R9589		FB1V35

FB VDD	
FBVDD_ALTVO	Regulator Output
0	1.35 / 1.55 V
1	1.80 V


SYNC MASTER=K18 POWER		SYNC DATE=06/26/2009	
PAGE TITLE			
1V8 / 1V55 FB Power Supply			
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		REVISION	
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		<BRANCH>	
		PAGE	95 OF 132
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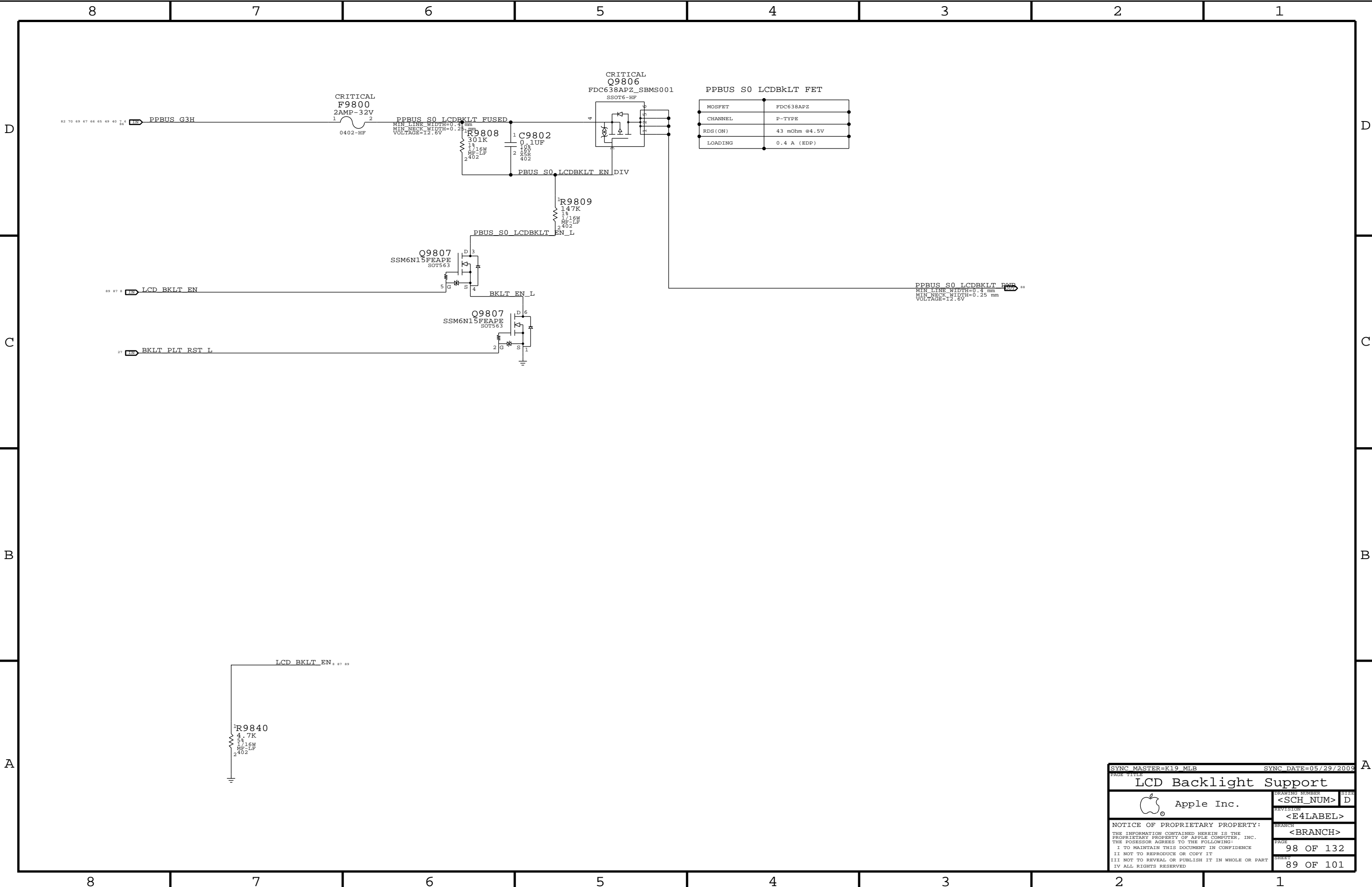






\*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.  
\*PPVOUT\_S0\_LCDBKLT\_PWR\_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.  
\* LVDS\_IG\_BKL\_PWM SHOULD BE AWAY FROM BOOST CIRCUIT


SYNC MASTER=K18 BKL		SYNC DATE=07/29/2009	
PAGE TITLE			
LCD BACKLIGHT DRIVER			
 Apple Inc.		DRAWING NUMBER	SIZE
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SYNC MASTER=K19\_MLB

SYNC DATE=05/29/2009

LCD Backlight Support

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8	7	6	5	4	3	2	1
D							D
C							C
B							B
A							A
8	7	6	5	4	3	2	1

Blank Page, was 1.2V/1.8V in K19

SYNC MASTER=K18 POWER		SYNC DATE=06/10/2009	
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Misc Power Supplies		DRAWING NUMBER	
 Apple Inc.		<SCH_NUM>	
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		<BRANCH>	
		PAGE	
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## CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364\_v1.5), Section 2.8

## PCI-Express


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_8SD	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?





























































































































































































































































SOURCE: Calpella SFF DG (DG-407364\_v1.5), Section 2.1 and Table 4-184.

## CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
DMI_S2N	PCIE_B5D	PCIE	DMI S2N P<3:0>
DMI_S2N	PCIE_B5D	PCIE	DMI S2N N<3:0>
DMI_N2S	PCIE_B5D	PCIE	DMI N2S P<3:0>
DMI_N2S	PCIE_B5D	PCIE	DMI N2S N<3:0>
FDI_DATA	PCIE_B5D	PCIE	FDI DATA P<7:0>
FDI_DATA	PCIE_B5D	PCIE	FDI DATA N<7:0>
	CPU_50S	CPU_AGTL	FDI FSYN<1..0>
	CPU_50S	CPU_AGTL	FDI_LSYN<1..0>
	CPU_50S	CPU_AGTL	FDI INT
	CPU_PECT	PCIE	CPU PEGI
FSB_CPUURST_L	CPU_50S	CPU_AGTL	FSB CPUURST L
PM_SYNC	CPU_50S	CPU_AGTL	PM SYNC
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM MEM PWRGD
CPU_VTT_S0_PGOOD	CPU_50S	CPU_AGTL	CPUVTTIS0 PGOOD
XDP_XPI_PWRGOOD	CPU_50S	CPU_ITP	XDP CPUPWRGD
XDP_DBRESET_L	CPU_50S	CPU_ITP	XDP DBRESET L
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP PRDY L
XDP_PREQ_1	CPU_50S	CPU_ITP	XDP PREQ L
	CPU_50S	CPU_AGTL	PM EXT TS L<0>
	CPU_50S	CPU_AGTL	PM EXT TS L<1>
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM RCOMP0
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM RCOMP1
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM RCOMP2
CPU_CFG	CPU_50S	CPU_ITP	CPU CFG<17..0>
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU CATERR L
	CPU_50S	CPU_AGTL	TP CPU VTT SELECT
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU PROCHOT L
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD
PM_THRMTRIP_L	CPU_50S	CPU_SMIL	PM THRMTRIP L
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB CLK133M CPU P
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB CLK133M CPU N
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB CLK133M ITP P
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB CLK133M ITP N
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M CPU P
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M CPU N
	CPU_55S	CPU_SMIL	CPU PSI_L
PM_DPRSLEVR	CPU_50S	CPU_AGTL	PM DPRSLPVR
	CPU_27P4S	CPU_COMP	CPU PEG_COMP
	CPU_27P4S	CPU_COMP	CPU PEG_RBIAS
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0
XDP_TDI	CPU_50S	CPU_ITP	XDP TDI
XDP_TDO	CPU_50S	CPU_ITP	XDP TDO
XDP_TMS	CPU_50S	CPU_ITP	XDP TMS
XDP_TCK	CPU_50S	CPU_ITP	XDP TCK
XDP_TRST_L	CPU_50S	CPU_ITP	XDP TRST L
XDP_BEM_L	CPU_50S	CPU_ITP	XDP BPM L<6..0>
XDP_BEM_L	CPU_50S	CPU_ITP	XDP BPM L<7>
(FSB_CPUURST_L)	CPU_50S	CPU_ITP	XDP CPUURST L
	CPU_55S	CPU_SMIL	CPU VID<6..0>
	CPU_50S	CPU_AGTL	CPUI MVP IMON
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VTTSENSE P
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VTTSENSE N
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX VSENSE P
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX VSENSE N
	CPU_55S	CPU_SMIL	GFX VID<6..0>
PM_DPRSLEVR	CPU_50S	CPU_AGTL	GFX DPRSLPVR
	CPU_50S	CPU_AGTL	GFX VR_EN
	CPU_50S	CPU_AGTL	GFXIMVP IMON
	PCIE_B5D	PCIE	PEG R2D P<15..0>
	PCIE_B5D	PCIE	PEG R2D N<15..0>
PEG_R2D	PCIE_B5D	PCIE	PEG R2D C P<15..0>
	PCIE_B5D	PCIE	PEG R2D C N<15..0>
PEG_D2R	PCIE_B5D	PCIE	PEG D2R P<15..0>
	PCIE_B5D	PCIE	PEG D2R N<15..0>
	PCIE_B5D	PCIE	PEG D2R C P<15..0>
	PCIE_B5D	PCIE	PEG D2R C N<15..0>

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<table><tr><th>PHYSICAL_RULE_SET</th><th>LAYER</th><th>ALLOW ROUTE ON LAYER?</th><th>MINIMUM LINE WIDTH</th><th>MINIMUM NECK WIDTH</th><th>MAXIMUM NECK LENGTH</th><th>DIFFPAIR PRIMARY GAP</th><th>DIFFPAIR NECK GAP</th></tr><tr><td>MEM_37S</td><td>*</td><td>=37_OHM_SE</td><td>=37_OHM_SE</td><td>=37_OHM_SE</td><td>=37_OHM_SE</td><td>=STANDARD</td><td>=STANDARD</td></tr><tr><td>MEM_40S</td><td>*</td><td>=40_OHM_SE</td><td>=40_OHM_SE</td><td>=40_OHM_SE</td><td>=40_OHM_SE</td><td>=STANDARD</td><td>=STANDARD</td></tr><tr><td>MEM_72D</td><td>*</td><td>=72_OHM_DIFF</td><td>=72_OHM_DIFF</td><td>=72_OHM_DIFF</td><td>=72_OHM_DIFF</td><td>=72_OHM_DIFF</td><td>=72_OHM_DIFF</td></tr><tr><td>MEM_50S</td><td>*</td><td>=50_OHM_SE</td><td>=50_OHM_SE</td><td>=50_OHM_SE</td><td>=50_OHM_SE</td><td>=STANDARD</td><td>=STANDARD</td></tr><tr><td>MEM_85D</td><td>*</td><td>=85_OHM_DIFF</td><td>=85_OHM_DIFF</td><td>=85_OHM_DIFF</td><td>=85_OHM_DIFF</td><td>=85_OHM_DIFF</td><td>=85_OHM_DIFF</td></tr></table>				PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD	MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD	MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD	MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	<table><tr><th rowspan="2">ELECTRICAL_CONSTRAINT_SET</th><th colspan="2">NET_TYPE</th><th rowspan="2"></th><th rowspan="2"></th></tr><tr><th>PHYSICAL</th><th>SPACING</th></tr><tr><td></td><td>MEM_A_CLK</td><td>MEM_72D</td><td>MEM_CLK</td><td>MEM A CLK P&lt;5..0&gt;</td><td>11 28</td></tr><tr><td></td><td>MEM_A_CLK</td><td>MEM_72D</td><td>MEM_CLK</td><td>MEM A CLK N&lt;5..0&gt;</td><td>11 28</td></tr><tr><td></td><td>MEM_A_CNTRL</td><td>MEM_37S</td><td>MEM_CTRL</td><td>MEM A CKE&lt;3..0&gt;</td><td>11 28</td></tr><tr><td></td><td>MEM_A_CNTRL</td><td>MEM_37S</td><td>MEM_CTRL</td><td>MEM A CS_L&lt;3..0&gt;</td><td>11 28</td></tr><tr><td></td><td>MEM_A_CNTRL</td><td>MEM_37S</td><td>MEM_CTRL</td><td>MEM A ODT&lt;3..0&gt;</td><td>11 28</td></tr><tr><td></td><td>MEM_A_CMD</td><td>MEM_40S</td><td>MEM_CMD</td><td>MEM A A&lt;15..0&gt;</td><td>11 28</td></tr><tr><td></td><td>MEM_A_CMD</td><td>MEM_40S</td><td>MEM_CMD</td><td>MEM A BA&lt;2..0&gt;</td><td>11 28</td></tr><tr><td></td><td>MEM_A_CMD</td><td>MEM_40S</td><td>MEM_CMD</td><td>MEM A RAS_L</td><td>11 28</td></tr><tr><td></td><td>MEM_A_CMD</td><td>MEM_40S</td><td>MEM_CMD</td><td>MEM A CAS_L</td><td>11 28</td></tr><tr><td></td><td>MEM_A_CMD</td><td>MEM_40S</td><td>MEM_CMD</td><td>MEM A WE_L</td><td>11 28</td></tr><tr><td></td><td>MEM_A_DQ_BYTE0</td><td>MEM_50S</td><td>MEM_DATA</td><td>MEM A DQ&lt;7..0&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQ_BYTE1</td><td>MEM_50S</td><td>MEM_DATA</td><td>MEM A DQ&lt;15..8&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQ_BYTE2</td><td>MEM_50S</td><td>MEM_DATA</td><td>MEM A DQ&lt;23..16&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQ_BYTE3</td><td>MEM_50S</td><td>MEM_DATA</td><td>MEM A DQ&lt;31..24&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQ_BYTE4</td><td>MEM_50S</td><td>MEM_DATA</td><td>MEM A DQ&lt;39..32&gt;</td><td>11 28 29</td></tr><tr><td></td><td>MEM_A_DQ_BYTE5</td><td>MEM_50S</td><td>MEM_DATA</td><td>MEM A DQ&lt;47..40&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQ_BYTE6</td><td>MEM_50S</td><td>MEM_DATA</td><td>MEM A DQ&lt;55..48&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQ_BYTE7</td><td>MEM_50S</td><td>MEM_DATA</td><td>MEM A DQ&lt;63..56&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQ_BYTE0</td><td>MEM_50S</td><td>MEM_DATA</td><td>MEM A DM&lt;0&gt;</td><td>11 28 29</td></tr><tr><td></td><td>MEM_A_DQ_BYTE1</td><td>MEM_50S</td><td>MEM_DATA</td><td>MEM A DM&lt;1&gt;</td><td>11 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DQS P&lt;1&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQS1</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM A DQS N&lt;1&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQS2</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM A DQS P&lt;2&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQS2</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM A DQS N&lt;2&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQS3</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM A DQS P&lt;3&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQS3</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM A DQS N&lt;3&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQS4</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM A DQS P&lt;4&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQS4</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM A DQS N&lt;4&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQS5</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM A DQS P&lt;5&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQS5</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM A DQS N&lt;5&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQS6</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM A DQS P&lt;6&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQS6</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM A DQS N&lt;6&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQS7</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM A DQS P&lt;7&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_A_DQS7</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM A DQS N&lt;7&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_B_CLK</td><td>MEM_72D</td><td>MEM_CLK</td><td>MEM B CLK P&lt;5..0&gt;</td><td>11 30</td></tr><tr><td></td><td>MEM_B_CLK</td><td>MEM_72D</td><td>MEM_CLK</td><td>MEM B CLK N&lt;5..0&gt;</td><td>11 30</td></tr><tr><td></td><td>MEM_B_CNTRL</td><td>MEM_37S</td><td>MEM_CTRL</td><td>MEM B CKE&lt;3..0&gt;</td><td>11 30</td></tr><tr><td></td><td>MEM_B_CNTRL</td><td>MEM_37S</td><td>MEM_CTRL</td><td>MEM B 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DQS N&lt;1&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_B_DQS2</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM B DQS P&lt;2&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_B_DQS2</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM B DQS N&lt;2&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_B_DQS3</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM B DQS P&lt;3&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_B_DQS3</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM B DQS N&lt;3&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_B_DQS4</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM B DQS P&lt;4&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_B_DQS4</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM B DQS N&lt;4&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_B_DQS5</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM B DQS P&lt;5&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_B_DQS5</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM B DQS N&lt;5&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_B_DQS6</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM B DQS P&lt;6&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_B_DQS6</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM B DQS N&lt;6&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_B_DQS7</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM B DQS P&lt;7&gt;</td><td>11 29</td></tr><tr><td></td><td>MEM_B_DQS7</td><td>MEM_85D</td><td>MEM_DQS</td><td>MEM B DQS N&lt;7&gt;</td><td>11 29</td></tr></table>				ELECTRICAL_CONSTRAINT_SET	NET_TYPE				PHYSICAL	SPACING		MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	11 28		MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	11 28		MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A CKE<3..0>	11 28		MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A CS_L<3..0>	11 28		MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A ODT<3..0>	11 28		MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	11 28		MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	11 28		MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS_L	11 28		MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS_L	11 28		MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE_L	11 28		MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM A DQ<7..0>	11 29		MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM A DQ<15..8>	11 29		MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM A DQ<23..16>	11 29		MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM A DQ<31..24>	11 29		MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM A DQ<39..32>	11 28 29		MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM A DQ<47..40>	11 29		MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM A DQ<55..48>	11 29		MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM A DQ<63..56>	11 29		MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM A DM<0>	11 28 29		MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM A DM<1>	11 29		MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM A DM<2>	11 29		MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM A DM<3>	11 29		MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM A DM<4>	11 29		MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM A DM<5>	11 29		MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM A DM<6>	11 29		MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM A DM<7>	11 29		MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	11 28 29		MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS N<0>	11 28 29		MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	11 29		MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<1>	11 29		MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	11 29		MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<2>	11 29		MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	11 29		MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<3>	11 29		MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	11 29		MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<4>	11 29		MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	11 29		MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<5>	11 29		MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	11 29		MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<6>	11 29		MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	11 29		MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<7>	11 29		MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	11 30		MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	11 30		MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM B CKE<3..0>	11 30		MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM B CS_L<3..0>	11 30		MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM B ODT<3..0>	11 30		MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	11 30		MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	11 30		MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS_L	11 30		MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS_L	11 30		MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE_L	11 30		MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM B DQ<7..0>	11 29		MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM B DQ<15..8>	11 29		MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM B DQ<23..16>	11 29		MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM B DQ<31..24>	11 29		MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM B DQ<39..32>	11 29 30		MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM B DQ<47..40>	11 29		MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM B DQ<55..48>	11 29		MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM B DQ<63..56>	11 29		MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM B DM<0>	11 29 30		MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM B DM<1>	11 29		MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM B DM<2>	11 29		MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM B DM<3>	11 29		MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM B DM<4>	11 29		MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM B DM<5>	11 29		MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM B DM<6>	11 29		MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM B DM<7>	11 29		MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	11 29 30		MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS N<0>	11 29 30		MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	11 29		MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<1>	11 29		MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	11 29		MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<2>	11 29		MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	11 29		MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<3>	11 29		MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	11 29		MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<4>	11 29		MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	11 29		MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<5>	11 29		MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	11 29		MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<6>	11 29		MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	11 29		MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>	11 29
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															
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DQ/DM signals should be matched within 0.508mm of associated DQS pair.																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
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## Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.  
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.  
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.  
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.  
SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Sections 2.5.3 & 2.5.4.

## SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.7.1.

## USB 2.0 Interface Constraints


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905\_v1.5), Section 3.8

## PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
DP_ML	DP_85D	DP_85D	DISPLAYPORT	DP IG ML P<3.0>
DP_ML	DP_85D	DP_85D	DISPLAYPORT	DP IG ML N<3.0>
DP_AUX_CH	DP_85D	DP_85D	DISPLAYPORT	DP IG AUX CH P
DP_AUX_CH	DP_85D	DP_85D	DISPLAYPORT	DP IG AUX CH N
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS	LVDS IG A CLK P
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS	LVDS IG A CLK N
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS	LVDS IG A DATA P<2.0>
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS	LVDS IG A DATA N<2.0>
LVDS_IG_A_DATA3	LVDS_85D	LVDS	LVDS	NC LVDS IG A DATAP<3>
LVDS_IG_A_DATA3	LVDS_85D	LVDS	LVDS	NC LVDS IG A DATAN<3>
LVDS_IG_B_CLK	LVDS_85D	LVDS	LVDS	TP LVDS IG B CLKP
LVDS_IG_B_CLK	LVDS_85D	LVDS	LVDS	TP LVDS IG B CLKN
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS	LVDS IG B DATA P<2.0>
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS	LVDS IG B DATA N<2.0>
LVDS_IG_B_DATA3	LVDS_85D	LVDS	LVDS	NC LVDS IG B DATAP<3>
LVDS_IG_B_DATA3	LVDS_85D	LVDS	LVDS	NC LVDS IG B DATAN<3>
SATA_HDD_R2D	SATA_90D	SATA	SATA	SATA HDD R2D C P
SATA_HDD_R2D	SATA_90D	SATA	SATA	SATA HDD R2D C N
SATA_HDD_R2D	SATA_90D	SATA	SATA	SATA HDD R2D P
SATA_HDD_R2D	SATA_90D	SATA	SATA	SATA HDD R2D N
SATA_HDD_D2R	SATA_90D	SATA	SATA	SATA HDD D2R P
SATA_HDD_D2R	SATA_90D	SATA	SATA	SATA HDD D2R N
SATA_HDD_D2R	SATA_90D	SATA	SATA	SATA HDD D2R C P
SATA_HDD_D2R	SATA_90D	SATA	SATA	SATA HDD D2R C N
SATA_ODD_R2D	SATA_90D	SATA	SATA	SATA ODD R2D C P
SATA_ODD_R2D	SATA_90D	SATA	SATA	SATA ODD R2D C N
SATA_ODD_R2D	SATA_90D	SATA	SATA	SATA ODD R2D P
SATA_ODD_R2D	SATA_90D	SATA	SATA	SATA ODD R2D N
SATA_ODD_D2R	SATA_90D	SATA	SATA	SATA ODD D2R P
SATA_ODD_D2R	SATA_90D	SATA	SATA	SATA ODD D2R N
SATA_ODD_D2R	SATA_90D	SATA	SATA	SATA ODD D2R C P
SATA_ODD_D2R	SATA_90D	SATA	SATA	SATA ODD D2R C N
SATA_HDD_R2D	SATA_90D	SATA	SATA	SATA HDD R2D RDRV IN P
SATA_HDD_R2D	SATA_90D	SATA	SATA	SATA HDD R2D RDRV IN N
SATA_HDD_R2D	SATA_90D	SATA	SATA	SATA HDD R2D RDRV OUT P
SATA_HDD_R2D	SATA_90D	SATA	SATA	SATA HDD R2D RDRV OUT N
SATA_HDD_D2R	SATA_90D	SATA	SATA	SATA HDD D2R RDRV IN P
SATA_HDD_D2R	SATA_90D	SATA	SATA	SATA HDD D2R RDRV IN N
SATA_HDD_D2R	SATA_90D	SATA	SATA	SATA HDD D2R RDRV OUT P
SATA_HDD_D2R	SATA_90D	SATA	SATA	SATA HDD D2R RDRV OUT N
PCH_SATA_ICOMP			SATA_ICOMP	PCH SATAICOMP
USB_HUB1_UP	USB_85D	USB	USB	USB HUB1 UP P
USB_HUB1_UP	USB_85D	USB	USB	USB HUB1 UP N
USB_HUB2_UP	USB_85D	USB	USB	USB HUB2 UP P
USB_HUB2_UP	USB_85D	USB	USB	USB HUB2 UP N
USB_EXT_A	USB_85D	USB	USB	USB EXT_A P
USB_EXT_A	USB_85D	USB	USB	USB EXT_A N
USB_EXTB	USB_85D	USB	USB	USB EXTB P
USB_EXTB	USB_85D	USB	USB	USB EXTB N
USB_EXTC	USB_85D	USB	USB	USB EXTC P
USB_EXTC	USB_85D	USB	USB	USB EXTC N
USB_EXTD	USB_85D	USB	USB	USB EXTD P
USB_EXTD	USB_85D	USB	USB	USB EXTD N
USB_MINI	USB_85D	USB	USB	USB MINI P
USB_MINI	USB_85D	USB	USB	USB MINI N
USB_WM	USB_85D	USB	USB	USB WM P
USB_WM	USB_85D	USB	USB	USB WM N
USB_CAMERA	USB_85D	USB	USB	USB CAMERA CONN P
USB_CAMERA	USB_85D	USB	USB	USB CAMERA CONN N
USB_BT	USB_85D	USB	USB	USB BT P
USB_BT	USB_85D	USB	USB	USB BT N
USB_TPAD	USB_85D	USB	USB	USB TPAD P
USB_TPAD	USB_85D	USB	USB	USB TPAD N
USB_IR	USB_85D	USB	USB	USB IR P
USB_IR	USB_85D	USB	USB	USB IR N
USB_SDCARD	USB_85D	USB	USB	USB SDCARD P
USB_SDCARD	USB_85D	USB	USB	USB SDCARD N
USB_BRCRYPT	USB_85D	USB	USB	USB BRCRYPT P
USB_BRCRYPT	USB_85D	USB	USB	USB BRCRYPT N
PCH_USB_RBIAS	PCH_USB_RBIAS			PCH USB RBIAS
PCH_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	PCIE CLK100M PCH P
PCH_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	PCIE CLK100M PCH N
PCH_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	FSB CLK133M PCH P
PCH_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	FSB CLK133M PCH N
PCH_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	PCH CLK96M DOT P
PCH_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	PCH CLK96M DOT N
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	PCH CLK100M SATA P
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	PCH CLK100M SATA N
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	PCH CLK14P3M REFCLK
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	PCH CLK133M PCIIIN
GFX_CLK_DLLSS	CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	GFX CLK120M DLLSS P
GFX_CLK_DLLSS	CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	GFX CLK120M DLLSS N

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## LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for IbeX Peak M (DG-398905-398905\_v1.5), Section 3.15

## SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

## HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for IbeX Peak M (DG-398905-398905\_v1.5), Section 3.15

## SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?


## SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

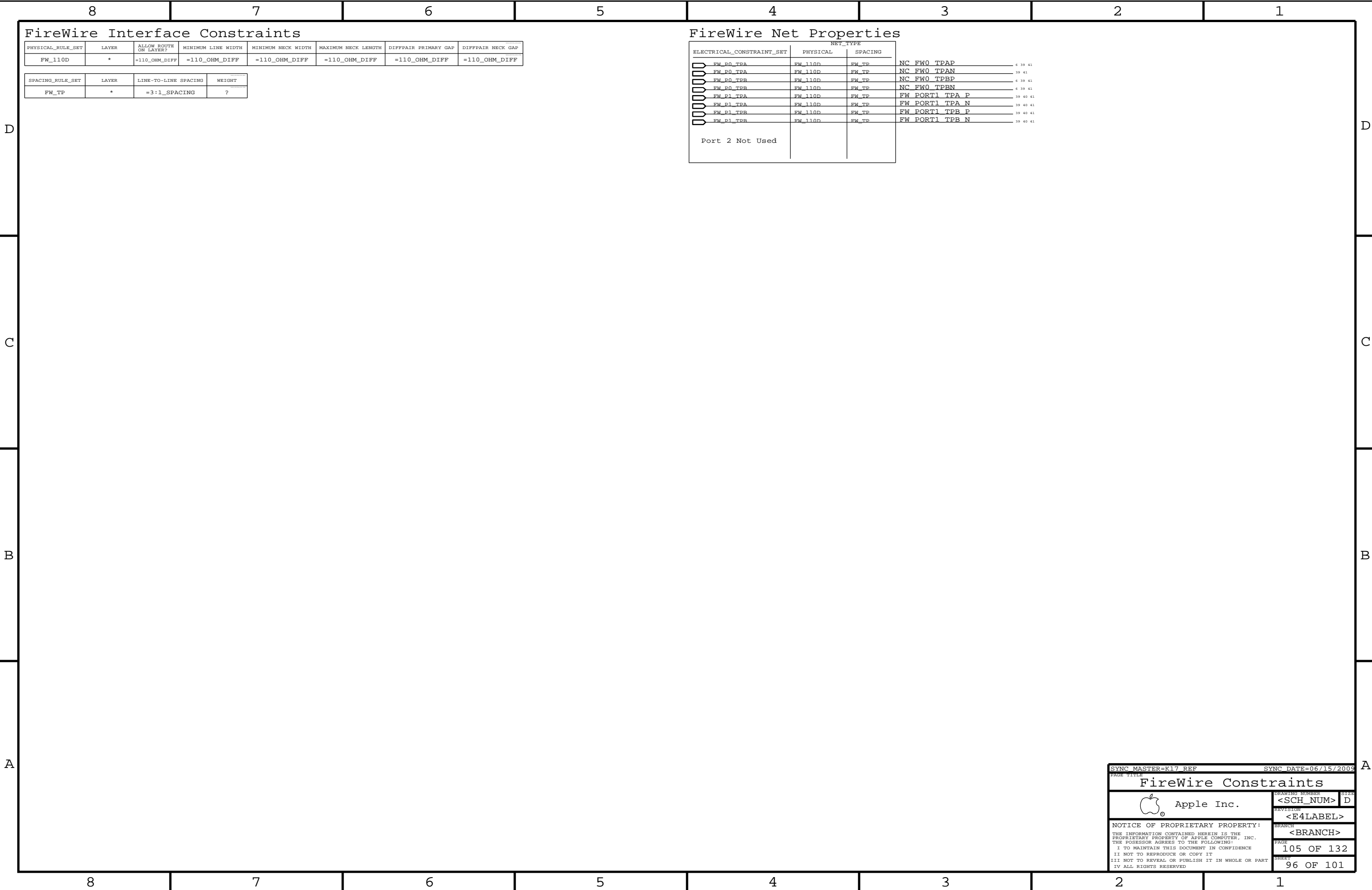
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

## PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	LPC_AD	LPC_50S	LPC	LPC_AD<3..0> 6 17 45 47 87
	LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L 6 17 45 47 87
	LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L 6 27 47 87
	MCP_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R 17 27
		CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC 27 45
		CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS 6 27 47
	SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK 17 25 26 28 30 32 42 47 48 63
	SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA 17 25 26 28 30 32 42 47 48 63
	SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK 17 48
	SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA 17 48
	SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK 17 48
	SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA 17 48
	HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK 17 58
		HDA_50S	HDA	HDA_BIT_CLK_R 17
	HDA_SYNC	HDA_50S	HDA	HDA_SYNC 17 58
		HDA_50S	HDA	HDA_SYNC_R 17
	HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L 17
		HDA_50S	HDA	HDA_RST_L 17 58
	HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0 17 58
		HDA_50S	HDA	AUD_SDI_R 58
	HDA_SDOUIT	HDA_50S	HDA	HDA_SDOUIT 17 58
		HDA_50S	HDA	HDA_SDOUIT_R 17
	PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK 18 46
	SPI_CLK	SPI_55S	SPI	SPI_CLK_R 17 47
		SPI_55S	SPI	SPI_CLK 47
	SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R 17 47
		SPI_55S	SPI	SPI_MOSI 47
	SPI_MISO	SPI_55S	SPI	SPI_MISO 17 47
	SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L 17 47
		SPI_55S	SPI	SPI_CS0_L 47
		PCIE_85D	PCIE	PCIE_ENET_R2D_P 37
		PCIE_85D	PCIE	PCIE_ENET_R2D_N 37
	PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P 17 37
		PCIE_85D	PCIE	PCIE_ENET_R2D_C_N 17 37
	PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P 17 37
		PCIE_85D	PCIE	PCIE_ENET_D2R_N 17 37
		PCIE_85D	PCIE	PCIE_ENET_D2R_C_P 37
		PCIE_85D	PCIE	PCIE_ENET_D2R_C_N 37
		PCIE_85D	PCIE	PCIE_AP_R2D_P 6 33
		PCIE_85D	PCIE	PCIE_AP_R2D_N 6 33
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P 17 33
		PCIE_85D	PCIE	PCIE_AP_R2D_C_N 17 33
	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P 6 17 33
		PCIE_85D	PCIE	PCIE_AP_D2R_N 6 17 33
		PCIE_85D	PCIE	PCIE_FW_R2D_P 39
		PCIE_85D	PCIE	PCIE_FW_R2D_N 39
	PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P 17 39
		PCIE_85D	PCIE	PCIE_FW_R2D_C_N 17 39
	PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P 17 39
		PCIE_85D	PCIE	PCIE_FW_D2R_N 17 39
		PCIE_85D	PCIE	PCIE_FW_D2R_C_P 39
		PCIE_85D	PCIE	PCIE_FW_D2R_C_N 39
	PCIE_AP_D2R	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_P
		PCIE_85D	PCIE	CONN_PCIE_AP_D2R_N
	PCIE_AP_R2D	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_P
		PCIE_85D	PCIE	CONN_PCIE_AP_R2D_N
	MCP_PE0_REFCLK	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P 17 74
		CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N 17 74
	PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P 17 37
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N 17 37
	MCP_PE1_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P 17 33
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N 17 33
	MCP_PE2_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P 17 39
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N 17 39
	MCP_PE3_REFCLK	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_P 6 17
		CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_N 6 17
FEAD		CPH_27P4S	CPH_COMP	PCH_VSS_NCTF<1> 6 20
FEAD		CPH_27P4S	CPH_COMP	PCH_VSS_NCTF<2> 6 20
FEAD		CPH_27P4S	CPH_COMP	PCH_VSS_NCTF<5> 6 20
FEAD		CPH_27P4S	CPH_COMP	TP_PCH_VSS_NCTF<7> 20
FEAD		CPH_27P4S	CPH_COMP	PCH_VSS_NCTF<9> 6 20 84
FEAD		CPH_27P4S	CPH_COMP	PCH_VSS_NCTF<9> 6 20 84
FEAD		CPH_27P4S	CPH_COMP	PCH_VSS_NCTF<11> 6 20
FEAD		CPH_27P4S	CPH_COMP	PCH_VSS_NCTF<12> 6 20
FEAD		CPH_27P4S	CPH_COMP	PCH_VSS_NCTF<15> 6 20
FEAD		CPH_27P4S	CPH_COMP	PCH_VSS_NCTF<17> 6 20
FEAD		CPH_27P4S	CPH_COMP	PCH_VSS_NCTF<19> 6 20
FEAD		CPH_27P4S	CPH_COMP	PCH_VSS_NCTF<21> 6 20
FEAD		CPH_27P4S	CPH_COMP	PCH_VSS_NCTF<22> 6 20
FEAD		CPH_27P4S	CPH_COMP	PCH_VSS_NCTF<25> 20
FEAD		CPH_27P4S	CPH_COMP	PCH_VSS_NCTF<27> 6 20
FEAD		CPH_27P4S	CPH_COMP	PCH_VSS_NCTF<29> 6 20

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## SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	CHGR_CSI	1T01_DIEFPAIR		CHGR_CSI_P
		1T01_DIEFPAIR		CHGR_CSI_N
	CHGR_CSO	1T01_DIEFPAIR		CHGR_CSO_P
		1T01_DIEFPAIR		CHGR_CSO_N

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## GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.095 MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

## Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.  
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.  
DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.  
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.  
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

## GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET		SET_TYPE		
		PHYSICAL	SPECIFIC	
	FB_A_CLK	GDDR3_80D	GDDR3_CLK	FB A CLK P<0>
		GDDR3_80D	GDDR3_CLK	FB A CLK N<0>
	FB_B_CLK	GDDR3_80D	GDDR3_CLK	FB A CLK P<1>
		GDDR3_80D	GDDR3_CLK	FB A CLK N<1>
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A MA<1..0>
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A MA<12..6>
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A BA<2..0>
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A RAS_L
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A UCAS_L
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A WE_L
	FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB A UCCKE
	FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB A LCKE
	FB_AB_CSD	GDDR3_40R55SE	GDDR3_CMD	FB A LCS0_L
	FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB A DRAM_RST
	FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB A LMA<5..2>
	FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB A UMA<5..2>
	FB_A_WDOS0	GDDR3_40SE	GDDR3_DQS	FB A WDOS<0>
	FB_A_WDOS1	GDDR3_40SE	GDDR3_DQS	FB A WDOS<1>
	FB_A_WDOS2	GDDR3_40SE	GDDR3_DQS	FB A WDOS<2>
	FB_A_WDOS3	GDDR3_40SE	GDDR3_DQS	FB A WDOS<3>
	FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB A RDOS<0>
	FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB A RDOS<1>
	FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB A RDOS<2>
	FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB A RDOS<3>
	FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB A DQ<7..0>
	FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB A DQ<15..8>
	FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB A DQ<23..16>
	FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB A DQ<31..24>
	FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB A DQM_L<0>
	FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB A DQM_L<1>
	FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB A DQM_L<2>
	FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB A DQM_L<3>
	FB_B_WDOS0	GDDR3_40SE	GDDR3_DQS	FB A WDOS<4>
	FB_B_WDOS1	GDDR3_40SE	GDDR3_DQS	FB A WDOS<5>
	FB_B_WDOS2	GDDR3_40SE	GDDR3_DQS	FB A WDOS<6>
	FB_B_WDOS3	GDDR3_40SE	GDDR3_DQS	FB A WDOS<7>
	FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB A RDOS<4>
	FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB A RDOS<5>
	FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB A RDOS<6>
	FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB A RDOS<7>
	FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB A DQ<39..32>
	FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB A DQ<47..40>
	FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB A DQ<55..48>
	FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB A DQ<63..56>
	FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB A DQM_L<4>
	FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB A DQM_L<5>
	FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB A DQM_L<6>
	FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB A DQM_L<7>

### GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET		SET_TYPE		
		PHYSICAL	SPACING	
	FB_C_CLK	GDDR3_80N	GDDR3_CLK	FB B CLK P<0>
		GDDR3_80D	GDDR3_CLK	FB B CLK N<0>
	FB_D_CLK	GDDR3_80D	GDDR3_CLK	FB B CLK P<1>
		GDDR3_80D	GDDR3_CLK	FB B CLK N<1>
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B MA<1..0>
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B MA<12..6>
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B BA<2..0>
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B RAS L
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B UCAS L
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B WE L
	FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB B UCKE
	FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB B LCKE
FB	FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB B LCS0 L
	FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB B DRAM_RST
	FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB B LMA<5..2>
	FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB B UMA<5..2>
	FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB B WDQS<0>
	FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB B WDQS<1>
	FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB B WDQS<2>
	FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB B WDQS<3>
	FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB B RDQS<0>
	FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB B RDQS<1>
	FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB B RDQS<2>
	FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB B RDQS<3>
	FB_C_DQ_RVTE0	GDDR3_40SE	GDDR3_DATA	FB B DQ<7..0>
	FB_C_DQ_RVTE1	GDDR3_40SE	GDDR3_DATA	FB B DQ<15..8>
	FB_C_DQ_RVTE2	GDDR3_40SE	GDDR3_DATA	FB B DQ<23..16>
	FB_C_DQ_RVTE3	GDDR3_40SE	GDDR3_DATA	FB B DQ<31..24>
	FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB B DOM L<0>
	FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB B DOM L<1>
	FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB B DOM L<2>
	FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB B DOM L<3>
	FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB B WDQS<4>
	FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB B WDQS<5>
	FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB B WDQS<6>
	FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB B WDQS<7>
	FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB B RDQS<4>
	FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB B RDQS<5>
	FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB B RDQS<6>
	FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB B RDQS<7>
	FB_D_DQ_RVTE0	GDDR3_40SE	GDDR3_DATA	FB B DQ<39..32>
	FB_D_DQ_RVTE1	GDDR3_40SE	GDDR3_DATA	FB B DQ<47..40>
	FB_D_DQ_RVTE2	GDDR3_40SE	GDDR3_DATA	FB B DQ<55..48>
	FB_D_DQ_RVTE3	GDDR3_40SE	GDDR3_DATA	FB B DQ<63..56>
	FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB B DOM L<4>
	FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB B DOM L<5>
	FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB B DOM L<6>
	FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB B DOM L<7>
FB	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A LCAS L
FB	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B LCAS L

## MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET		SET_TYPE		
	PHYSICAL		FUNCTION	
R000	LVDS_A_CLK	LVDS_85D	LVDS	LVDS A CLK P 84 87
R001	LVDS_A_CLK	LVDS_85D	LVDS	LVDS A CLK N 84 87
R002	LVDS_A_DATA	LVDS_85D	LVDS	LVDS A DATA P<2..0> 84 87
R003	LVDS_A_DATA	LVDS_85D	LVDS	LVDS A DATA N<2..0> 84 87
R004	LVDS_B_CLK	LVDS_85D	LVDS	LVDS B CLK P 84 87
R005	LVDS_B_CLK	LVDS_85D	LVDS	LVDS B CLK N 84 87
R006	LVDS_B_DATA	LVDS_85D	LVDS	LVDS B DATA P<2..0> 84 87
R007	LVDS_B_DATA	LVDS_85D	LVDS	LVDS B DATA N<2..0> 84 87
R008	LVDS_85D	LVDS_85D	LVDS	LVDS CONN A CLK F P 6 83
R009	LVDS_85D	LVDS_85D	LVDS	LVDS CONN A CLK F N 6 83
R010	LVDS_85D	LVDS_85D	LVDS	LVDS CONN B CLK F P 6 83
R011	LVDS_85D	LVDS_85D	LVDS	LVDS CONN B CLK F N 6 83
R012	LVDS_85D	LVDS_85D	LVDS	LVDS CONN A CLK P 83 84
R013	LVDS_85D	LVDS_85D	LVDS	LVDS CONN A CLK N 83 84
R014	LVDS_85D	LVDS_85D	LVDS	LVDS CONN A DATA P<2..0> 6 83 84
R015	LVDS_85D	LVDS_85D	LVDS	LVDS CONN A DATA N<2..0> 6 83 84
R016	LVDS_85D	LVDS_85D	LVDS	LVDS CONN B CLK P 83 84
R017	LVDS_85D	LVDS_85D	LVDS	LVDS CONN B CLK N 83 84
R018	LVDS_85D	LVDS_85D	LVDS	LVDS CONN B DATA P<2..0> 6 83 84
R019	LVDS_85D	LVDS_85D	LVDS	LVDS CONN B DATA N<2..0> 6 83 84
R020	DP_ML	DP_85D	DISPLAYPORT	DP ML C P<3..0> 85
R021		DP_85D	DISPLAYPORT	DP ML C N<3..0> 85
R022	DP_ML	DP_85D	DISPLAYPORT	DP ML P<3..0> 84 85
R023		DP_85D	DISPLAYPORT	DP ML N<3..0> 85
R024	DP_ML	DP_85D	DISPLAYPORT	DP ML CONN P<3..0> 84 85
R025		DP_85D	DISPLAYPORT	DP ML CONN N<3..0> 85
R026	DP_AUX_CH	DP_85D	DISPLAYPORT	DP AUX CH C P 84 85
R027	DP_AUX_CH	DP_85D	DISPLAYPORT	DP AUX CH C N 84 85

## G96 Net Properties

ELECTRICAL_CONSTRAINT_SET		SET_TYPE		
		PHYSICAL	SPACING	
	(CKLDS_POWER)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M
	CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS
	LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS EG A CLK P
	LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS EG A CLK N
	LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS EG A DATA P<2..0>
	LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS EG A DATA N<2..0>
EP200	LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC LVDS EG A DATA P<3>
EP200	LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC LVDS EG A DATA N<3>
	LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS EG B DATA P<2..0>
	LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS EG B DATA N<2..0>
EP200	LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC LVDS EG B DATA P<3>
EP200	LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC LVDS EG B DATA N<3>
EP200	DP_ML	DP_85D	DISPLAYPORT	DP EG ML P<3..0>
EP200	DP_ML	DP_85D	DISPLAYPORT	DP EG ML N<3..0>
EP200	DP_AUX_CH	DP_85D	DISPLAYPORT	DP EG AUX CH P
EP200	DP_AUX_CH	DP_85D	DISPLAYPORT	DP EG AUX CH N
EP200		DP_85D	DISPLAYPORT	DP EG AUX CH C P
EP200		DP_85D	DISPLAYPORT	DP EG AUX CH C N

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_I101_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_I101_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	= STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCI_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

## Graphics , SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE9_90D	BGA	100_DIFF_BGA

## Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

## K18 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
		ENET 100D	ENETCONN	ENETCONN P<3...0>
		ENET 100D	ENETCONN	ENETCONN N<3...0>
		SATA_90D	SATA	SATA ODD R2D UF P
		SATA_90D	SATA	SATA ODD R2D UF N
		SATA_90D	SATA	SATA ODD D2R UF P
		SATA_90D	SATA	SATA ODD D2R UF N
		SATA_90D	SATA	SATA HDD D2R UF P
		SATA_90D	SATA	SATA HDD D2R UF N
		SATA_90D	SATA	SATA HDD R2D UF P
		SATA_90D	SATA	SATA HDD R2D UF N
	SENSE DIFFPAIR	THERM 170J 55G	THERM	CPUTHMSNS D2 P
	SENSE DIFFPAIR	THERM 170J 55G	THERM	CPUTHMSNS D2 N
R28	SENSE DIFFPAIR	THERM 170J 55G	THERM	CPU THERMD P
R28	SENSE DIFFPAIR	THERM 170J 55G	THERM	CPU THERMD N
	SENSE DIFFPAIR	THERM 170J 55G	THERM	GPUTHMSNS D P
	SENSE DIFFPAIR	THERM 170J 55G	THERM	GPUTHMSNS D N
	SENSE DIFFPAIR	THERM 170J 55G	THERM	GPU TDIODE P
	SENSE DIFFPAIR	THERM 170J 55G	THERM	GPU TDIODE N
	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	CPUVTTISNS R N
		SENSE 170J 55G	SENSE	CPUVTTISNS R P
	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	CPUVITS0 CS N
		SENSE 170J 55G	SENSE	CPUVITS0 CS P
	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	DDRISNS R N
		SENSE 170J 55G	SENSE	DDRISNS R P
	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	GFXIMVP CS N
		SENSE 170J 55G	SENSE	GFXIMVP CS P
	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	GFXIMVP CS R N
		SENSE 170J 55G	SENSE	GFXIMVP CS R P
	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	GPX ISNS R N
		SENSE 170J 55G	SENSE	GPX ISNS R P
	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	GPUISNS N
		SENSE 170J 55G	SENSE	GPUISNS P
	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS 1V5 S3 N
		SENSE 170J 55G	SENSE	ISNS 1V5 S3 P
	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS AIRPORT N
		SENSE 170J 55G	SENSE	ISNS AIRPORT P
R41	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS AIRPORT P
R49	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS AIRPORT R N
R49	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS AIRPORT R P
R49	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS CPU N
R49	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS CPU P
R49	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS HDD N
R49	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS HDD P
R49	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS HDD R N
R49	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS HDD R P
R49	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS LCDBLKT N
R49	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS LCDBLKT P
R49	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS ODD N
R49	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS ODD P
	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS ODD R N
		SENSE 170J 55G	SENSE	ISNS ODD R P
	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS P1V8GPU N
		SENSE 170J 55G	SENSE	ISNS P1V8GPU P
R49	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS P1V8GPU R N
R49	SENSE DIFFPAIR	SENSE 170J 55G	SENSE	ISNS P1V8GPU R P

## K18 Specific Net Properties


ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	
PCIE CLK100M AP	CLK PCIE 90D	CLK PCIE	PCIE CLK100M AP CONN P 6 33
	CLK PCIE 90D	CLK PCIE	PCIE CLK100M AP CONN N 6 33
	1T01_DIEFFPAIR		CHGR CSI R P 65
	1T01_DIEFFPAIR		CHGR CSI R N 65
	1T01_DIEFFPAIR		CHGR CSO R P 49 65
	1T01_DIEFFPAIR		CHGR CSO R N 49 65
(USB_EXTA)	USB_85D	USB	USB2 EXTA MIXED P 43
(USB_EXTA)	USB_85D	USB	USB2 EXTA MIXED N 43
(USB_EXTA)	USB_85D	USB	USB2 LT1 P 6 43
(USB_EXTA)	USB_85D	USB	USB2 LT1 N 6 43
	USB_85D	USB	CONN USB2_BT P 6 33
	USB_85D	USB	CONN USB2_BT N 6 33
	USB_85D	USB	USB LT2 P 6 43
	USB_85D	USB	USB LT2 N 6 43
	DP_85D	DISPLAYPORT	DP IG AUX CH C P 84
	DP_85D	DISPLAYPORT	DP IG AUX CH C N 84
SPK_OUT	DIEFFPAIR	AUDIO	SPKRCONN L OUT P 6 61 62
	DIEFFPAIR	AUDIO	SPKRCONN L OUT N 6 61 62
SPK_OUT	DIEFFPAIR	AUDIO	SPKRCONN R OUT P 6 61 62
	DIEFFPAIR	AUDIO	SPKRCONN R OUT N 6 61 62
SPK_OUT	DIEFFPAIR	AUDIO	SPKRCONN S OUT P 6 61 62
	DIEFFPAIR	AUDIO	SPKRCONN S OUT N 6 61 62
	USB_85D	USB	USB TPAD R P 63
	USB_85D	USB	USB TPAD R N 63
	SR_POWER		PP3V3 S5 6 7 17 18 19 20 21 23 27 31 38 57 62 71 72 73 75 85 86 50 51 52
	SR_POWER		PP3V3 S0 6 7 17 18 19 20 21 23 24 25 26 27 28 30 34 37 40 42 46 47 48 53 54 55 56 57 58 59 60 61 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99
	SR_POWER		PP1V5 S3RS0 6 7 13 16 31 42 72 73 63 68 87
	GND		GND

8	7	6	5	4	3	2	1
K18 Board-Specific Spacing & Physical Constraints							
BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA		MM	15.5.1
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL9, ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL9, ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9, ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DEFAULT	*	0.1 MM	?	*	*	BGA	BGA_P1MM
STANDARD	*	=DEFAULT	?	MEM_CLK	*	BGA	BGA_P2MM
BGA_P1MM	*	=DEFAULT	?	CLK_PCIE	*	BGA	BGA_P2MM
BGA_P2MM	*	=DEFAULT	?	CLK_SLOW	*	BGA	BGA_P2MM
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?	2X_DIELECTRIC	*	0.140 MM	?
2:1_SPACING	*	0.2 MM	?	3X_DIELECTRIC	*	0.210 MM	?
2.5:1_SPACING	*	0.25 MM	?	4X_DIELECTRIC	*	0.280 MM	?
3:1_SPACING	*	0.3 MM	?				
4:1_SPACING	*	0.4 MM	?				
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_DIFF	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_DIFF	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_DIFF	TOP, BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.							
8	7	6	5	4	3	2	1

SYNC MASTER=K17\_REF

SYNC DATE=06/15/2009

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