

D

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B

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7918	1	SCREEN,MLB,N97A	SCN	CRITICAL	
820-2327	1	PCBF,MLB,N97	PCB	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7918	1	SCREEN,MLB,N97A	SCN	CRITICAL	
820-2327	1	PCBF,MLB,N97	PCB	CRITICAL	



1

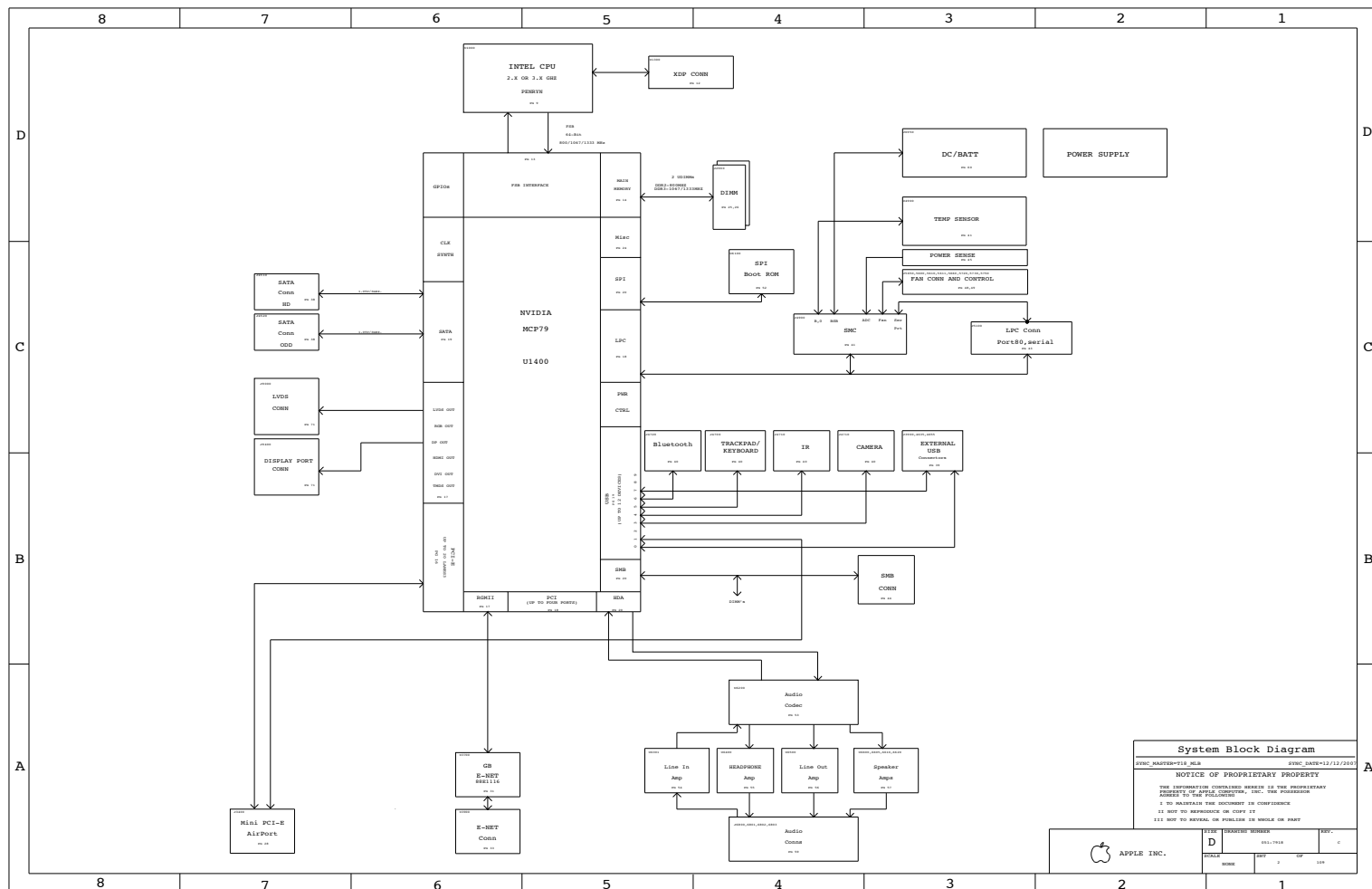
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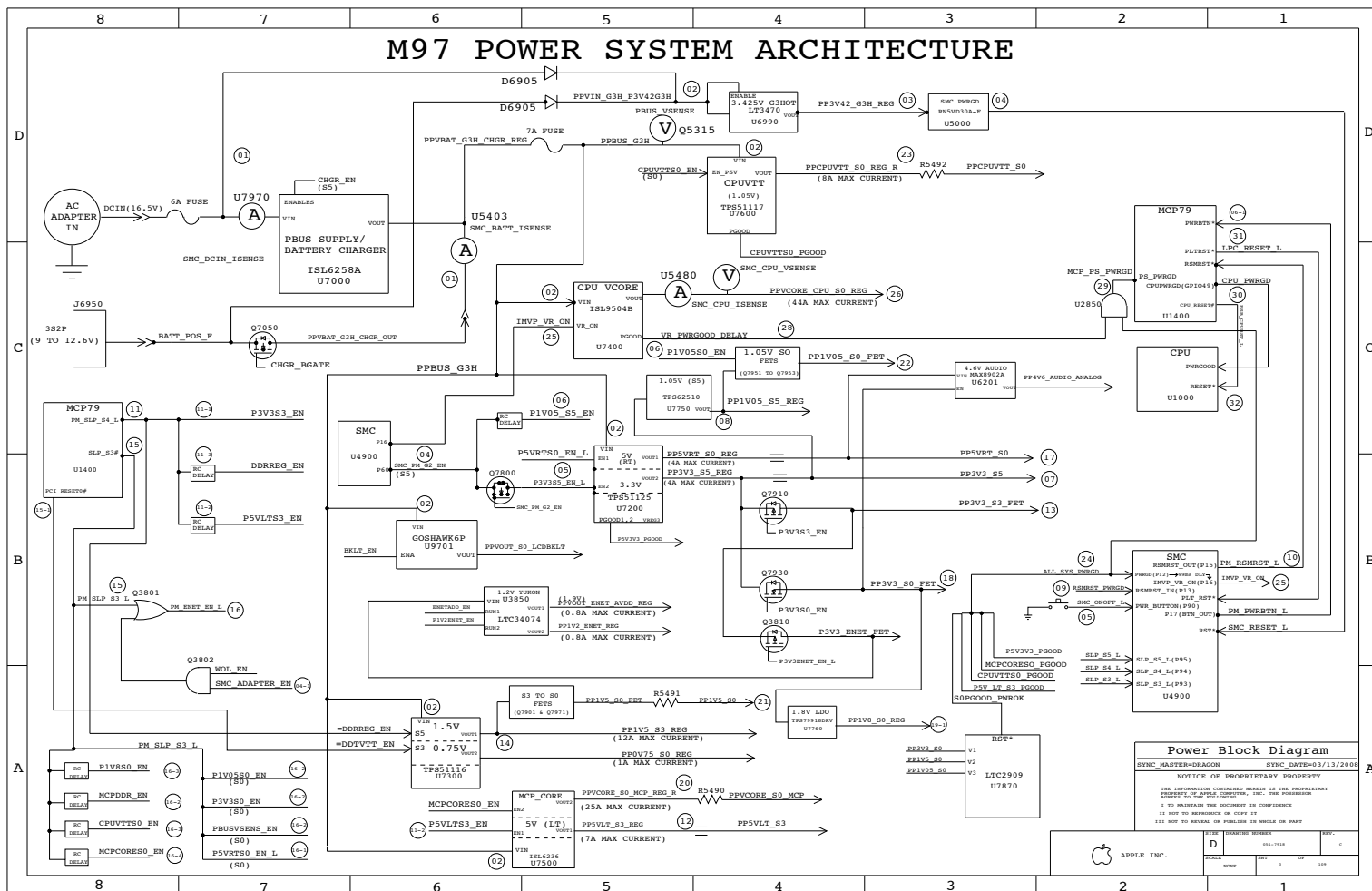
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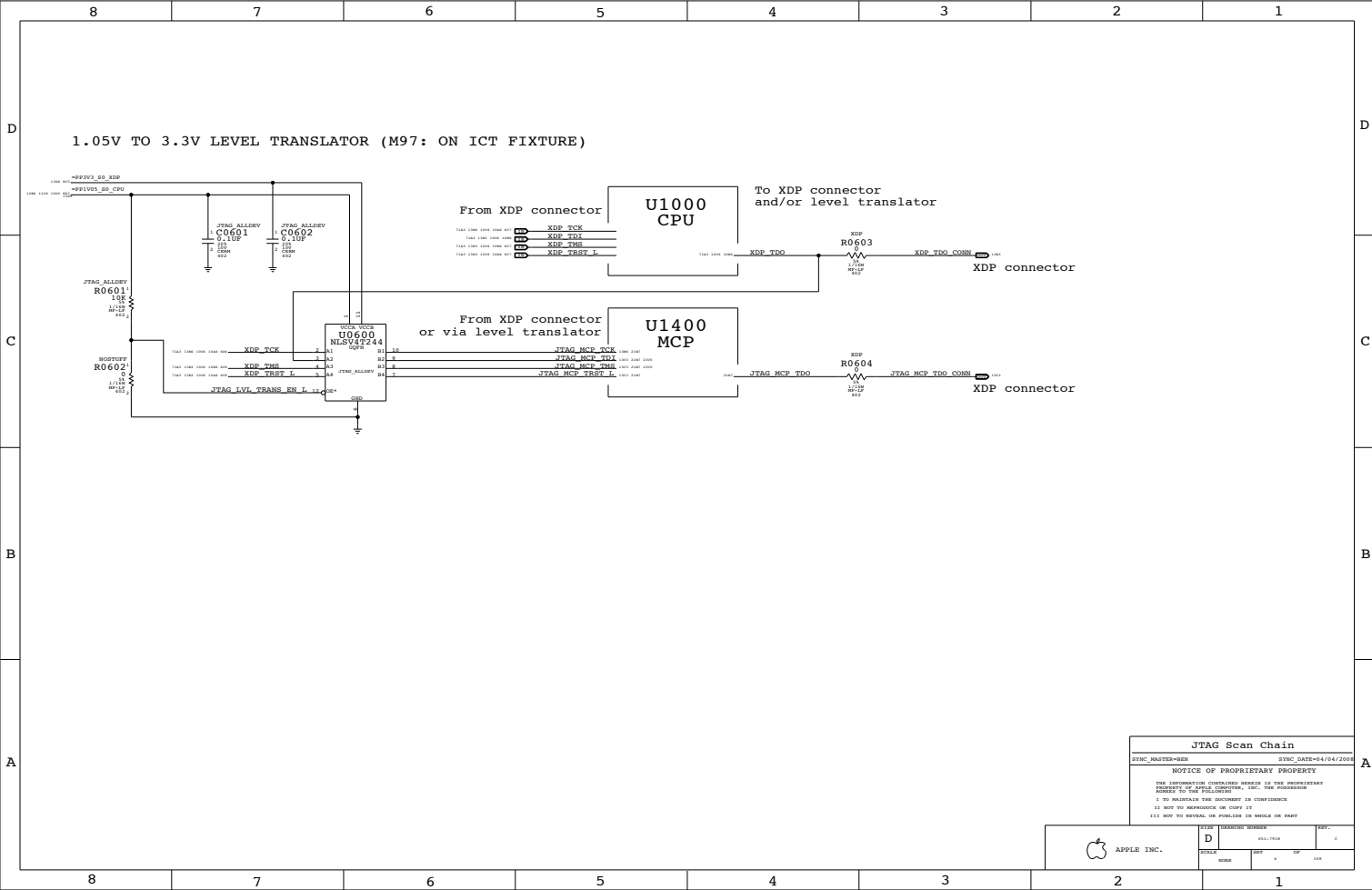
SUBMISSIONS ARE IN YELLOW TO # _____ FROM # _____ BY # _____ DATE _____ FILED # _____		METRIC DRAFTED _____ DRAFTED BY _____ DATE APPO _____ REV. DATE _____ ON APPRO _____ DISCUSSION _____ REVIEW _____ REVIEW _____		 APPLE INC. NOTICE OF PROPRIETARY PROTECTION THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. AND IS NOT TO BE DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE COMPUTER, INC. 1. NO REPRODUCTION OR DISCLOSURE OF THIS DOCUMENT IS TO BE MADE WITHOUT THE WRITTEN PERMISSION OF APPLE COMPUTER, INC. 2. NO REPRODUCTION OR DISCLOSURE OF THIS DOCUMENT IS TO BE MADE WITHOUT THE WRITTEN PERMISSION OF APPLE COMPUTER, INC.	
DO NOT WRITE (BRANDS) 		INTERNAL REVIEW REVIEW BY _____ DATE _____		SCHEM, M.L.B. M97A SCHEM NUMBER _____ REV. _____ 051-7918 _____ C	





M97 BOARD STACK-UP

[illegible]



JTAG Scan Chain

SYNCHRONIZED-BEN SYNCHRONIZED-BEN

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APPLE INC.		D		REV. 1.0		100	
DATE		REV		REV		REV	

8	7	6	5	4	3	2	1
Functional Test Points							
D	Fan Connectors		RIGHT CLUTCH CONN		DEBUG VOLTAGE		
	(NEED 3 TP)		TRUPE PPSVRT S0		TRUPE PPSVCORE S0 CPU		
	TRUPE FAN RT SW		TRUPE PPSV S3 ATCAMERA F		TRUPE PPSVUT4 S0		
	TRUPE FAN RT TACH		TRUPE PCIE MINI D2R N		TRUPE PPSVCORE S0 MCP		
	(NEED TO ADD 3 GND TP)		TRUPE PCIE MINI R2D N		TRUPE PPSV7 S0		
	MIC FUNC TEST		TRUPE PCIE CLUTCH MINI CONN P		TRUPE PPSV0 S0		
	TRUPE MIC HI CONN		TRUPE PCIE CLUTCH MINI CONN N		TRUPE PPSV5 S0		
	TRUPE MIC LO CONN		TRUPE USB CAMERA CONN N		TRUPE PPSVRT S0		
	TRUPE MIC SHLD CONN		TRUPE USB CAMERA CONN P		TRUPE PPSV3 S0		
	(NEED TO ADD 3 GND TP)		TRUPE PPSV BLAN		TRUPE PPSV7 S3		
C	SPEAKER FUNC TEST		TRUPE PCIE WAKE P		TRUPE PPSV7 S3		
	TRUPE SPEAKER L OUT		TRUPE SMBUS SMC A S3 SCL		TRUPE PPSV7 S3		
	TRUPE SPEAKER R OUT		TRUPE SMBUS SMC A S3 SDA		TRUPE PPSV7 S3		
	TRUPE SPEAKER L IN		TRUPE CONN USB2 BT P		TRUPE PPSV1V05 S5		
	TRUPE SPEAKER R IN		TRUPE CONN USB2 BT N		TRUPE PPSV3 GSH		
	TRUPE SPEAKER SUB L OUT		TRUPE MINI CLKREQ N I		TRUPE PPSV3 GSH		
	TRUPE SPEAKER SUB R OUT		TRUPE MINI RESET CONN L		TRUPE PPSV3 INDET PHY		
	(NEED TO ADD 3 GND TP)		SATA HDD CONN		TRUPE PPSV1V05 DET		
	THERMAL FUNC TEST		TRUPE PPSV S0 HDD FLT (NEED 4 TP)		TRUPE PPSV3 G3 RTC		
	TRUPE MCPHMSNS D2 P		TRUPE SATA HDD R2D P		TRUPE PPSV MEAN		
B	TRUPE MCPHMSNS D2 N		TRUPE SATA HDD R2D N		TRUPE PPSV S0 ODD		
	LVDS FUNC TEST		TRUPE SATA HDD R2D N		TRUPE PPSV S0 HDD FLT		
	TRUPE DPV3 LCDVDD SW F		TRUPE SATA HDD D2R C P		TRUPE PPSV S0 ADAPT SMC		
	TRUPE DPV3 S0 LDO F		TRUPE SATA HDD D2R C N		TRUPE PPSV S3 IDO		
	TRUPE PPSV0 S0 LDO F		TRUPE SATA ODD R2D N		TRUPE PPSV S3 IDO		
	TRUPE PPSV0 S0 LDO F		(NEED TO ADD 4 GND TP)		TRUPE PPSV S3 IDO		
	TRUPE LVDS IG DDC DATA		IPD FLEX CONN		TRUPE PPSV LCDVDD SW F		
	TRUPE LVDS IG A DATA SC0		TRUPE DPV3 S3 LDO		TRUPE PPSV S3 IDO		
	TRUPE LVDS IG A DATA SC1		TRUPE DPV3 S3 LDO		TRUPE PPSV S3 IDO		
	TRUPE LVDS IG A DATA SC2		TRUPE DPV3 S3 LDO		TRUPE PPSV S3 IDO		
	TRUPE LVDS IG A DATA SC3		TRUPE DPV3 S3 LDO		TRUPE PPSV S3 IDO		
A	TRUPE LVDS IG A DATA SC4		TRUPE DPV3 S3 LDO		TRUPE PPSV S3 IDO		
	TRUPE LVDS IG A DATA SC5		TRUPE DPV3 S3 LDO		TRUPE PPSV S3 IDO		

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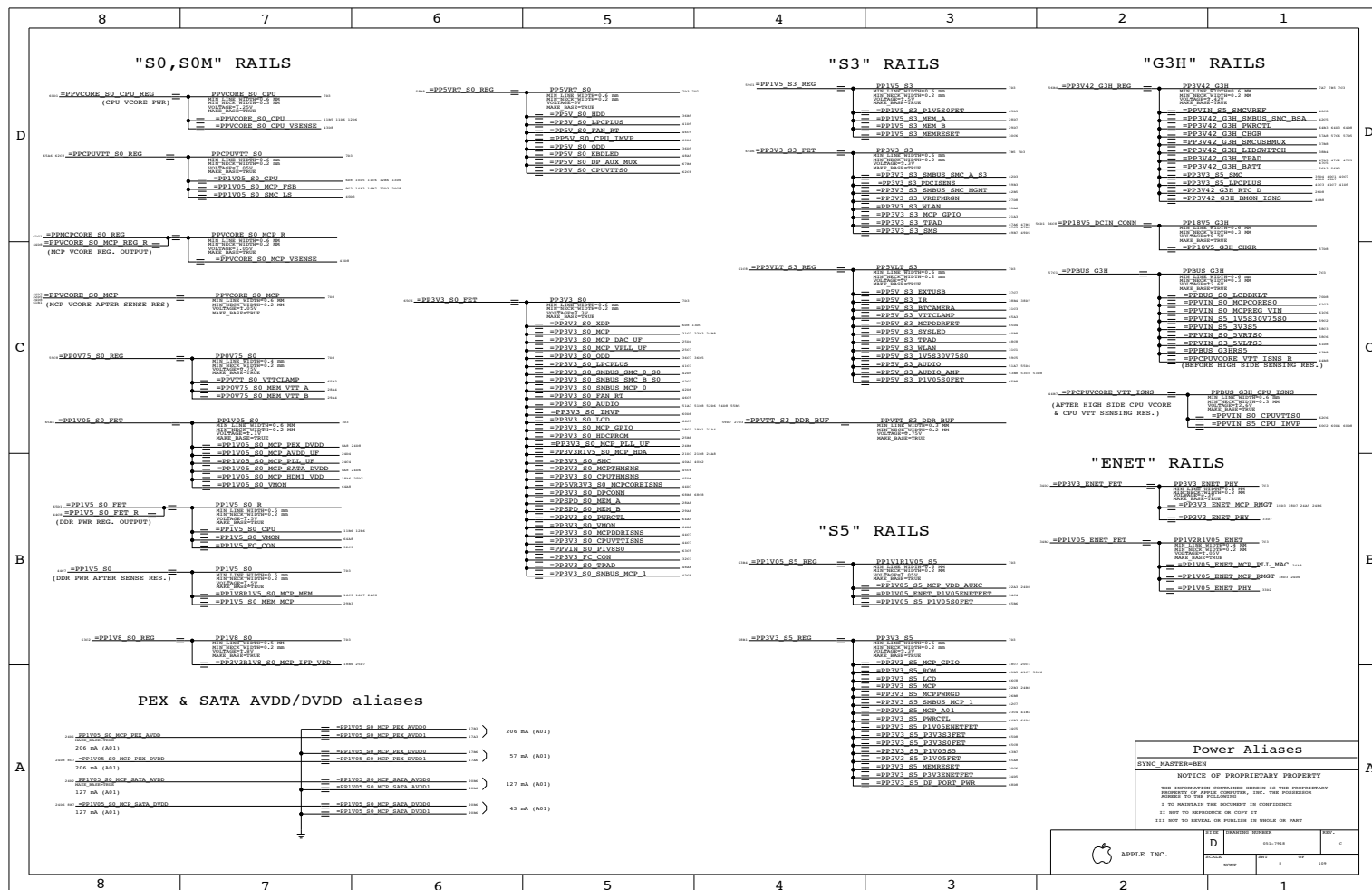
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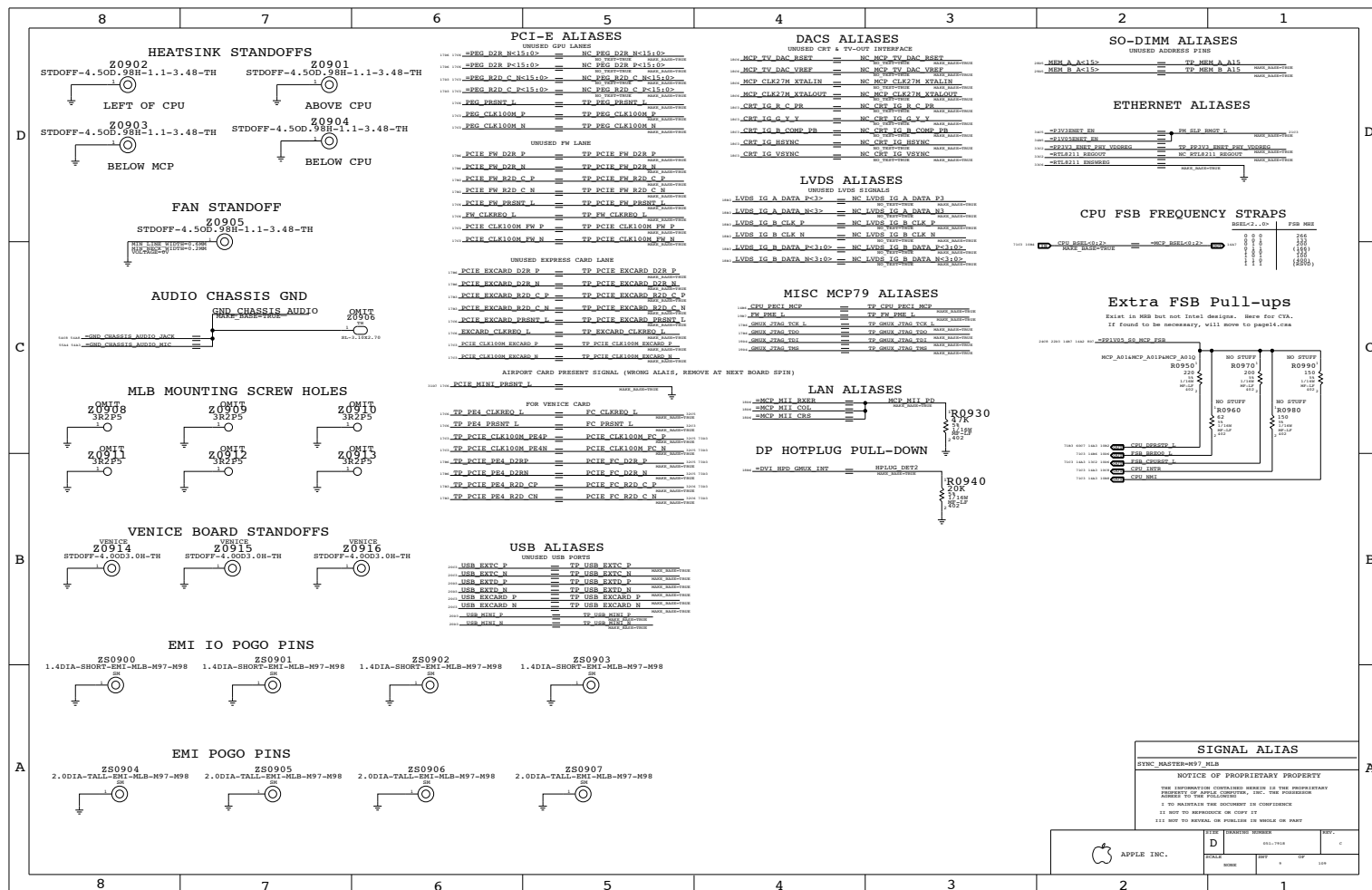
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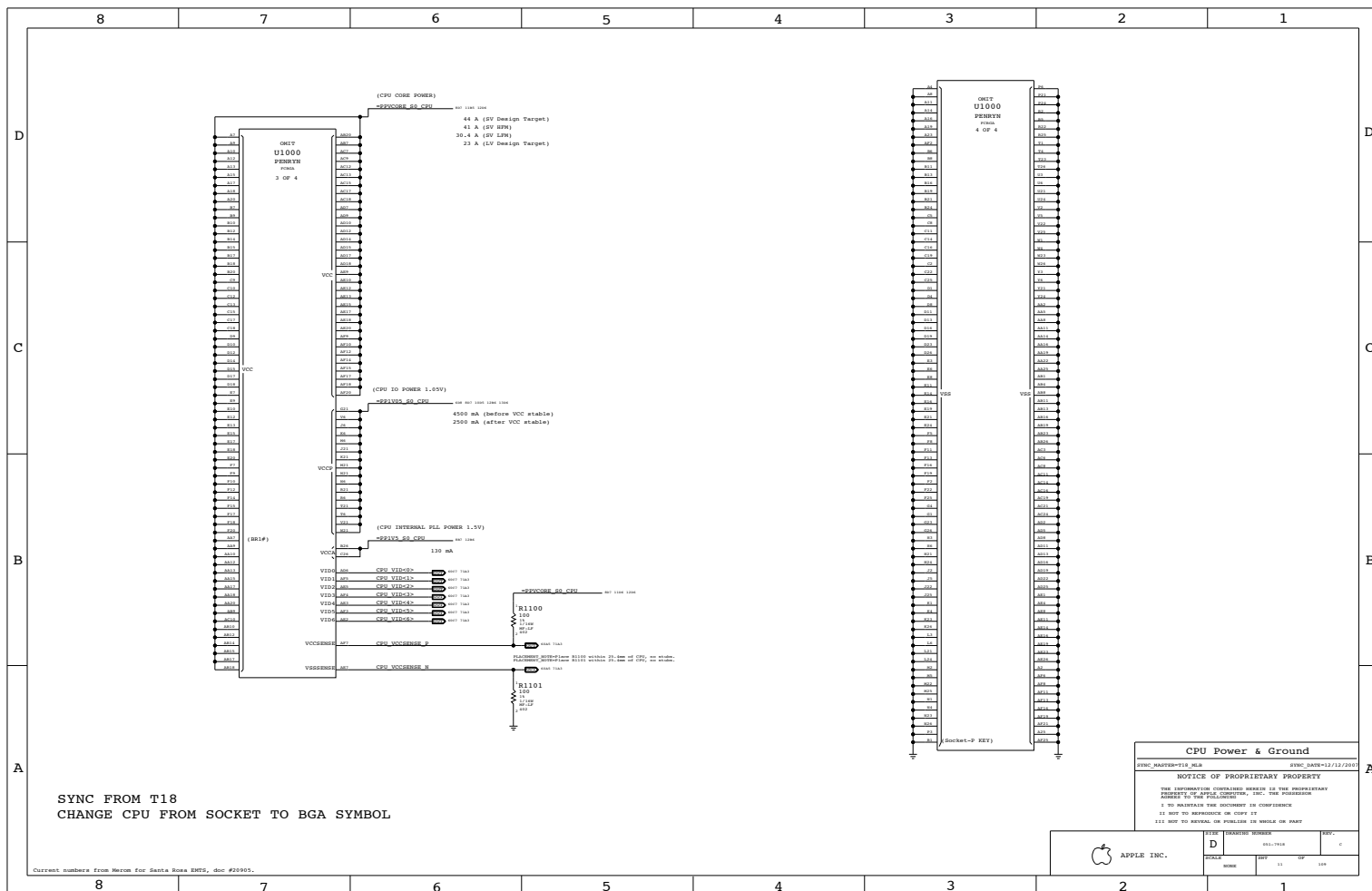
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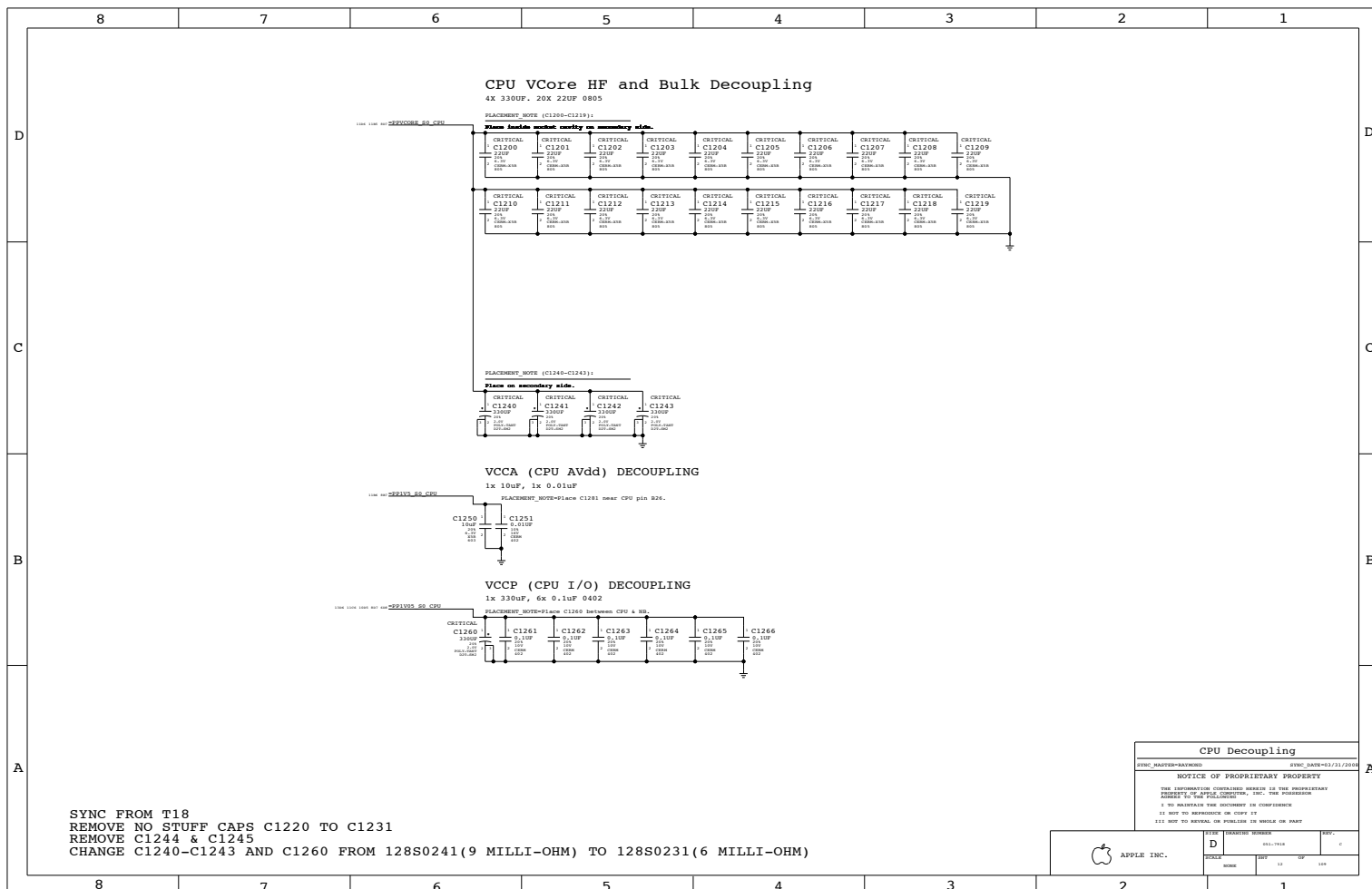
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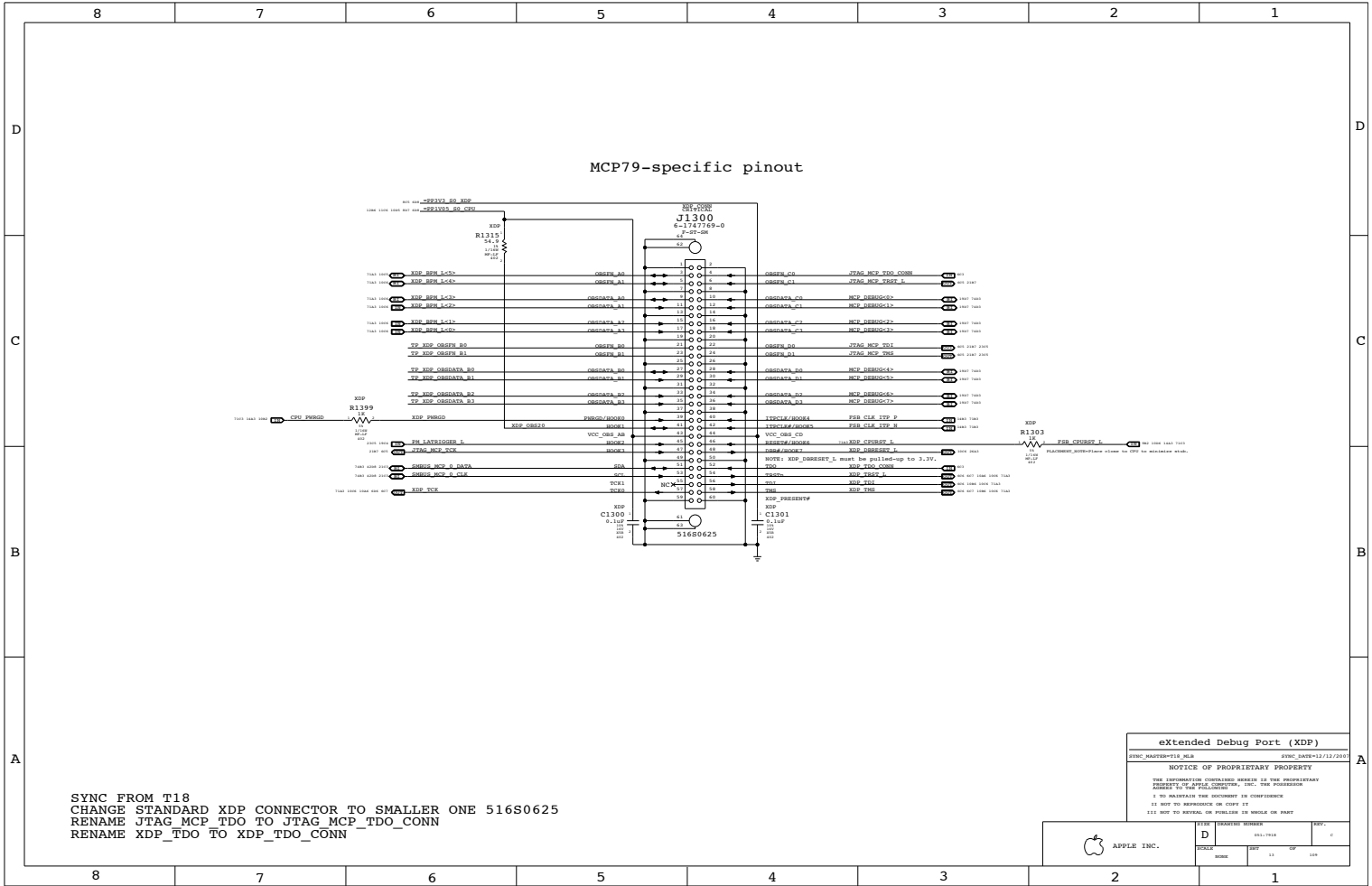
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D	08/11/2018	
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NONE	7	100

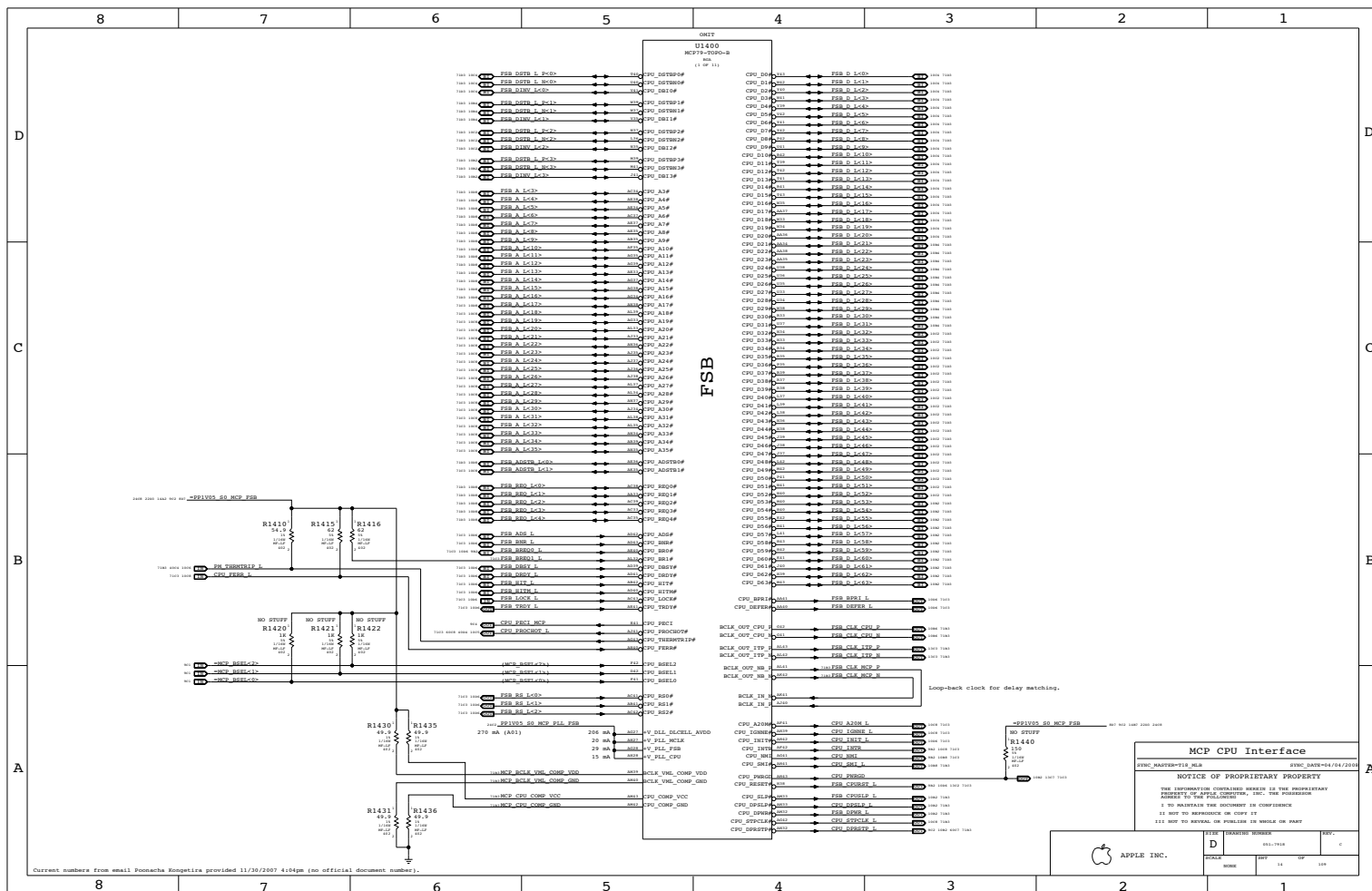


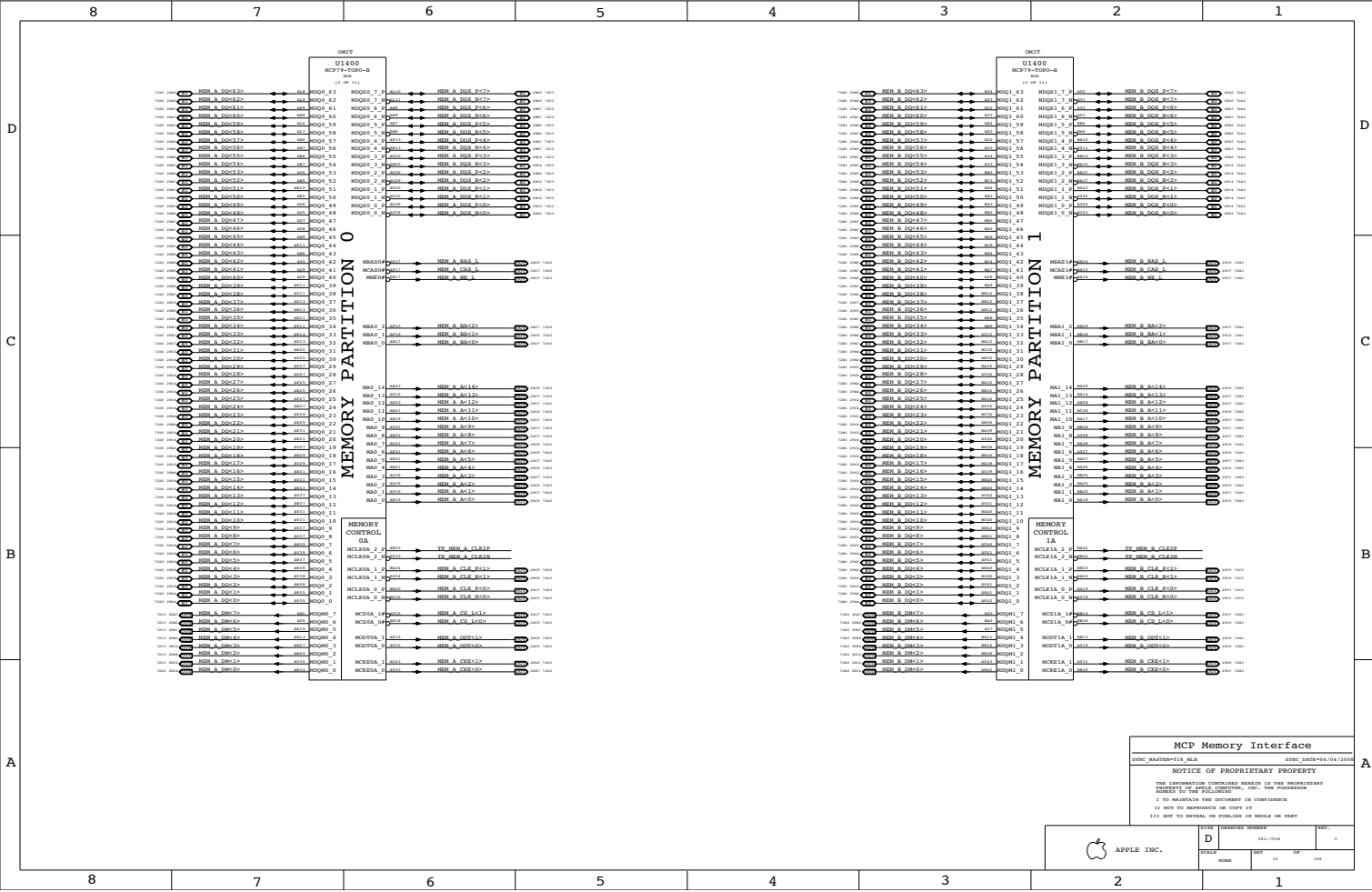


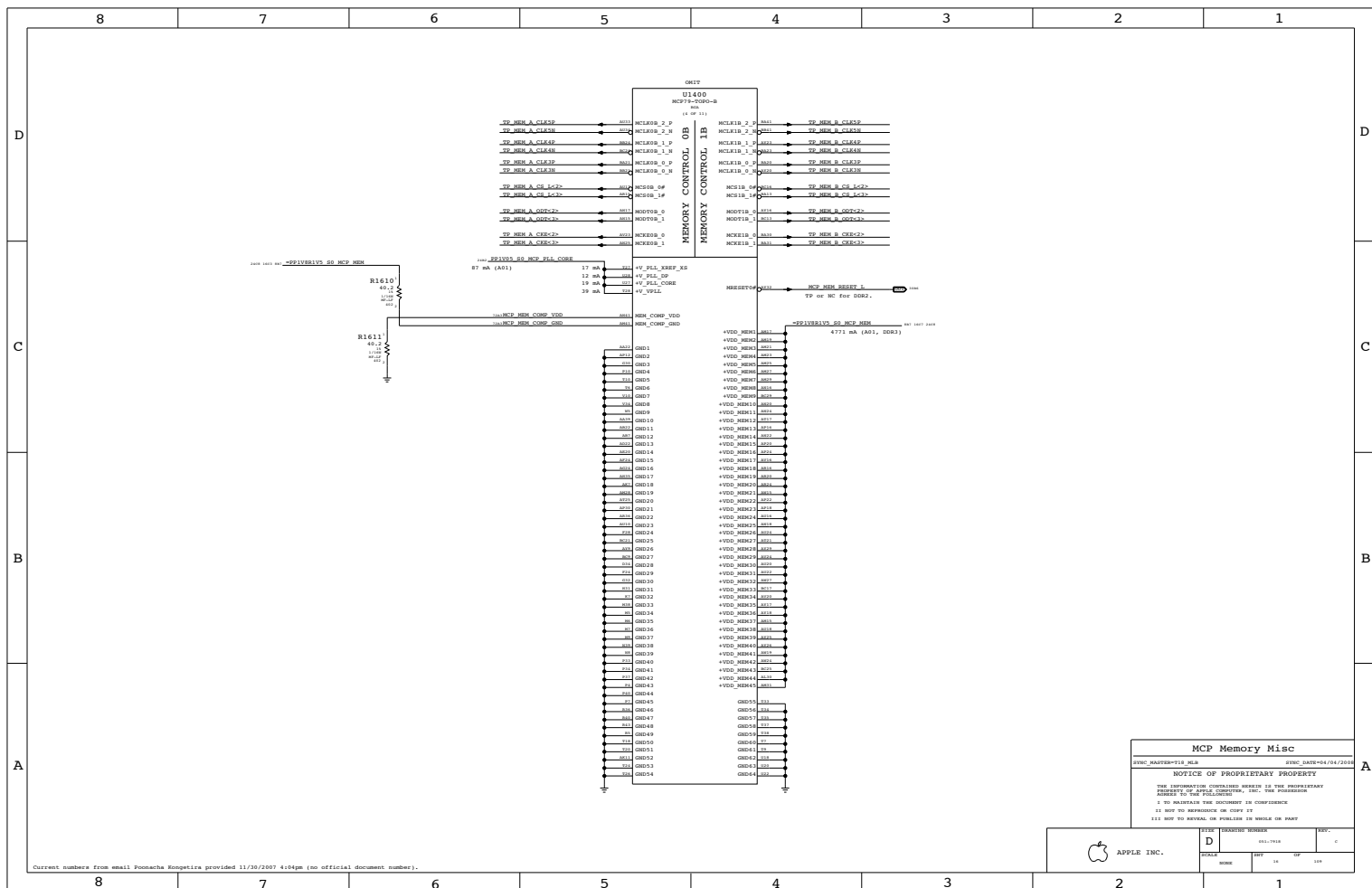


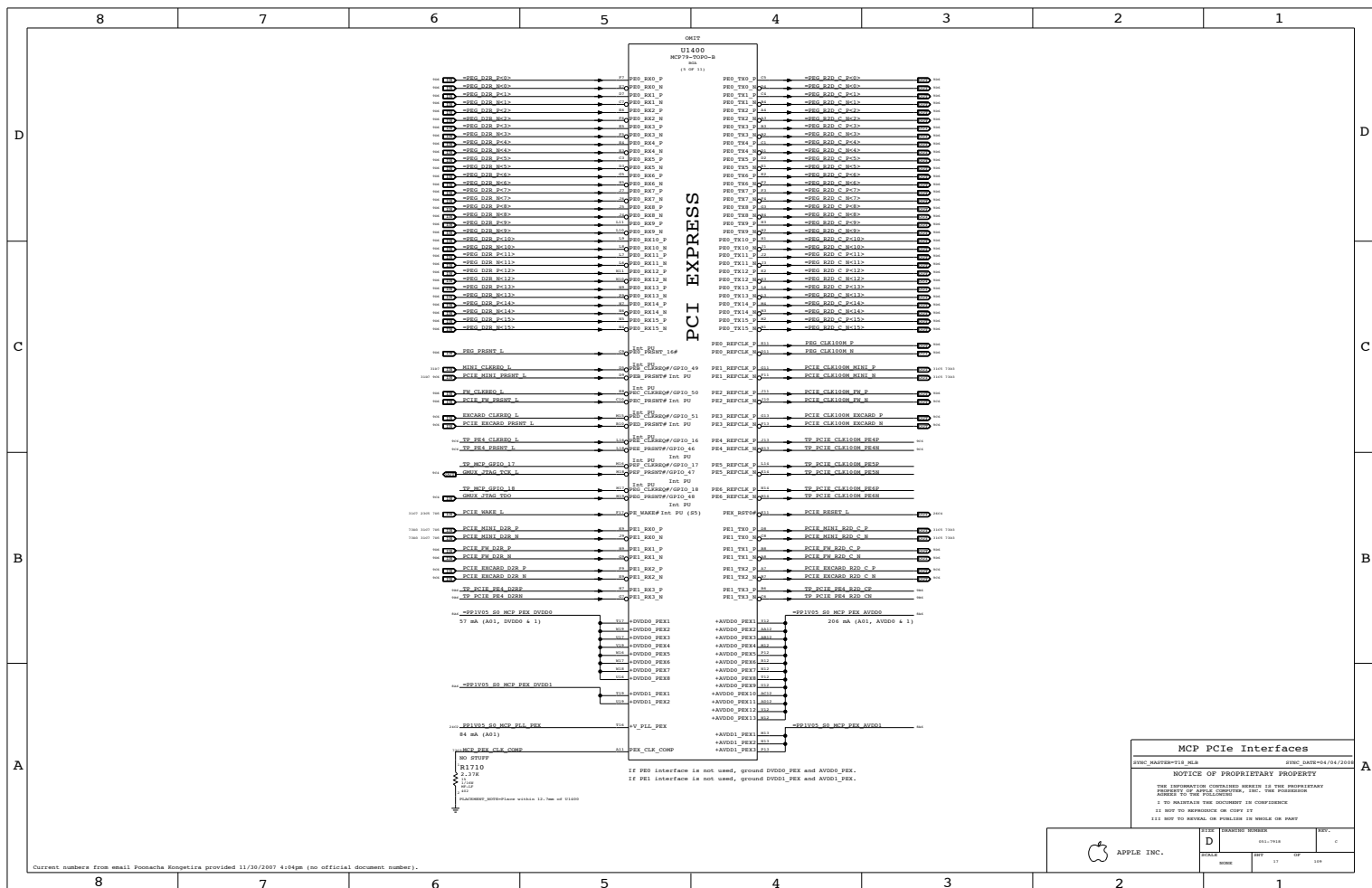


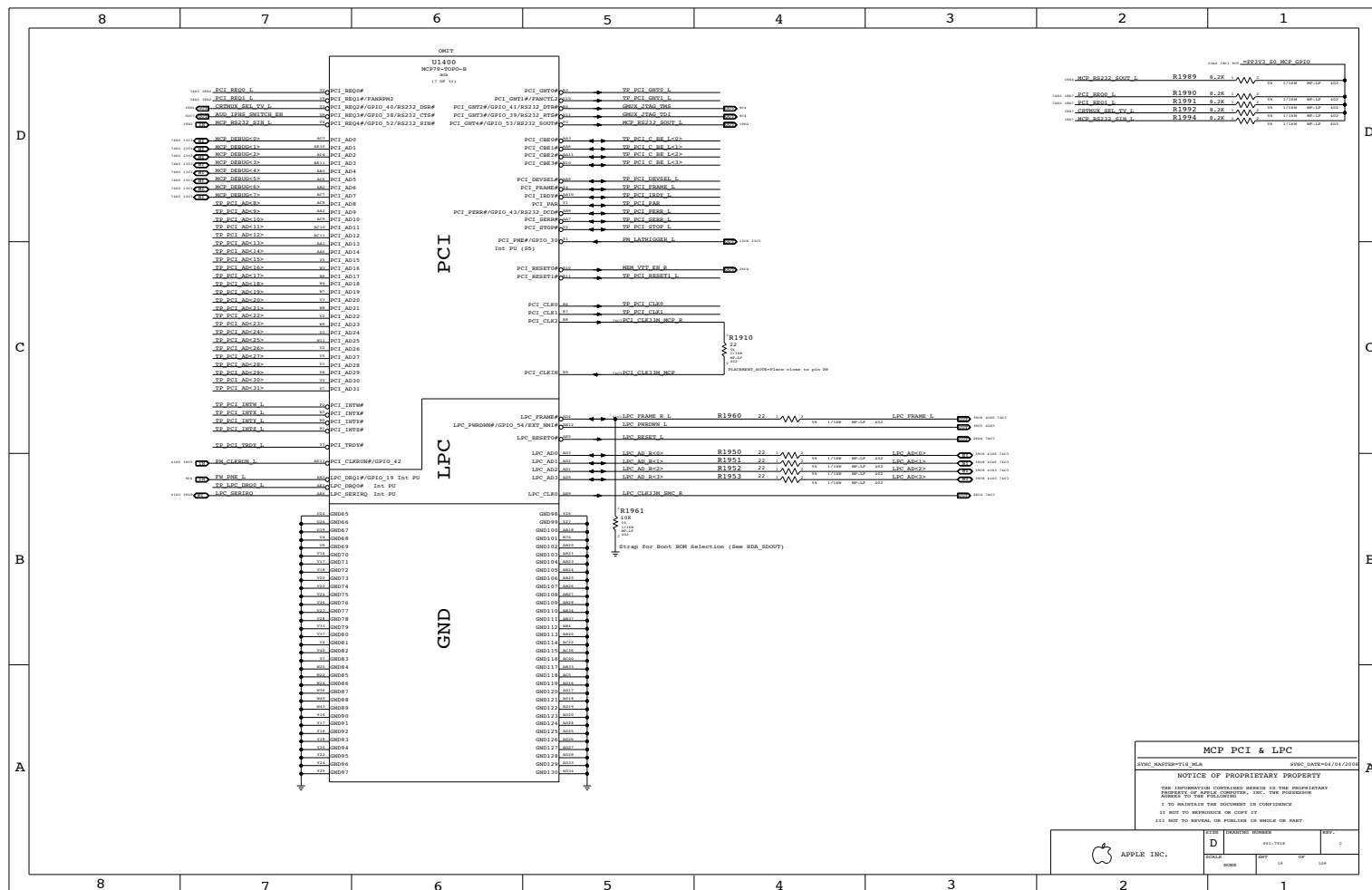


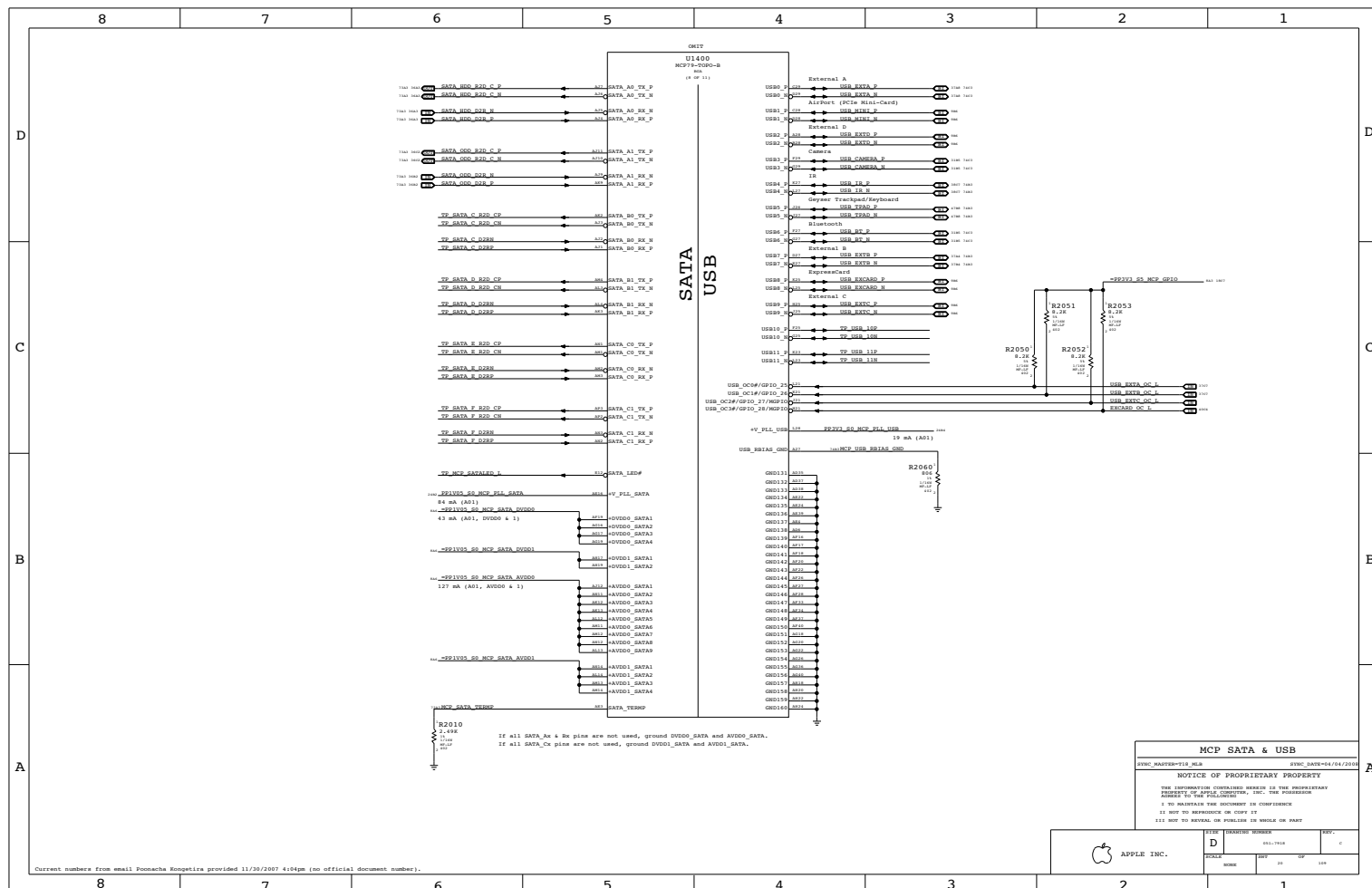


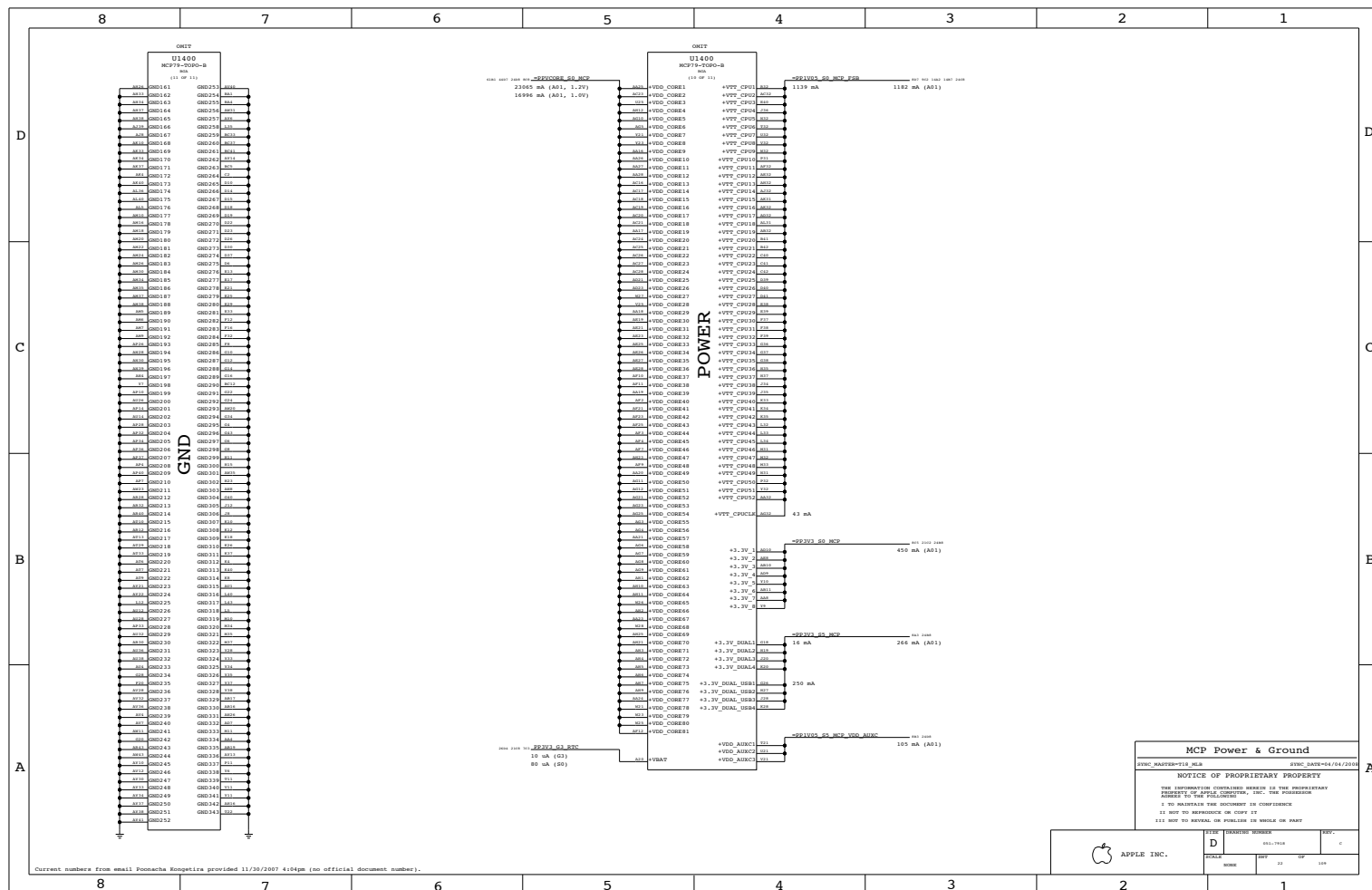


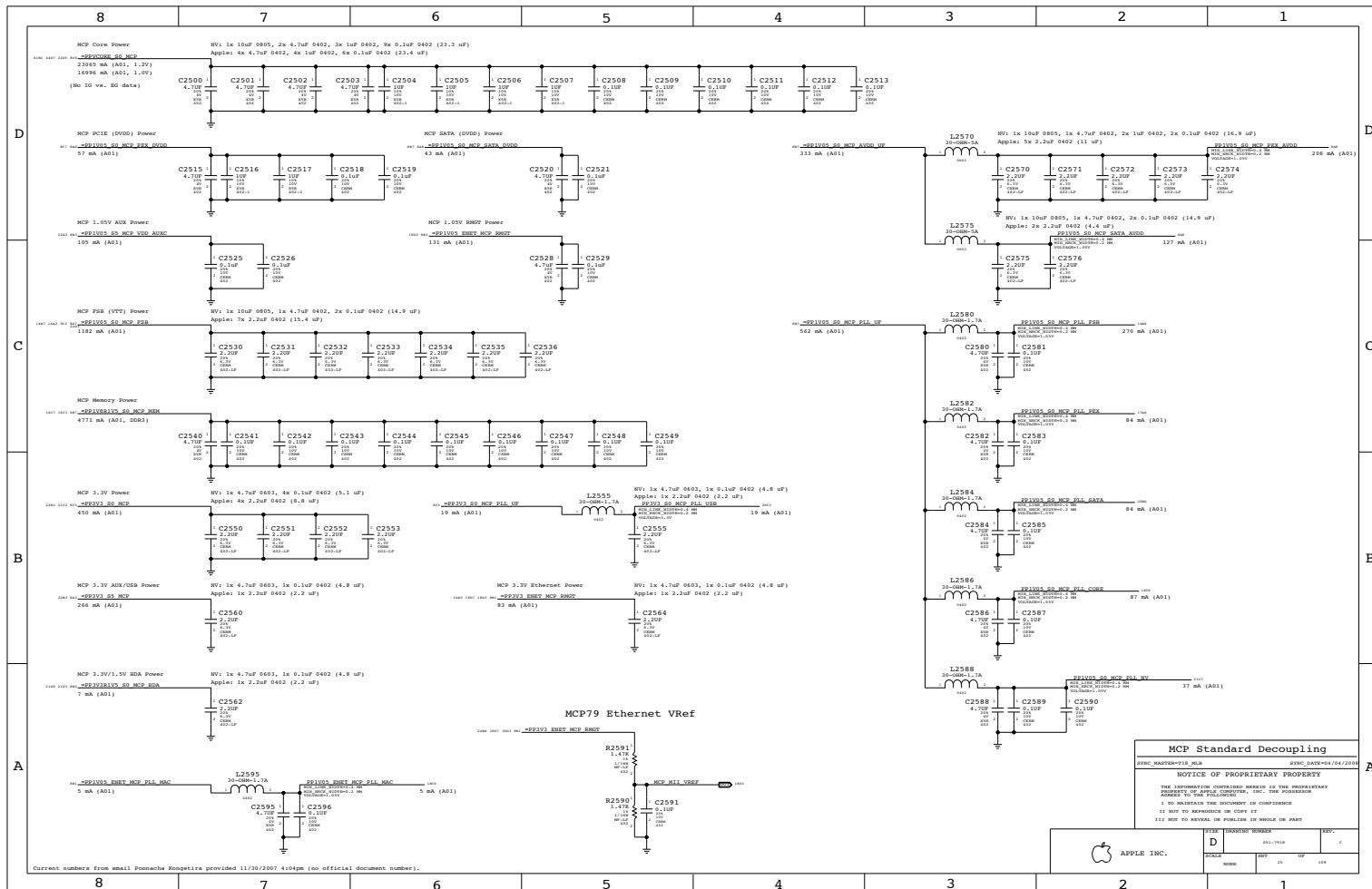


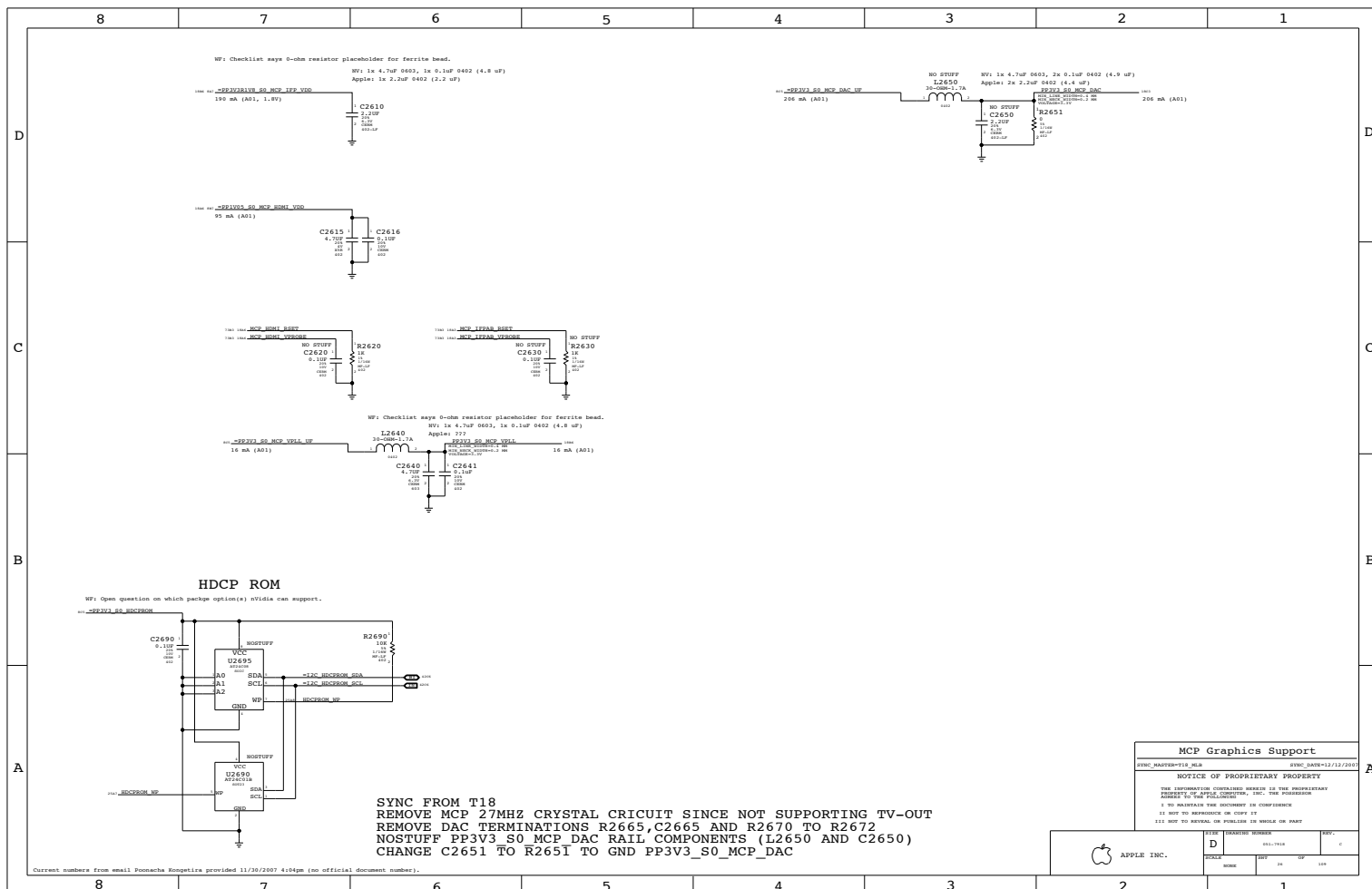


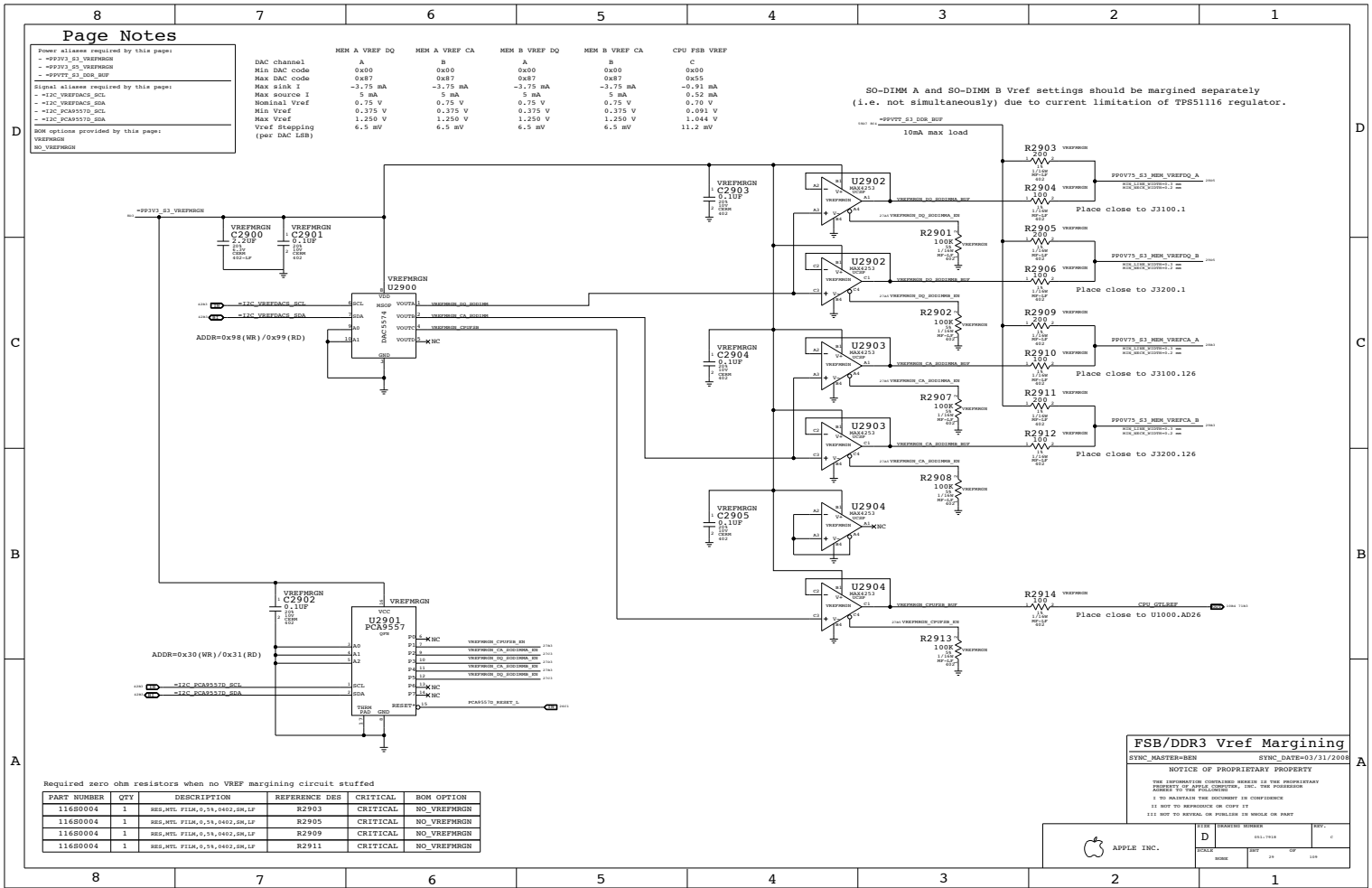


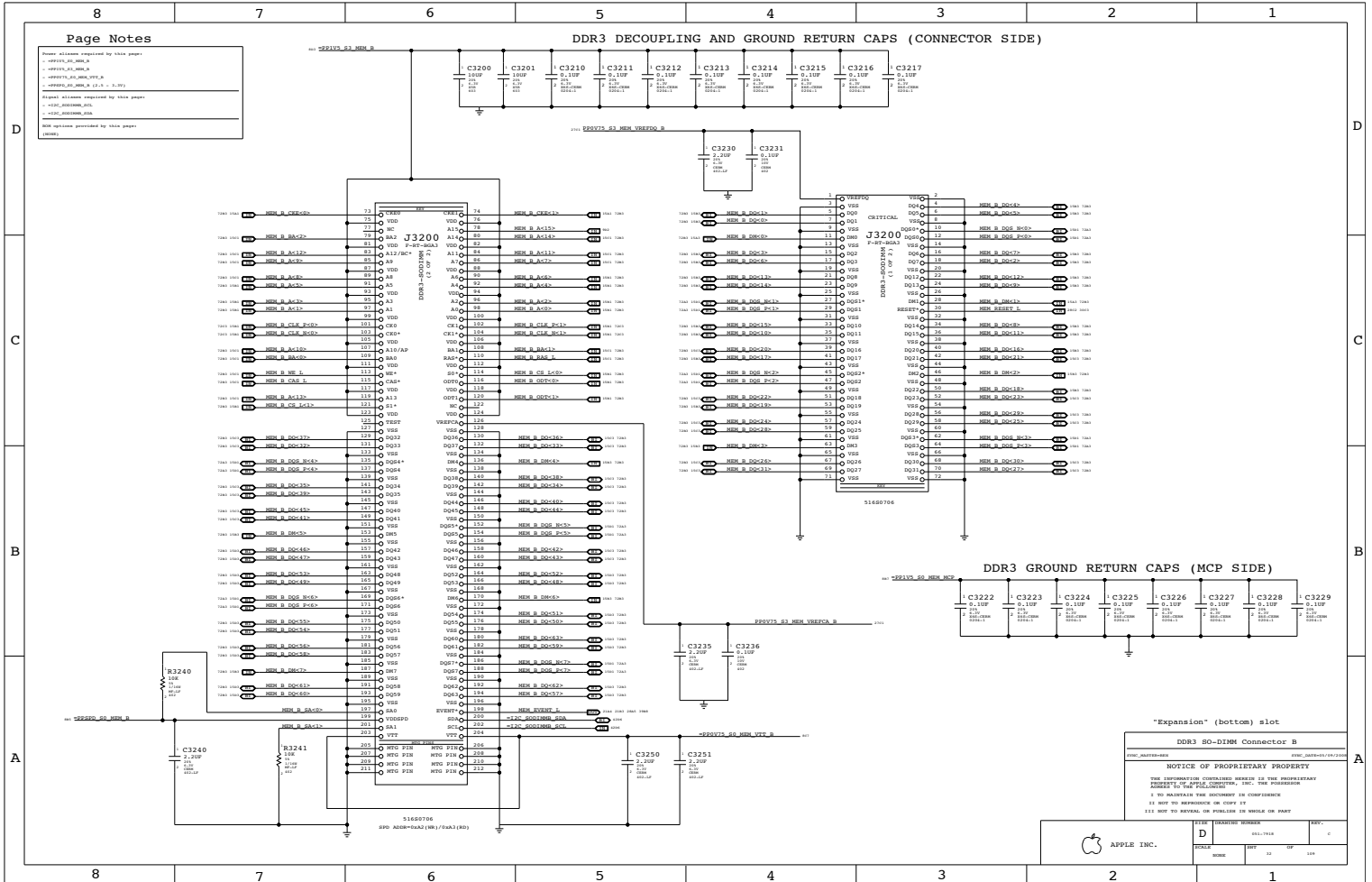


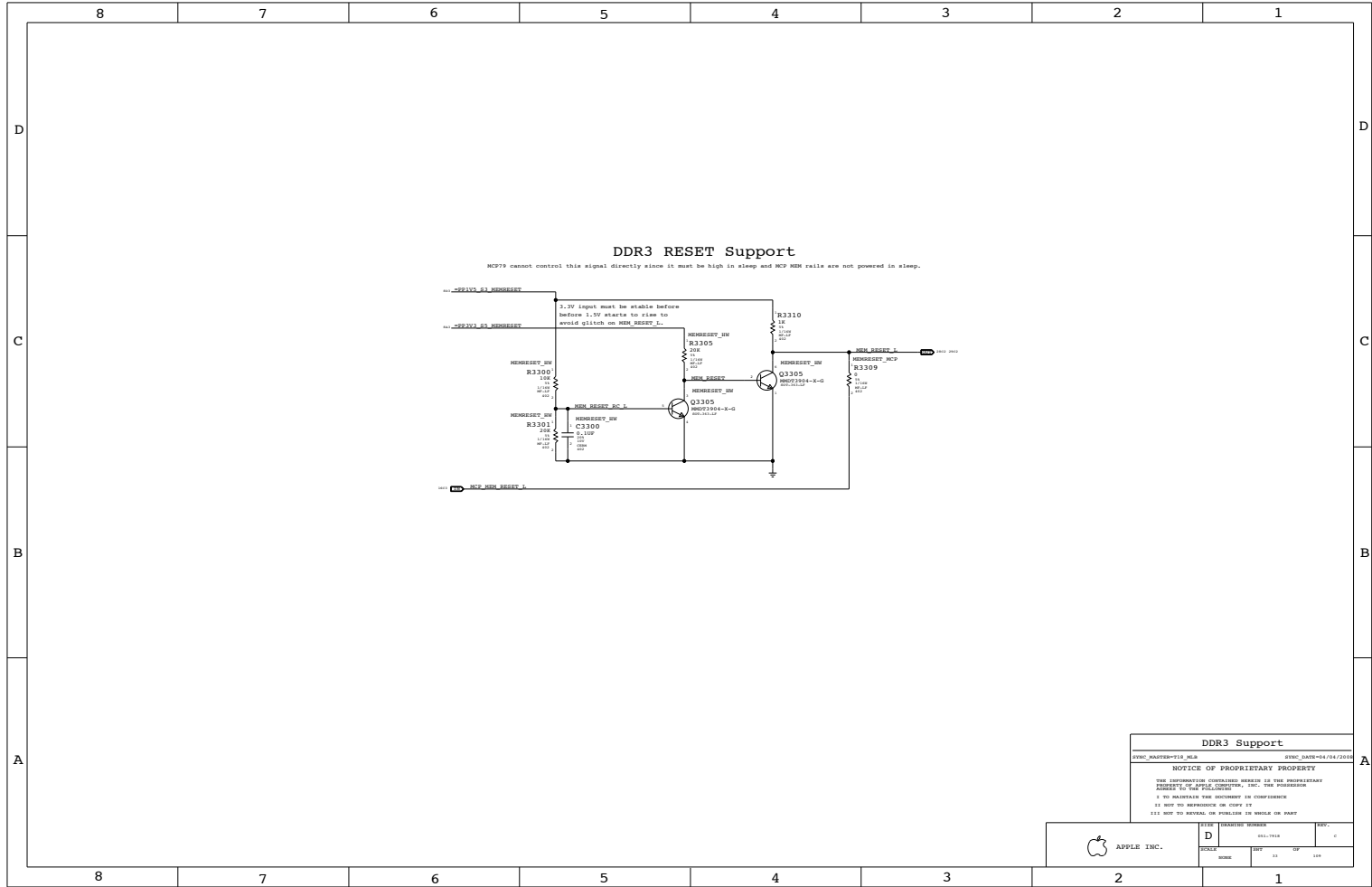












DDR3 Support

SYMC_MCP7900-110_MCU SYMC_MCP7900-110/104/105/106

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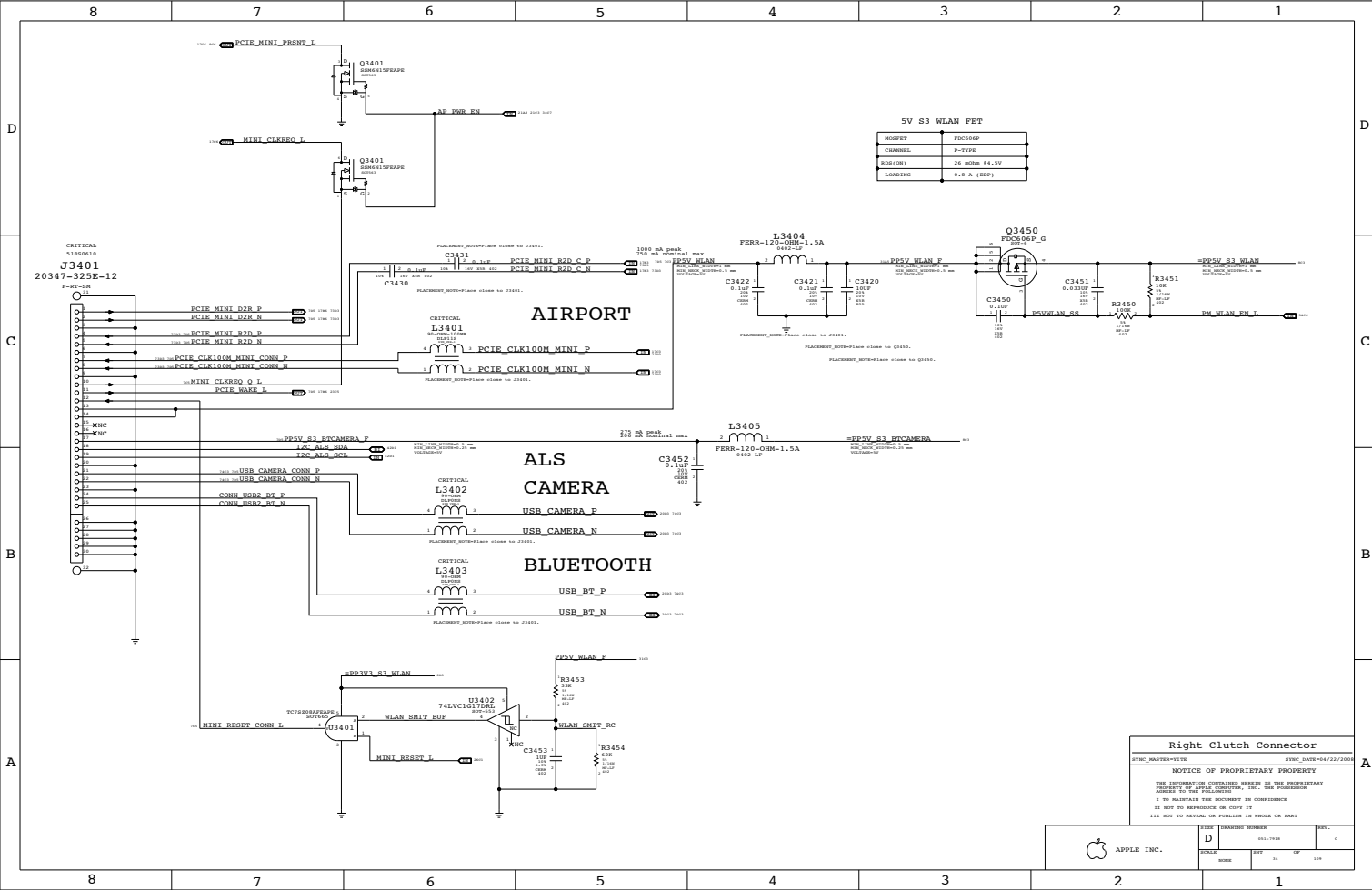
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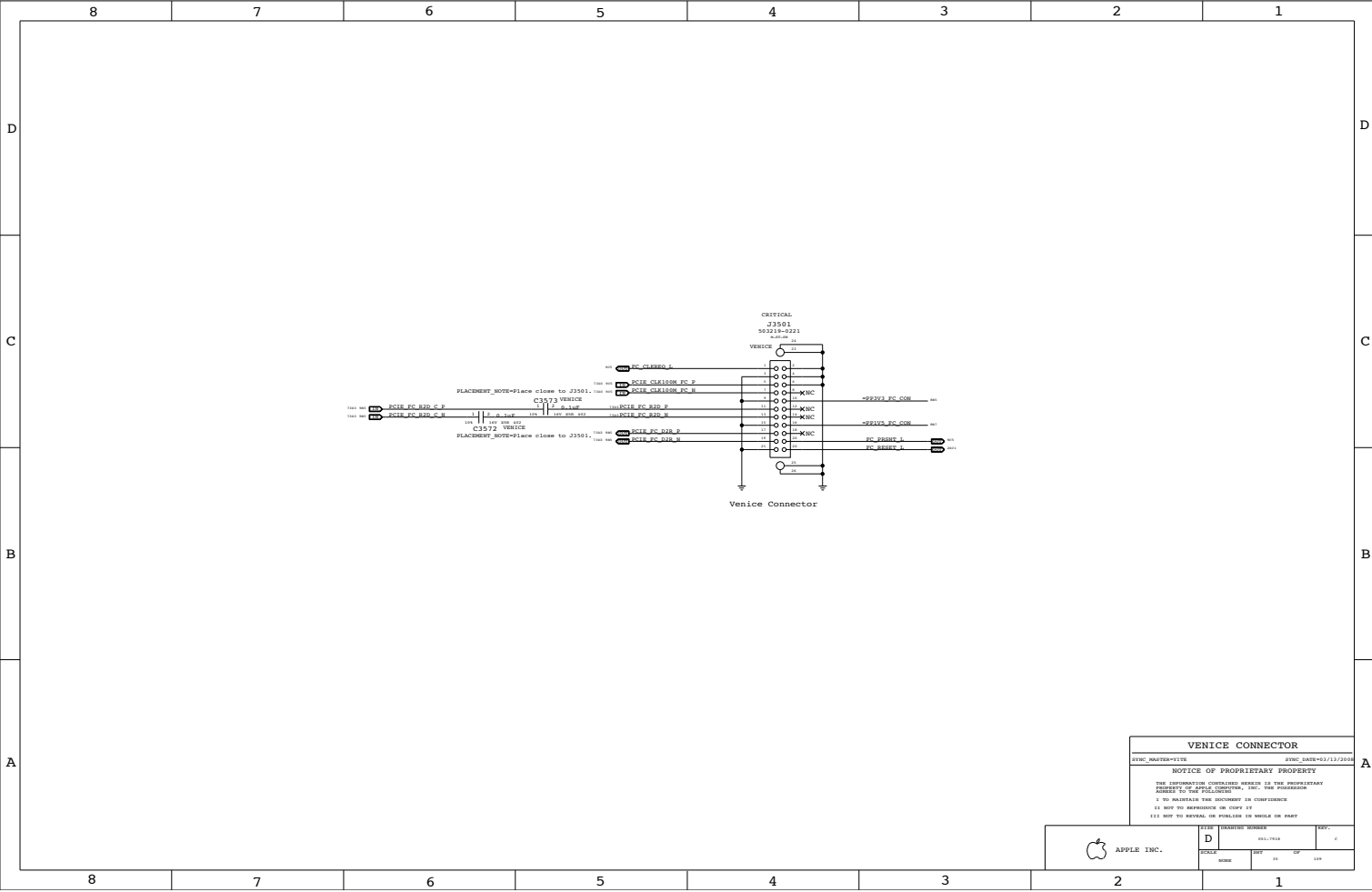
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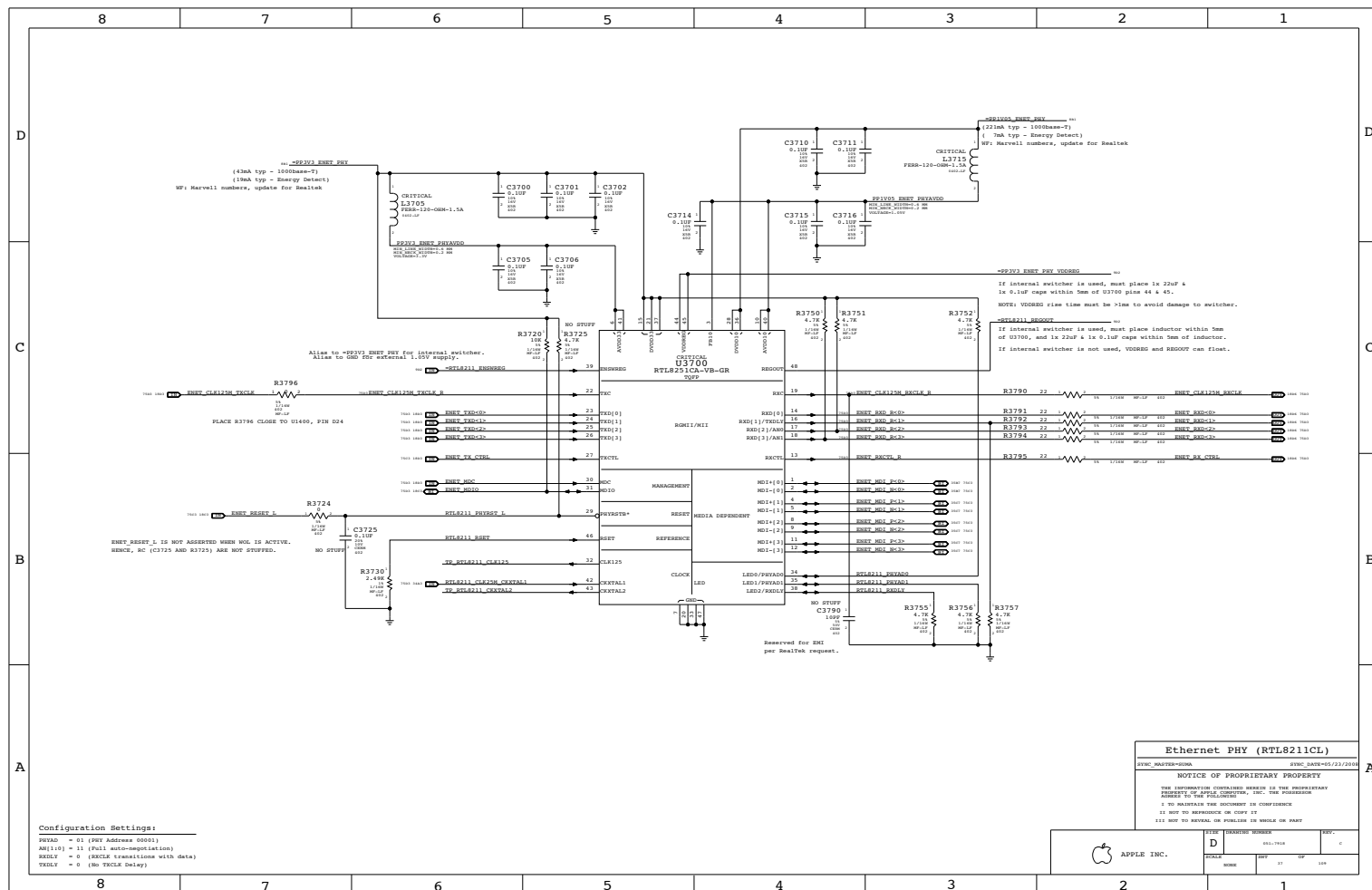
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VENICE CONNECTOR			
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FORM REVISION NUMBER			
D	001-1018	REV. 0	
APPLE INC.	DATE	BY	CHK





```
"WLAN" = ("S3" 44 "AP_PWR_EN" 44 ("AC" || "S0"))
```

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



@ 2.5V V_{GS}:
R_{DS(on)} = 90mOhm max
I(max) = 1.7A (85C)

Rds(on) = 90mOhm max

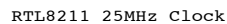
$$I(\text{max}) = 1.7 \text{ A (0.5C)}$$

MOBILE:

Recommend aliasing PM_SLP_RESET_L and
=P3V3ENET_EN. Nets separated on
AR2 for alternate power options.



Recommend aliasing PW_SLP_ENGT_L and
-PW05ENET_EN. Nets separated on
AR2 for alternate power options.



NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RSGT rails are powered.
Designs must ensure PHY is powered whenever RSGT rails are, or use separate crystal.

```

Ethernet & AirPort Support
-----
SYNC_MASTER=GDMA                                SYNC_DATE=07/01/2008

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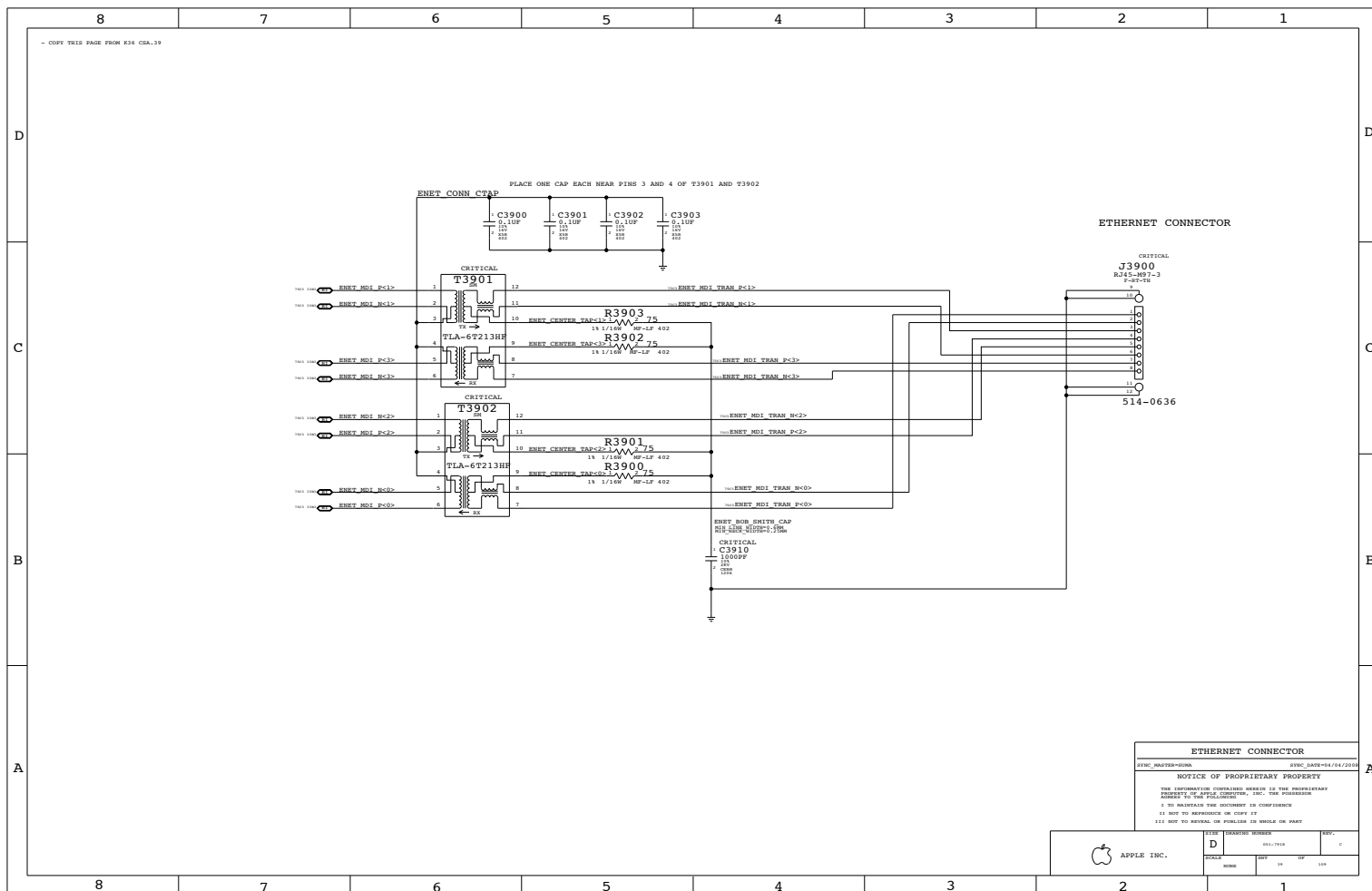
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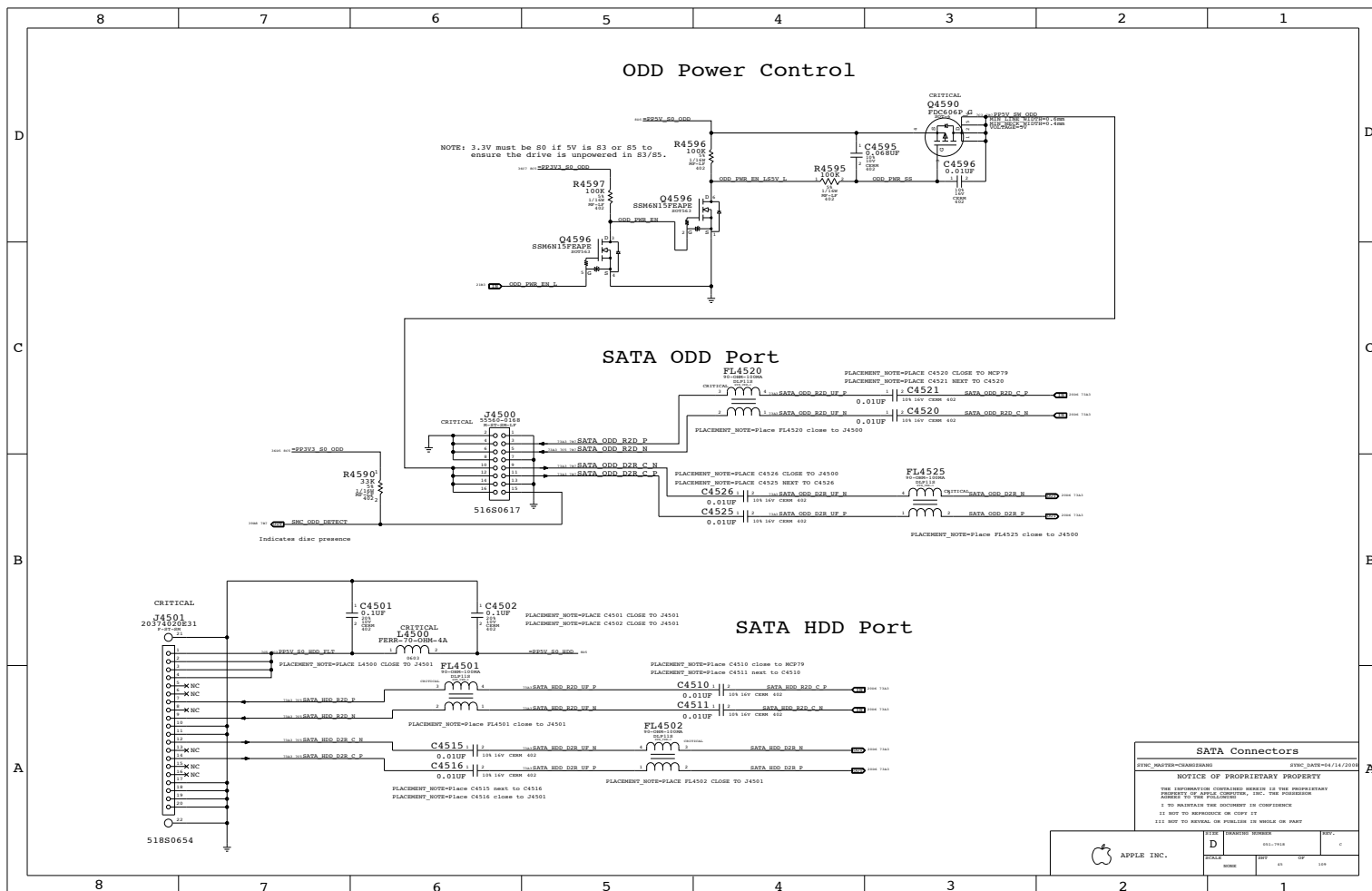
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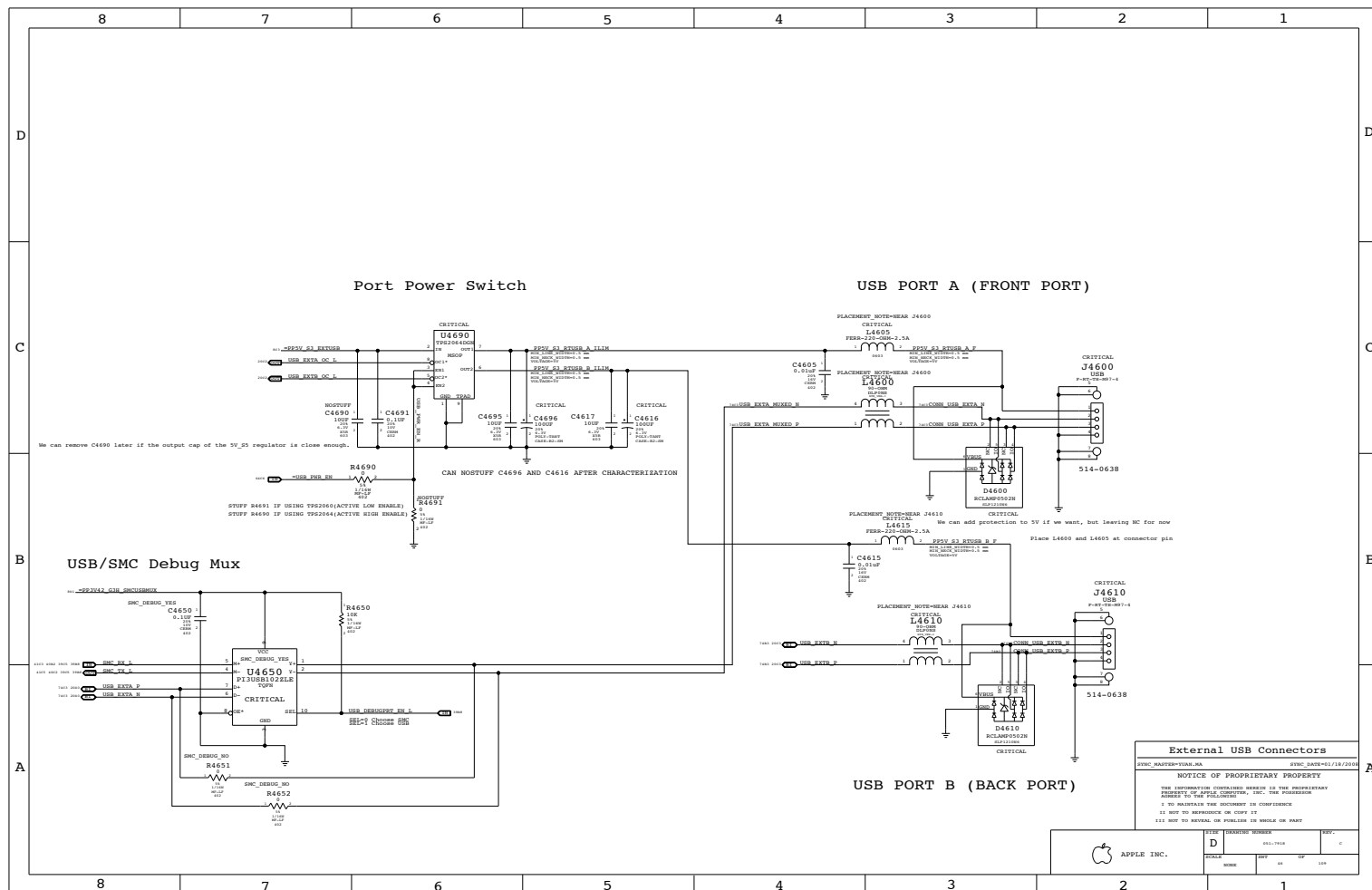
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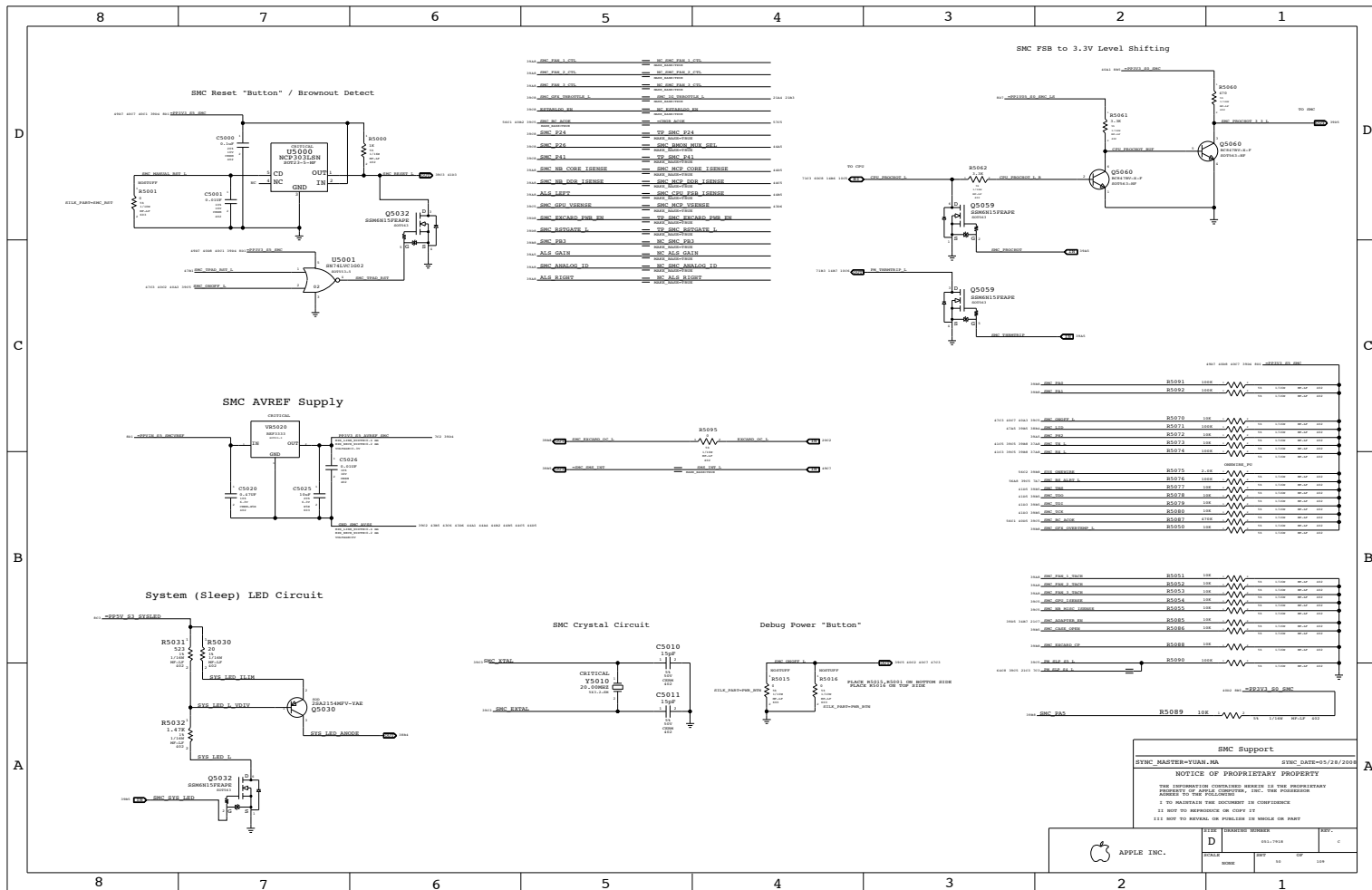


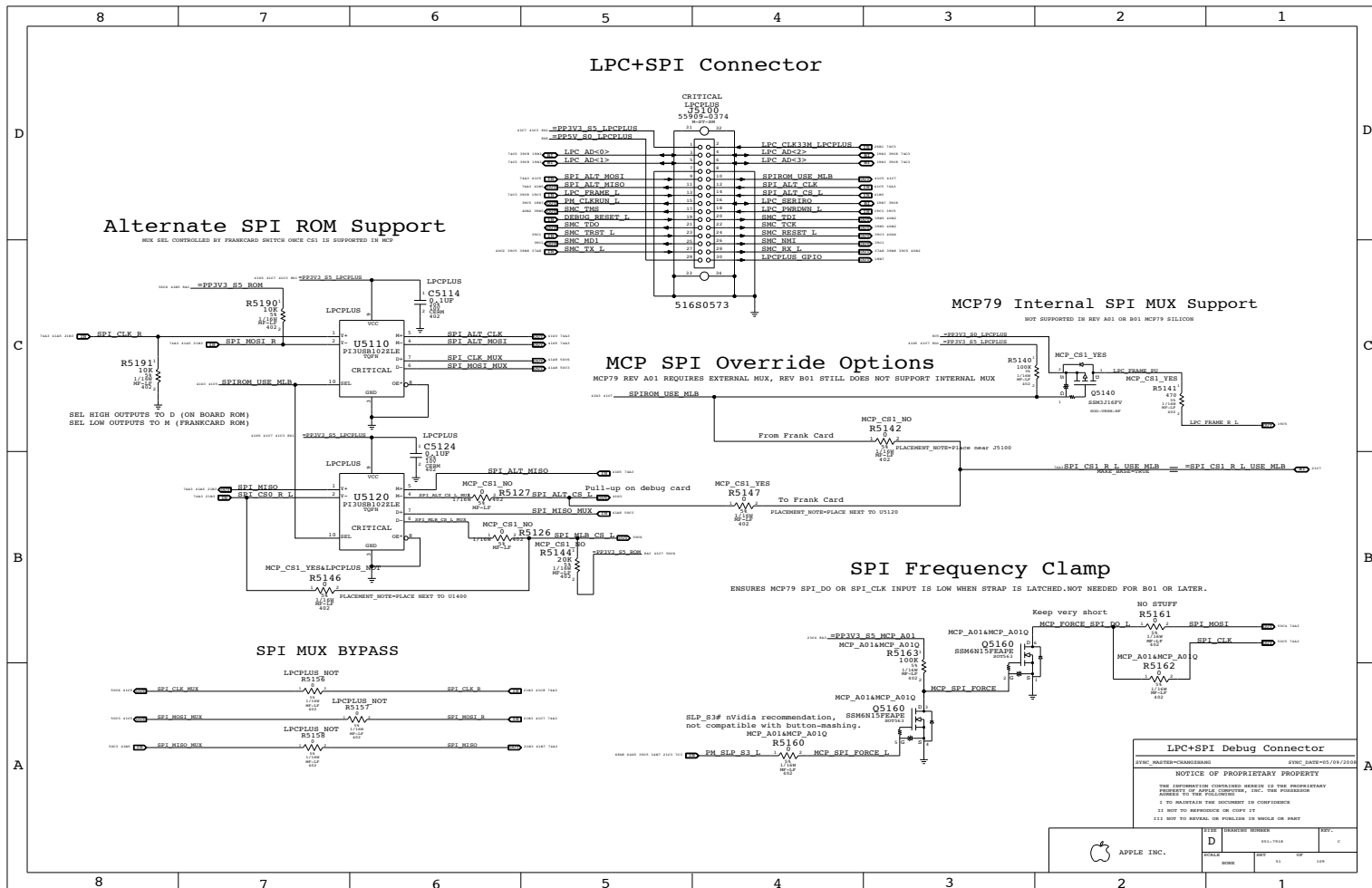
SIZE D	DRAWING NUMBER 051-7918	REV. C
SCALE NONE	SHEET OF 38 100	

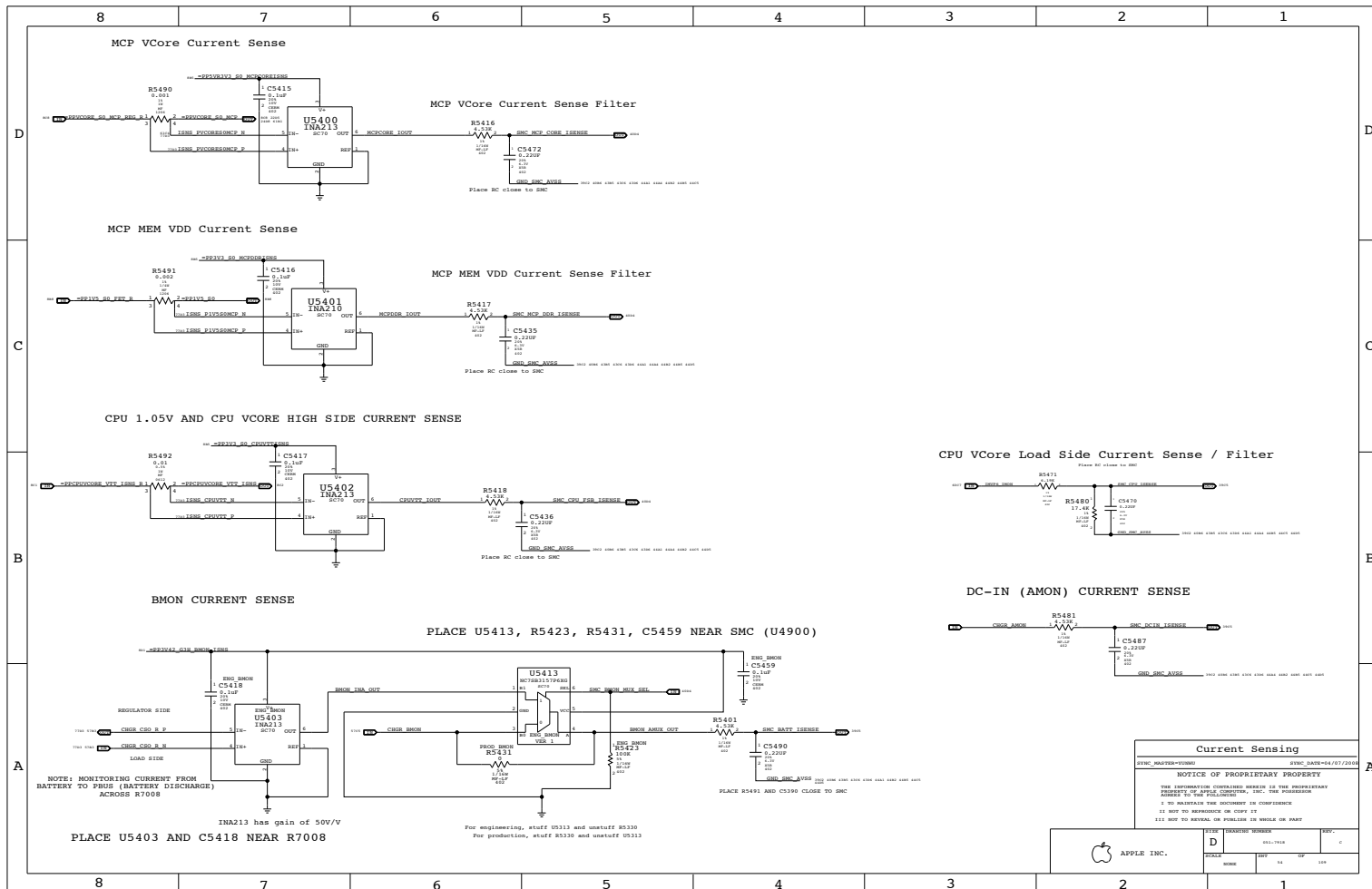


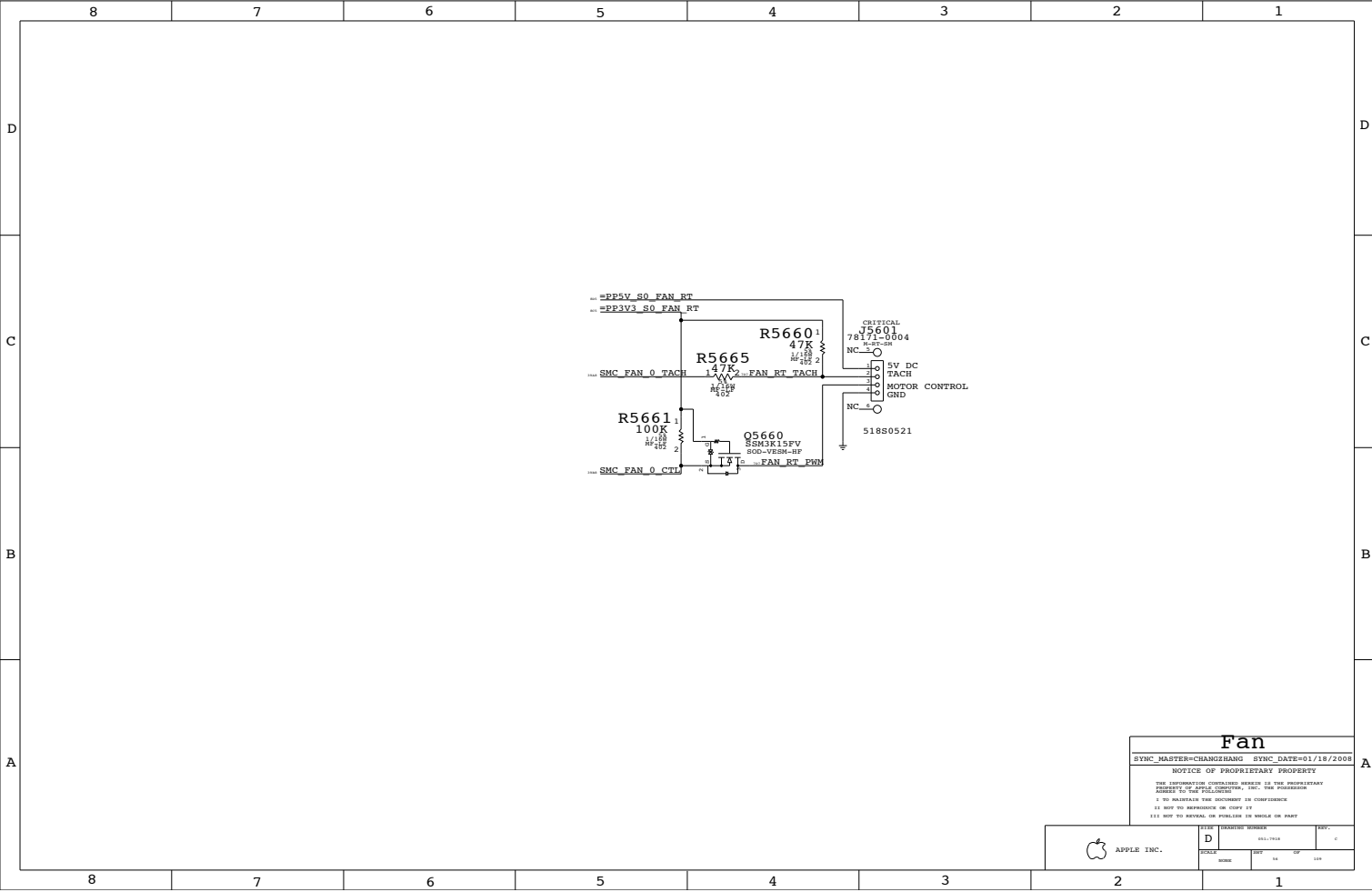


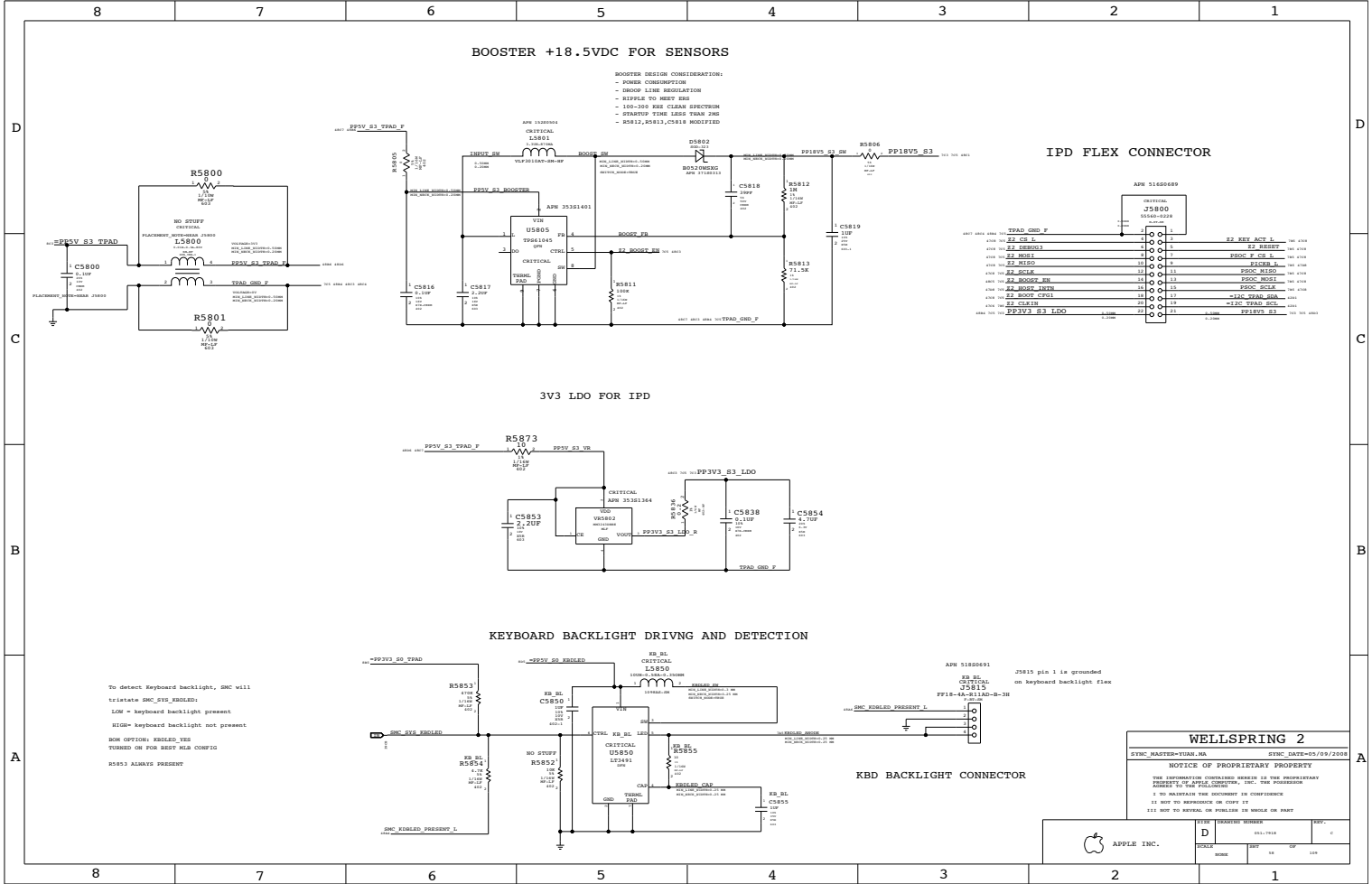












Digital SMS

Pull-up required if SMS_INT_L not used.

Desired orientation when placed on board top-side:

+E (+up) Front of system

Circle indicates pin 1 location when placed in correct orientation

Stuff R5931 AND NoDuff R5932 to use U5930
NoDuff R5931 AND Stuff R5932 if U5930 is not used

Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY BMC

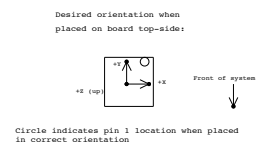
Desired orientation when placed on board top-side:

+E (+up) Front of system

Circle indicates pin 1 location when placed in correct orientation

SMS	
SYNC_MASTER=YUNWU	SYNC_DATE=06/26/2008
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APPLE INC.	DATE	DESIGN NUMBER	REV.
	2008-06-26	001-7010	C



Digital SMS

Pull-up required if SMS_INT_L not used.

Desired orientation when placed on board top-side:

+E (+up) Front of system

Circle indicates pin 1 location when placed in correct orientation

Stuff R5931 AND NoDuff R5932 to use U5930
NoDuff R5931 AND Stuff R5932 if U5930 is not used

Analog SMS

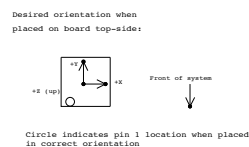
R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY BMC

Desired orientation when placed on board top-side:

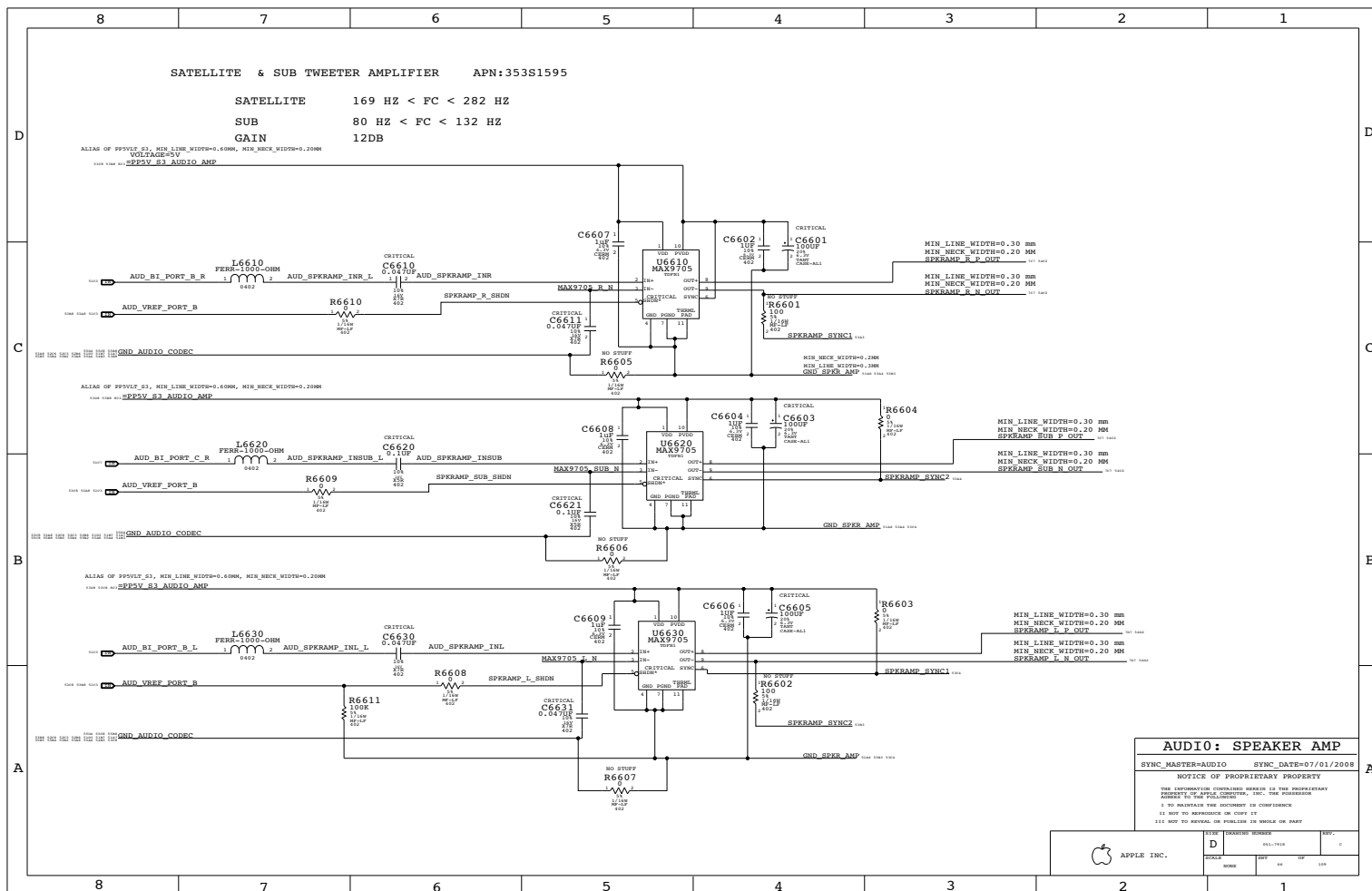
+E (+up) Front of system

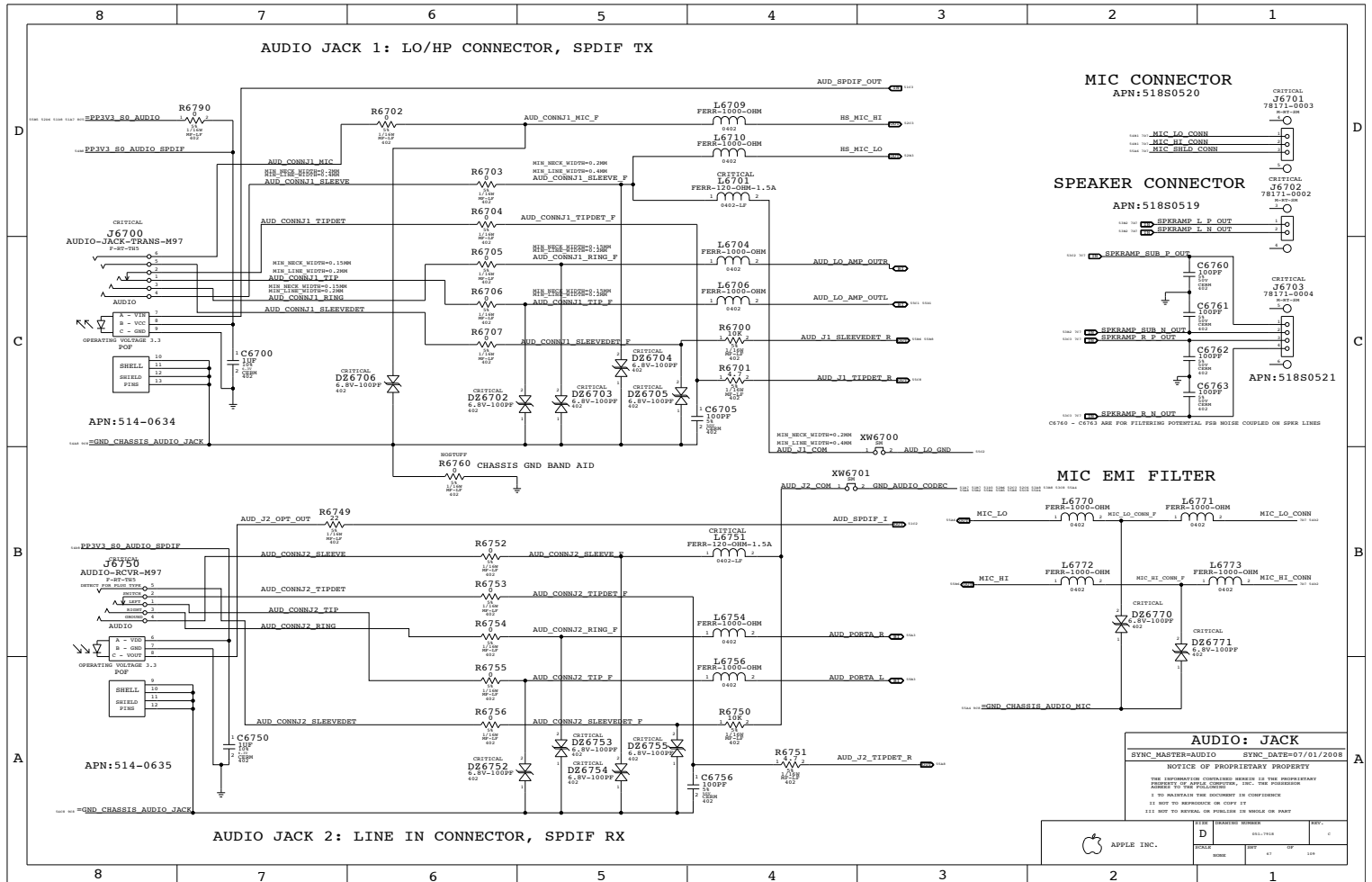
Circle indicates pin 1 location when placed in correct orientation

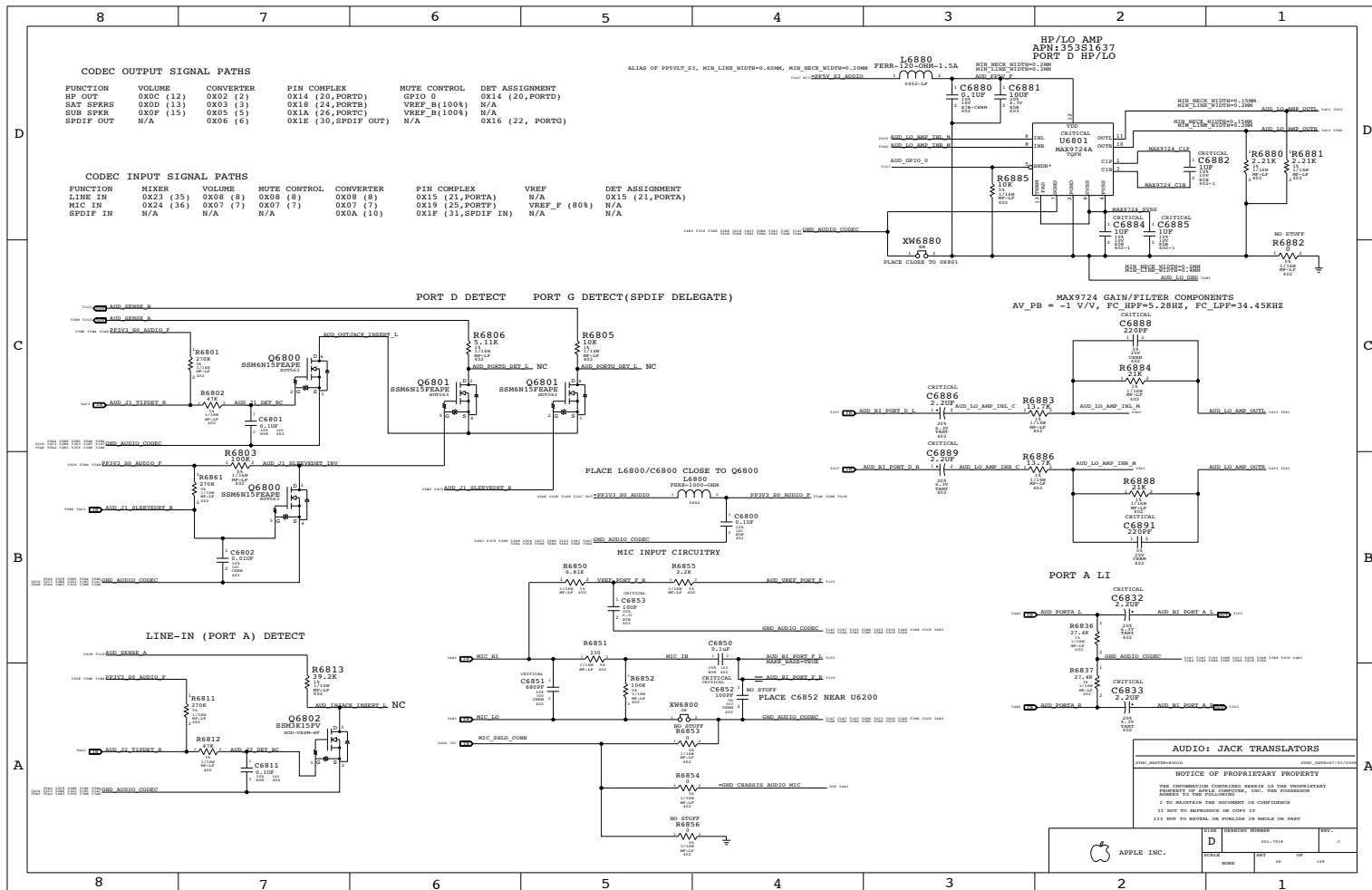
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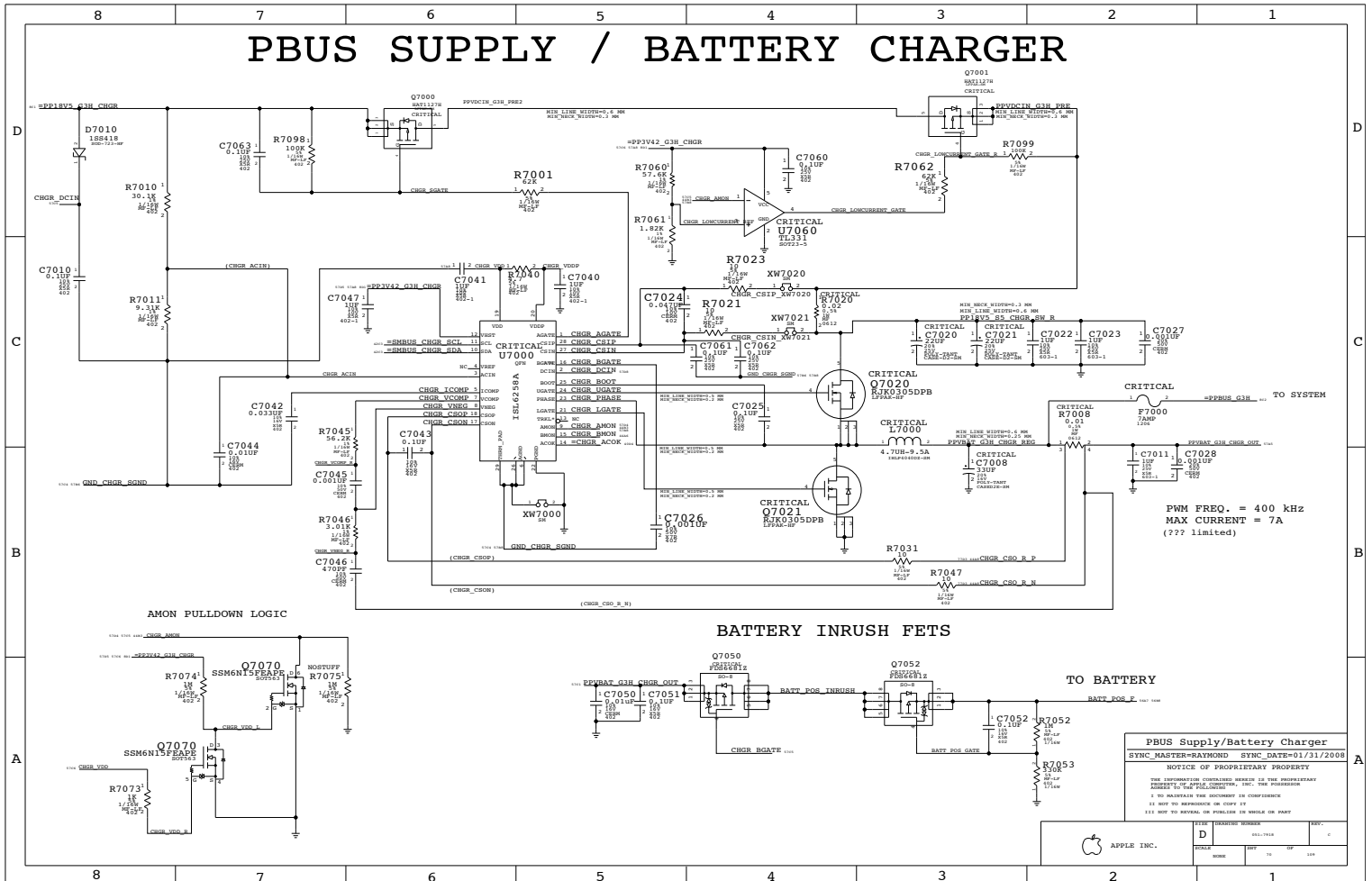
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ITEM D	SEARCHED INDEXED 061-7910	SER. C	
FILED	MADE	BY	OF
	NAME	NO	100







PBUS SUPPLY / BATTERY CHARGER



5V_RT/3.3V POWER SUPPLY

$V_{OUT} = (2 * R_A / R_B) + 2$ $V_{OUT} = (2 * R_C / R_D) + 2$

ROUTING NOTE:
Place XW7203 by Pin1 of L7260.
Place XW7204 by Pin2 of L7220.
Place XW7205 by CT252.

ROUTING NOTE:
Place XW7204 by Pin2 of L7220.
Place XW7205 by CT252.

ROUTING NOTE:
Place XW7201 between Pin 15 and Pin 25 of U7200.

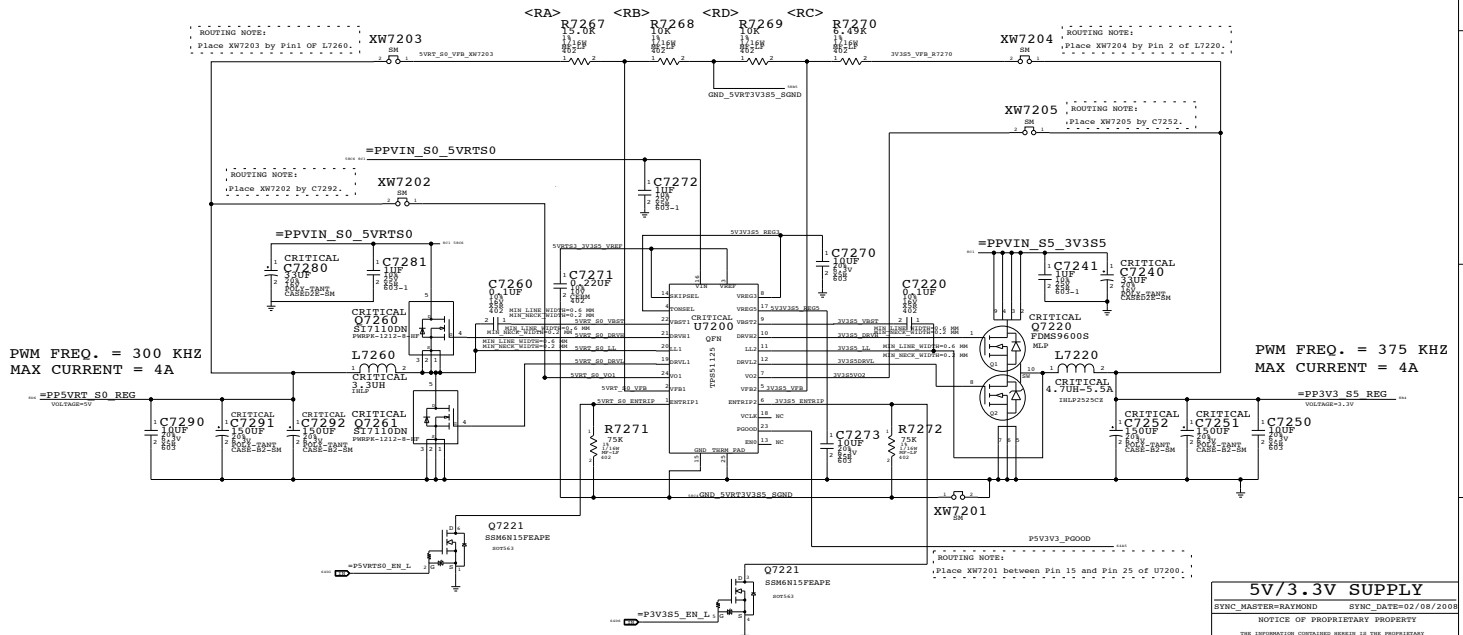
5V/3.3V SUPPLY
SYNC_MASTER=RAYMOND SYNC_DATE=02/08/2008
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SEPARATED MASTER P0000 FOR B000 1V AND 3V2.

APPLE INC.

REV	DATE	BY	CHK	APP	DATE
D	02/10/08				

$$V_{OUT} = (2 * RC / RD) + 2$$



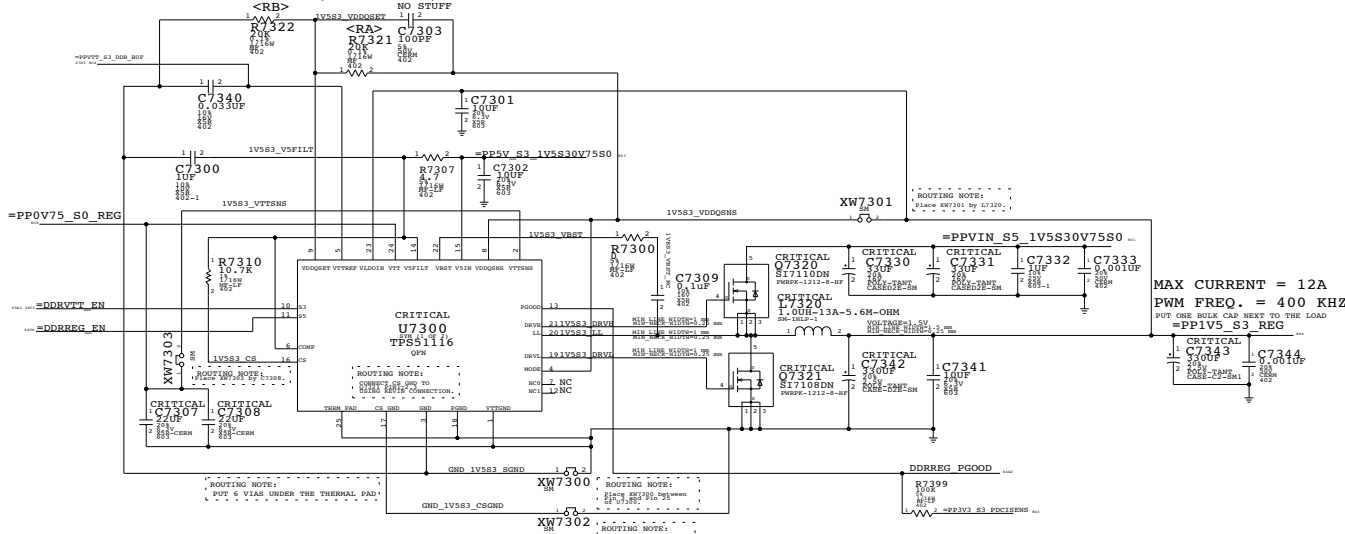
PWM FREQ. = 375 KHZ
MAX CURRENT = 4A

SEPERATED MASTER PGOOD FOR BOTH 5V AND 3V3.

5V/3.3V SUPPLY			
SYNC_MASTER=RAYMOND		SYNC_DATE=02/08/2008	
NOTICE OF PROPRIETARY PROPERTY			
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3. NOT TO REPRODUCE OR PUBLISH IN WHOLE OR PART			
TYPE	ISSUED NUMBER	REV.	
D	481/7918	C	
SCALE	REV	OF	TOT
NONE	73	100	

1.5V/0.75V(DDR3) POWER SUPPLY

$$V_{OUT} = 0.75V * (1 + R_A / R_B)$$



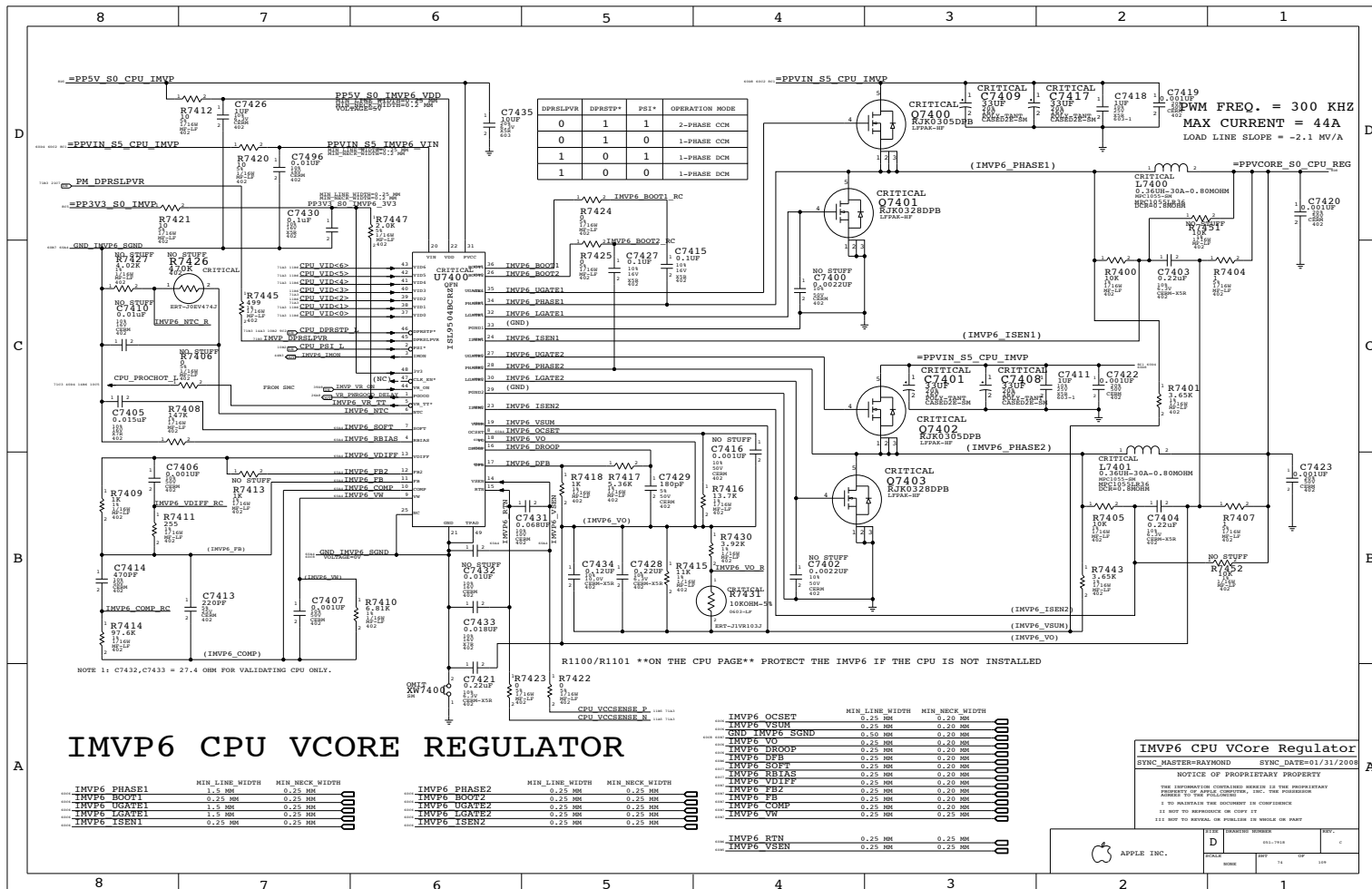
STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

1.5V/0.75V DDR3 SUPPLY

SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

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APPLE INC.	DATE	REV	1.0	1.0
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MCP VCORE/5V_S3 LEFT REGULATOR

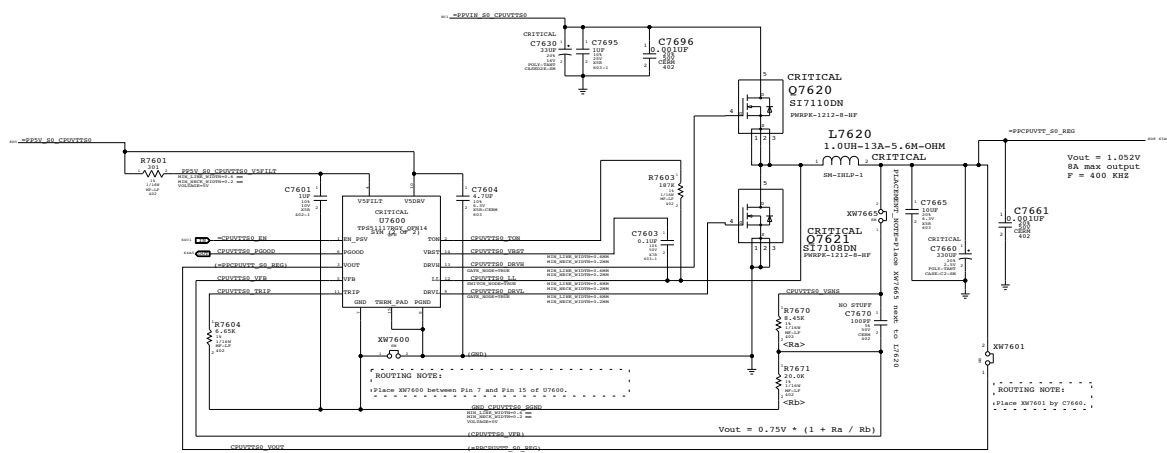
PCP7 Rev A01 requires higher core & analog voltages					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
1450183	1	RES, 0W, 1/4W, 100K, 1%, 0.605, 0.400, 0.50	R7570		PCP_A01
1450184	1	RES, 0W, 1/4W, 100K, 1%, 0.605, 0.400, 0.50	R7571		PCP_A01
1450404	1	RES, 0W, 1/4W, 100K, 1%, 0.605, 0.400, 0.50	R7580		PCP_A01
1450404	1	RES, 0W, 1/4W, 100K, 1%, 0.605, 0.400, 0.50	R7581		PCP_A01
1450423	1	RES, 0W, 1/4W, 100K, 1%, 0.605, 0.400, 0.50	R7582		PCP_A01
1450273	1	RES, 0W, 1/4W, 100K, 1%, 0.605, 0.400, 0.50	R7576		PCP_A01ANDPCP_A010
1450404	1	RES, 0W, 1/4W, 100K, 1%, 0.605, 0.400, 0.50	R7571		PCP_A01ANDPCP_A010
1450404	1	RES, 0W, 1/4W, 100K, 1%, 0.605, 0.400, 0.50	R7570		PCP_A01ANDPCP_A010
1450447	1	RES, 0W, 1/4W, 100K, 1%, 0.605, 0.400, 0.50	R7581		PCP_A01ANDPCP_A010
1450447	1	RES, 0W, 1/4W, 100K, 1%, 0.605, 0.400, 0.50	R7582		PCP_A01ANDPCP_A010

VID<2:0>	Rev A01	Production	
	Voltage	Voltage	%CP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

M97 DIFFERENCES FROM LAST SYNC ON 12/05/07 TO T18 MLD:
 Added C7568 bulk cap on output.
 Tied TOW to REF.
 Changed Q7510 to 376506674.
 C7560 changed to 13850638.
 L7560 changed from T18 MLD inductor to 15250782.
 Changed Q7565 to 376506637.
 Changed R7514 to 280K. R7564 to 180K.

MCP VCORE REGULATOR			
25VC_MASTER=KATKIND		25VC_DATE=01/31/2008	
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TYPE	ISSUING NUMBER	REV.	
D	001-7910	C	
SCALE	DATE	OF	PAGES
		75	109

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[illegible]

CPU VTT(1.05V) SUPPLY	
SYNC_MASTER=RAYMOND	SYNC_DATE=02/08/2008

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DATE D	GRANTING NUMBER 001-7918	REV. C
SCALE NONE	ENV 76	OP 100

[illegible]

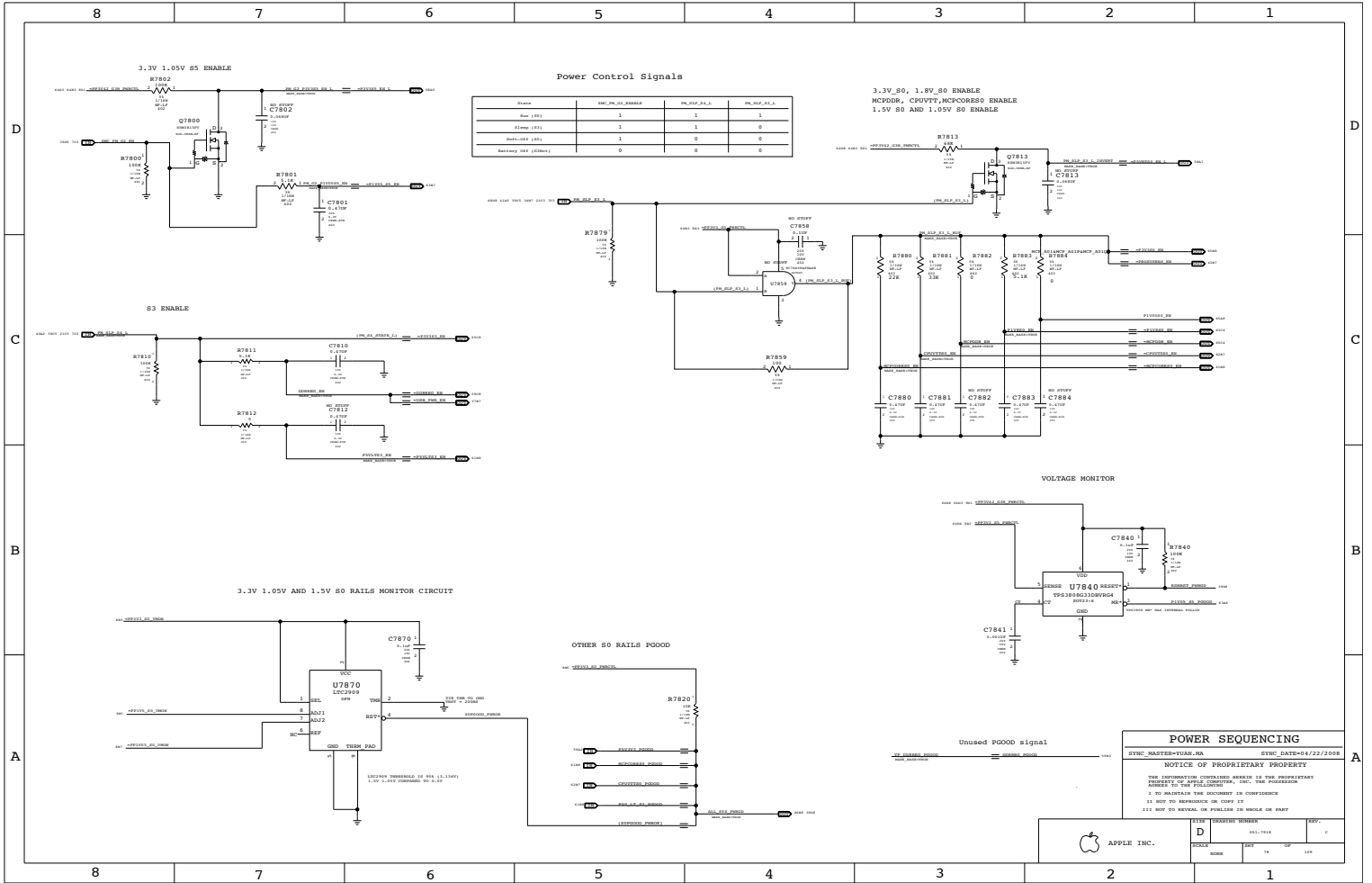
MCP79 Rev A01 requires higher voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11480464	1	RES,MTL FILM,1/16W,300K,1%,0002,SMD,LF	R7781	MCP	A01&MCP_A01P&MCP_A01Q

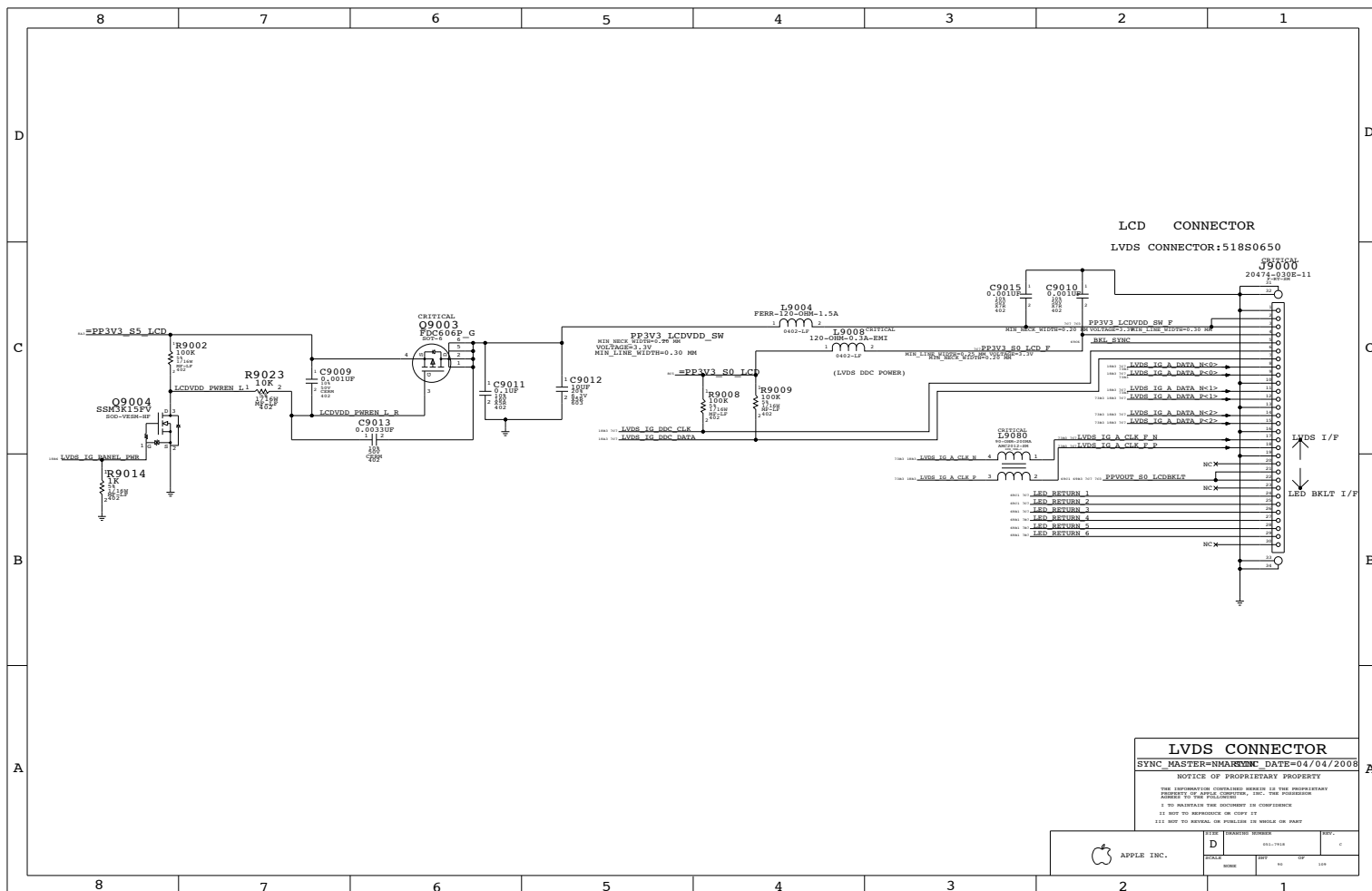
VOUT = 1.102V

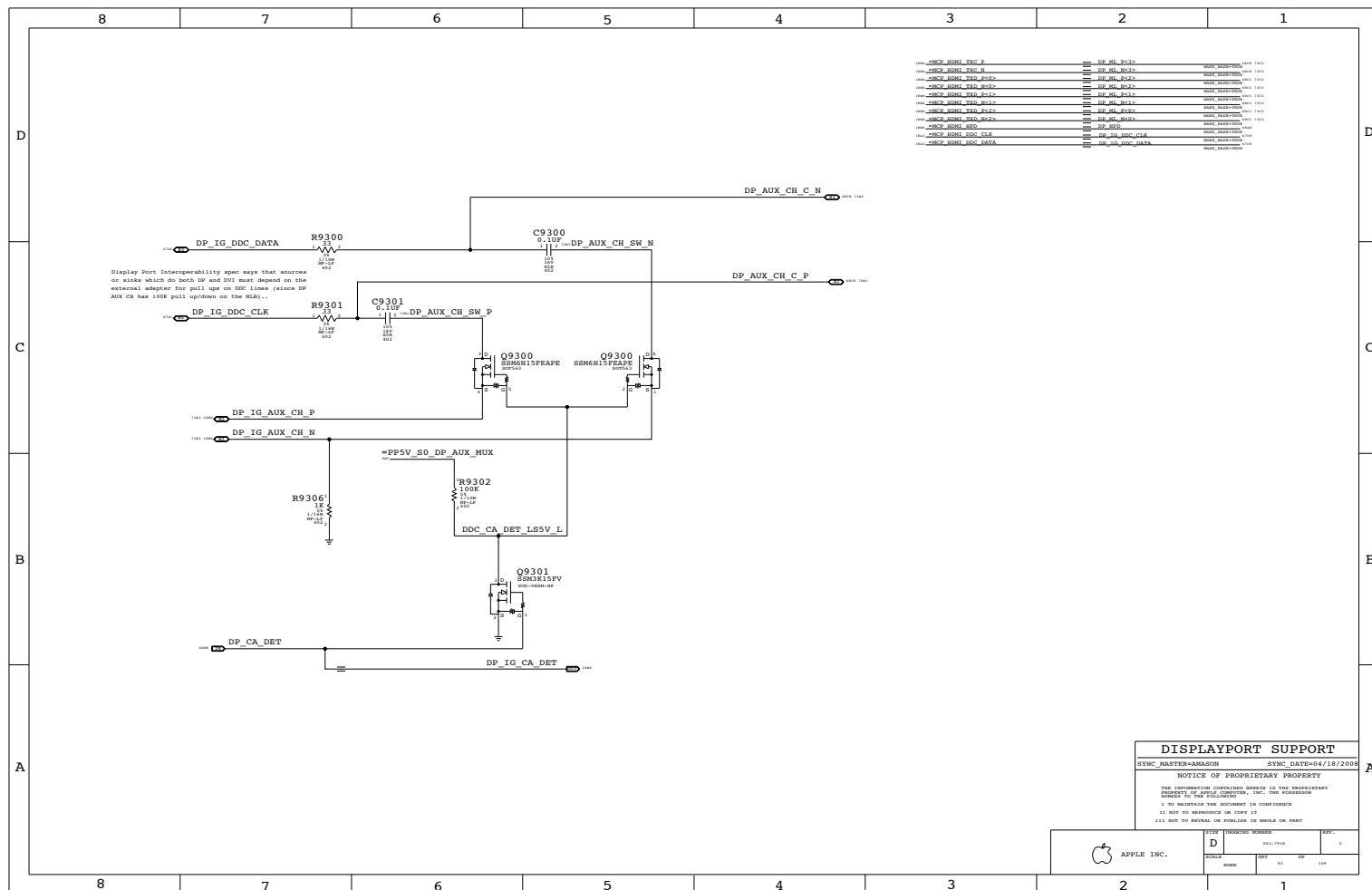
MISC POWER SUPPLIES	
SYNC_MASTER=RAYMOND	SYNC_DATE=01/23/2008
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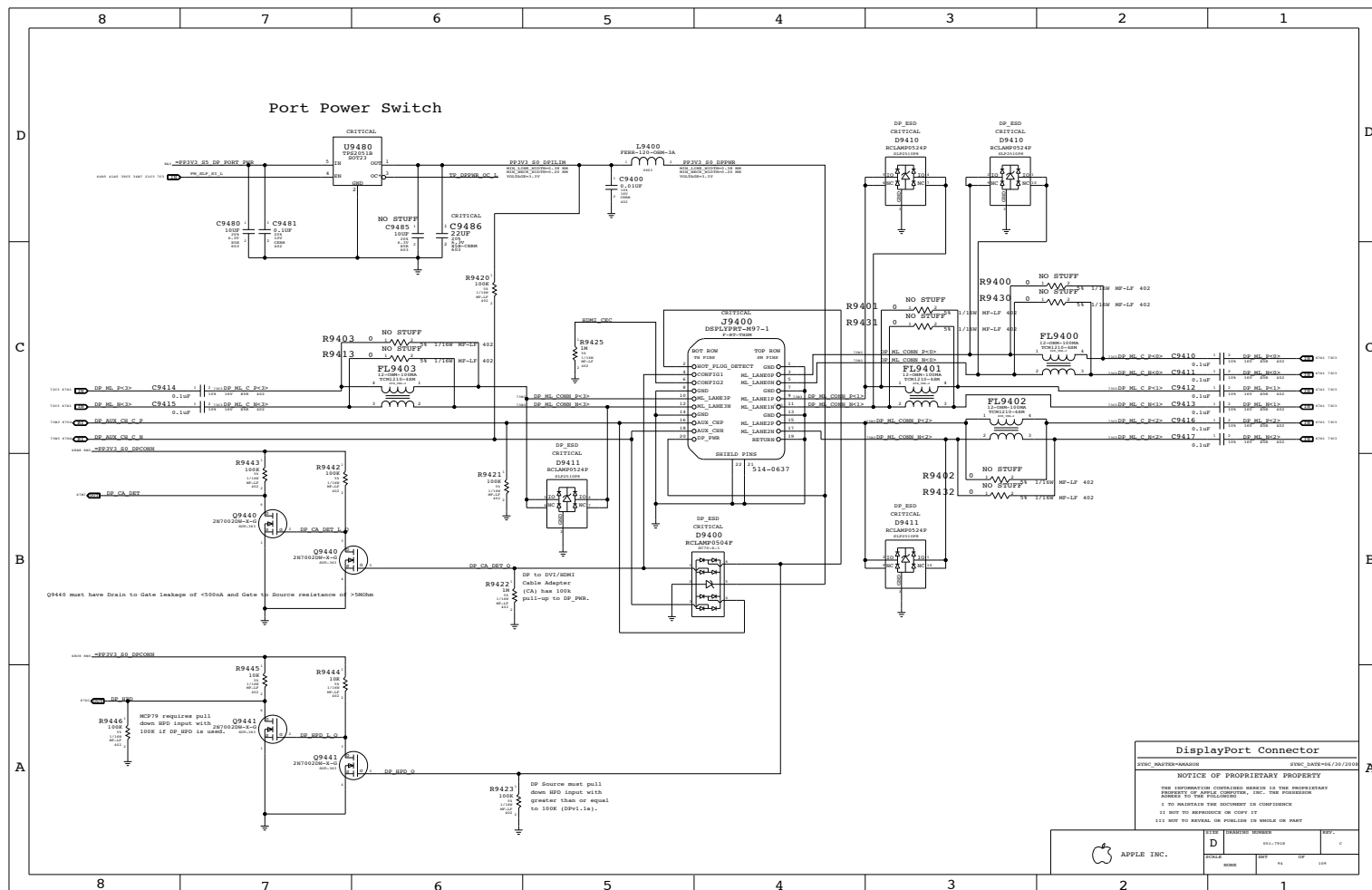
 APPLE INC.	ITEM D	DRAWING NUMBER 001.7910	REV. C
	SCALE NONE	HWY OF 77 100	

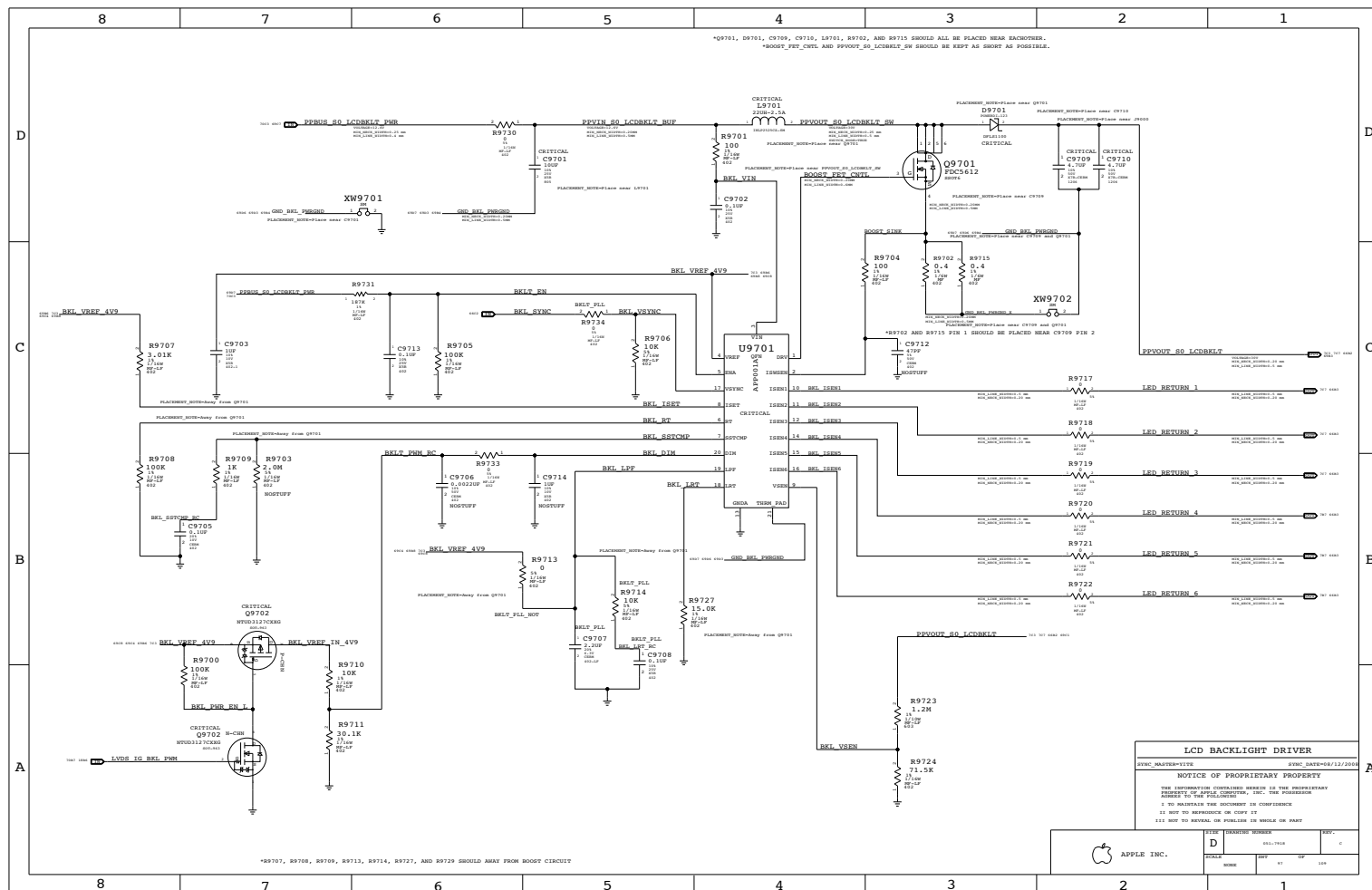


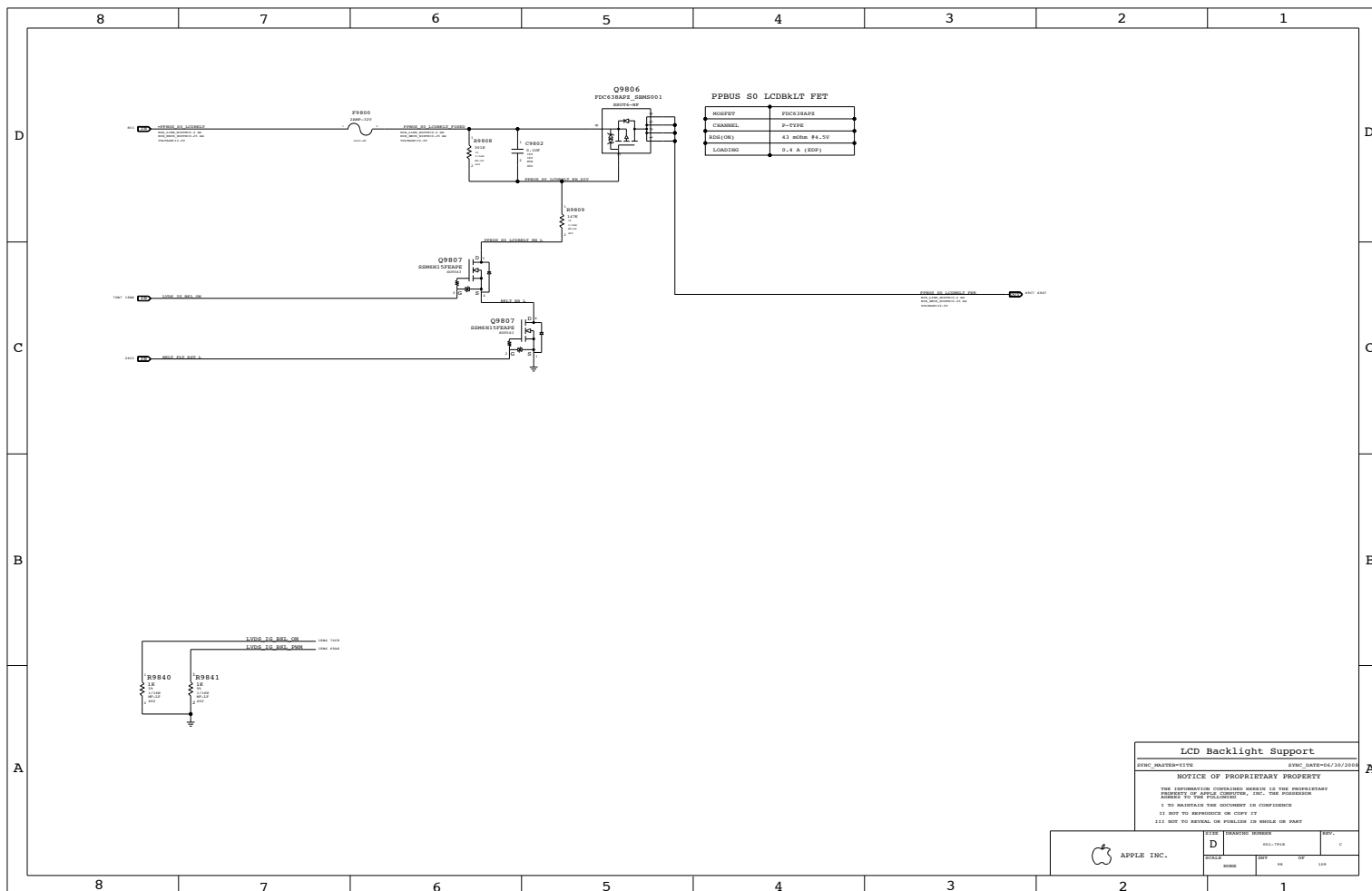












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PCI-Express																															
PROTOCOL_ROLE_KEY				LAYER				SOURCE_ROLE_KEY				REVISION_ROLE_KEY				MAXIMUM_ROLE_LENGTH				DIFFERENTIAL_PAIRING_KEY				DIFFERENTIAL_PAIRING_KEY							
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