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TECHNICAL DATA

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MCM4164CP

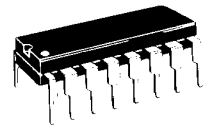
64K Bit Dynamic RAM

The MCM4164CP is a 65,536-bit, high-speed, low-power dynamic Random-Access Memory. It is organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology.

By multiplexing row- and column-address inputs, the MCM4164CP requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM4164CP incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 65,536 Words of 1 Bit
- Single +5 V Operation (±10%)
- Maximum Access Time
  - MCM4164CP15 = 150 ns
  - MCM4164CP20 = 200 ns
- Low Power Dissipation
  - 275 mW Maximum (Active)
  - 22 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- $\overline{RAS}$-Only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4517)
- Fast Page Mode Cycle Time



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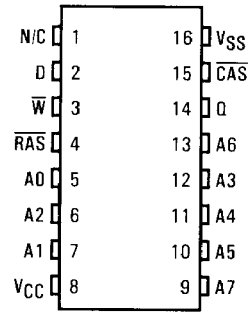
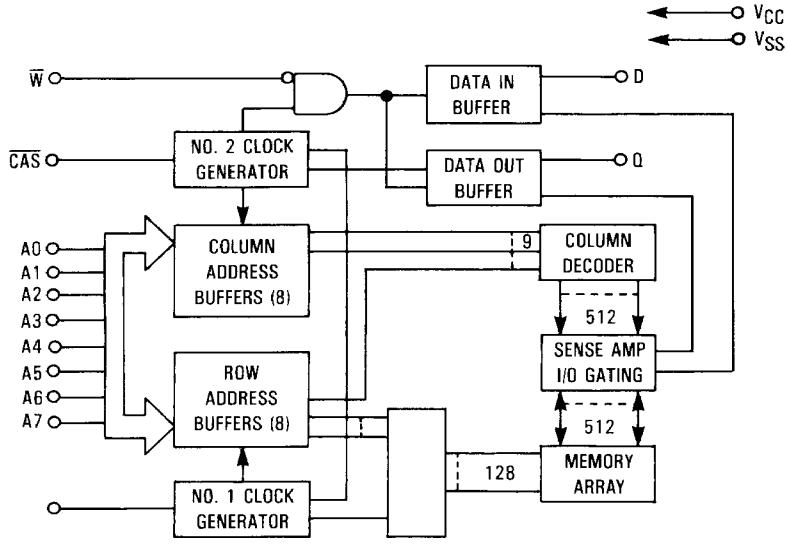
PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

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ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS} (Except V_{CC})	V_{in}, V_{out}	−1 to +7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic 0 Voltage, All Inputs	V_{IL}	−1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current (Standby)	I_{CC2}	—	4.0	mA	5
V_{CC} Power Supply Current ($t_{RC}=t_{RC}$ Min)	I_{CC1}	—	50	mA	4
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles ($t_{RC}=t_{RC}$ Min, $\overline{CAS}$ at Logic 1)	I_{CC3}	—	40	mA	4
V_{CC} Power Supply Current During Page Mode Cycle for $t_{RAS}=10\ \mu s$ ($t_{PC}=t_{PC}$ Min, $\overline{RAS}$ at Logic 0, $\overline{CAS}$ Cycling)	I_{CC4}	—	40	mA	4
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{I(L)}$	−10	10	μA	—
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{O(L)}$	−10	10	μA	—
Output Logic 1 Voltage @ $I_{out}=-5$ mA	V_{OH}	2.4	—	V	—
Output Logic 0 Voltage @ $I_{out}=4.2$ mA	V_{OL}	—	0.4	V	—

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A7), D	C_{I1}	4	5	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8	10	pF	7
Output Capacitance (Q), ($\overline{CAS}=V_{IH}$ to Disable Output)	C_O	5	7	pF	7

NOTES:
1. All voltages referenced to V_{SS}.
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 200 μs is required after power-up followed by an 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
4. Current is a function of cycle rate and output loading; maximum current is measured at the faster cycle rate with the output open.
5. $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C=\frac{I\Delta t}{\Delta V}$.

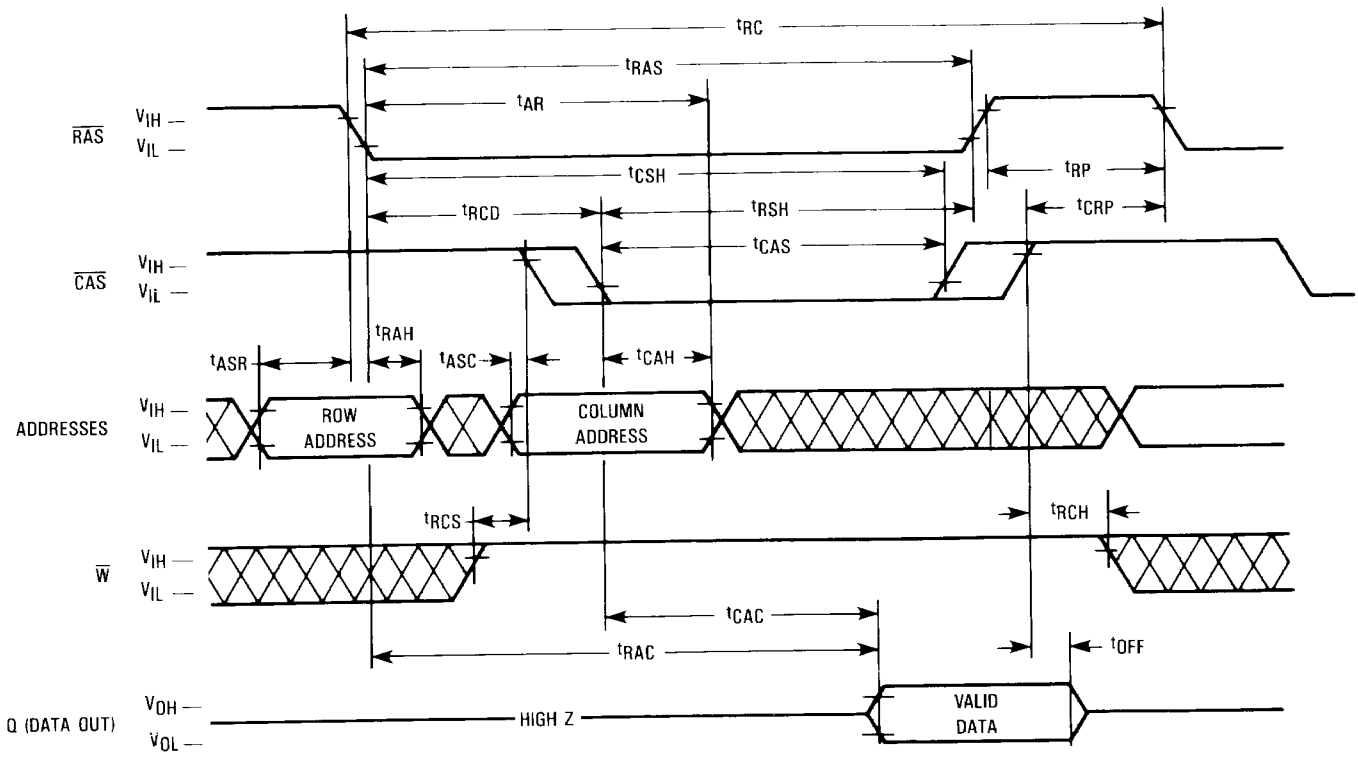
AC OPERATING CONDITIONS AND CHARACTERISTICS (Read, Write, and Read-Modify-Write Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted; See Notes 2, 3, and 6)

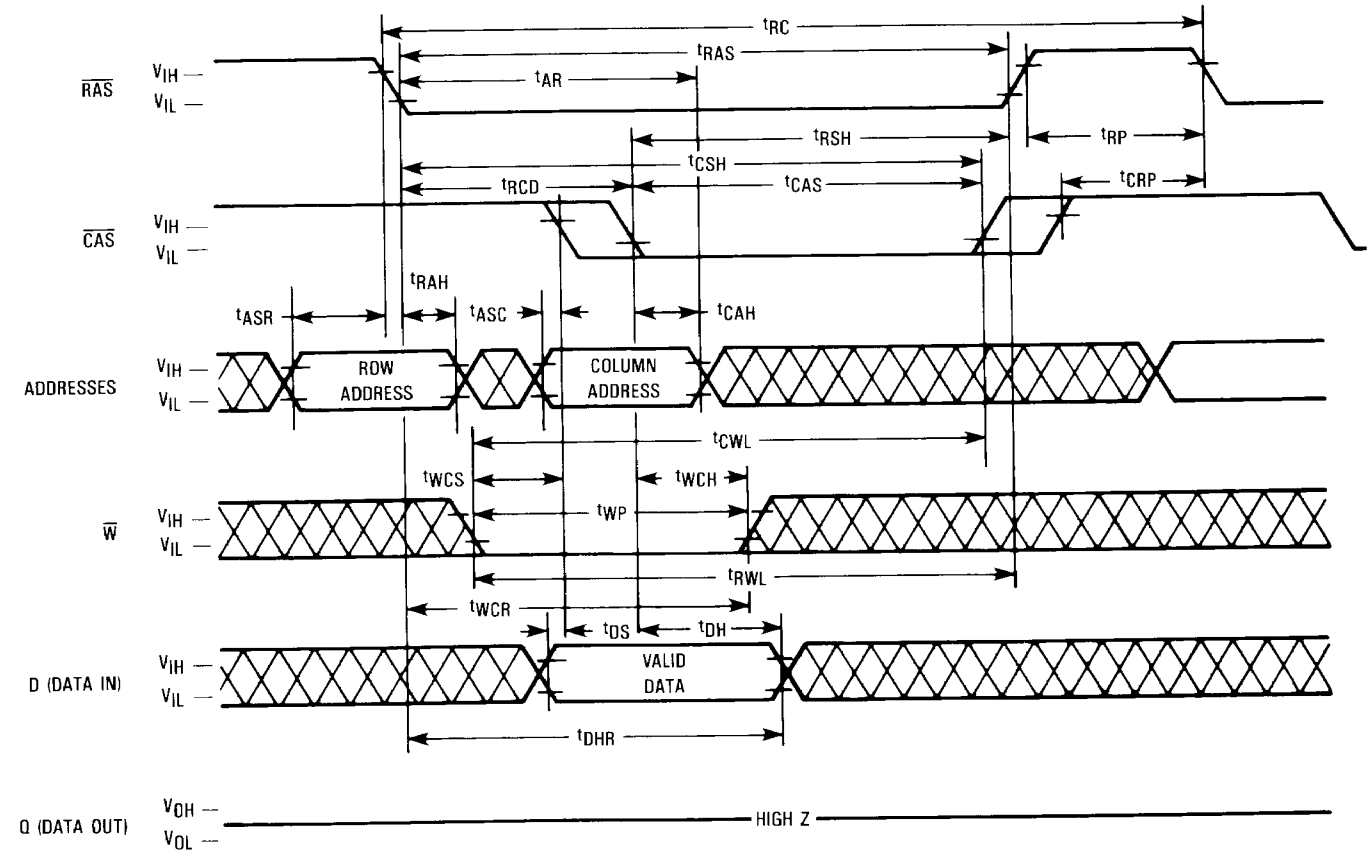
Parameter	Symbol	MCM4164CP15		MCM4164CP20		Unit	Notes
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	270	—	330	—	ns	8, 9
Read Write Cycle Time	t_{RWC}	285	—	350	—	ns	8, 9
Read-Modify-Write Cycle Time	t_{RMW}	310	—	390	—	ns	
Access Time from Row Address Strobe	t_{RAC}	—	150	—	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	—	75	—	100	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	40	0	50	ns	18
Row Address Strobe Precharge Time	t_{RP}	100	—	120	—	ns	
Row Address Strobe Pulse Width	t_{RAS}	150	10,000	200	10,000	ns	
Column Address Strobe Pulse Width	t_{CAS}	75	10,000	100	10,000	ns	
Row to Column Strobe Lead Time	t_{RCD}	25	75	30	100	ns	13
Row Address Setup Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	45	—	55	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	120	—	155	—	ns	17
Transition Time (Rise and Fall)	t_T	3	35	3	50	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	
Write Command Hold Time	t_{WCH}	45	—	55	—	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	120	—	155	—	ns	17
Write Command Pulse Width	t_{WP}	45	—	55	—	ns	
Write Command to Row Strobe Lead Time	t_{RWL}	45	—	55	—	ns	
Write Command to Column Strobe Lead Time	t_{CWL}	45	—	55	—	ns	
Data in Setup Time	t_{DS}	0	—	0	—	ns	15
Data in Hold Time	t_{DH}	45	—	55	—	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	120	—	155	—	ns	17
Column to Row Strobe Precharge Time	t_{CRP}	0	—	0	—	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	75	—	100	—	ns	
Refresh Period	t_{RFSH}	—	2.0	—	2.0	ms	
$\overline{WRITE}$ Command Setup Time	t_{WCS}	0	—	0	—	ns	16
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	50	—	60	—	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	125	—	160	—	ns	16
$\overline{CAS}$ Hold Time	t_{CSH}	150	—	200	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CP}	60	—	80	—	ns	
Page Mode Cycle Time	t_{PC}	145	—	200	—	ns	

8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
9. AC measurements $t_T = 5.0$ ns.
10. Assumes that $t_{RCD} \le t_{RCD}$ (max).
11. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
12. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \ge t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \ge t_{CWD}$ (min) and $t_{RWD} \ge t_{RWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. $t_{AR\ min} \le t_{AR} = t_{RCD} + t_{CAH}$
    $t_{DHR\ min} \le t_{DHR} = t_{RCD} + t_{DH}$
    $t_{WCR\ min} \le t_{WCR} = t_{RCD} + t_{WCH}$
18. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

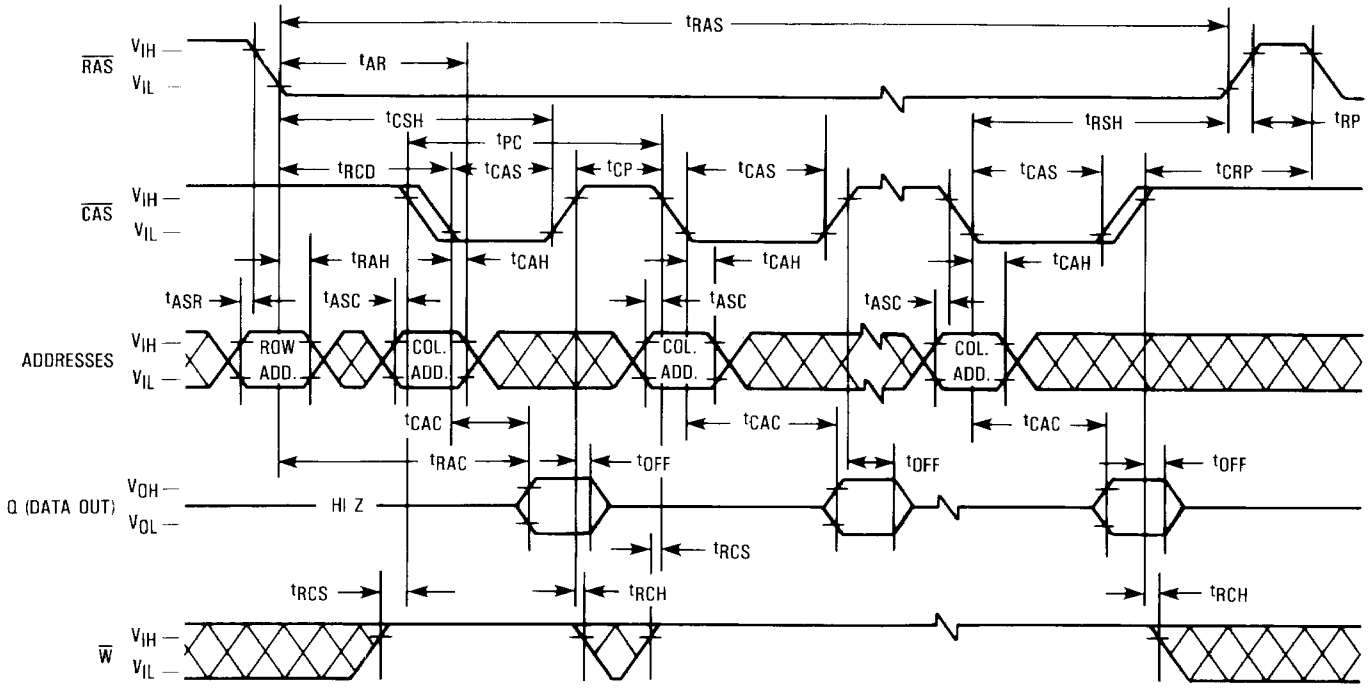
READ CYCLE TIMING



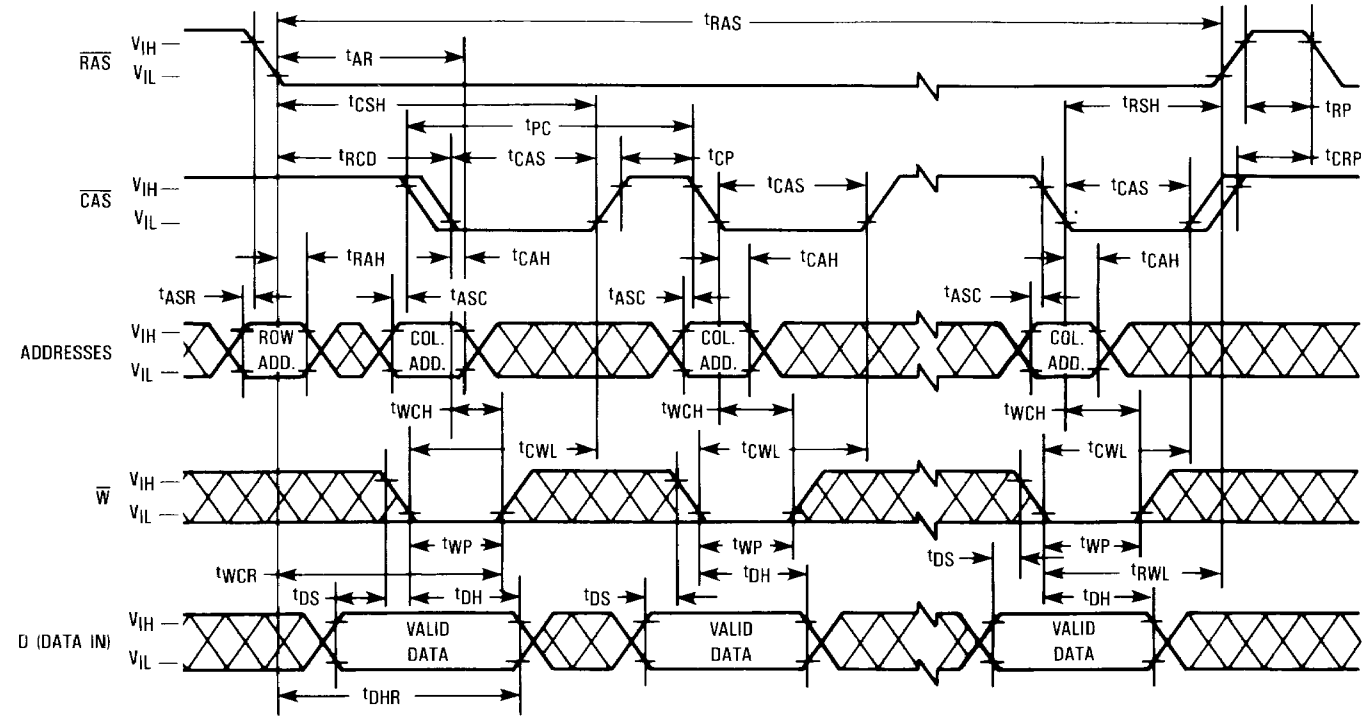
WRITE CYCLE TIMING



PAGE MODE READ CYCLE

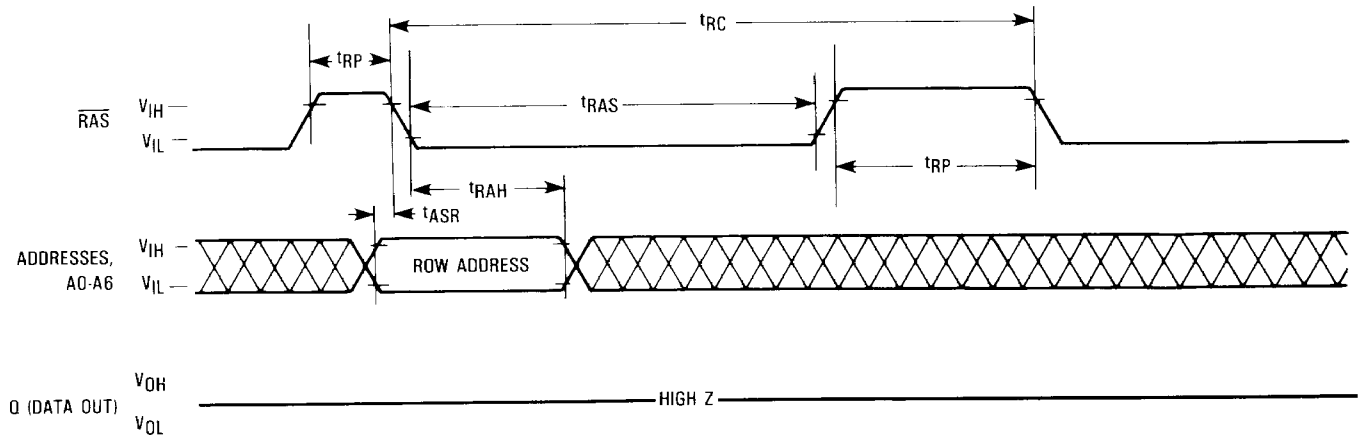


PAGE MODE WRITE CYCLE

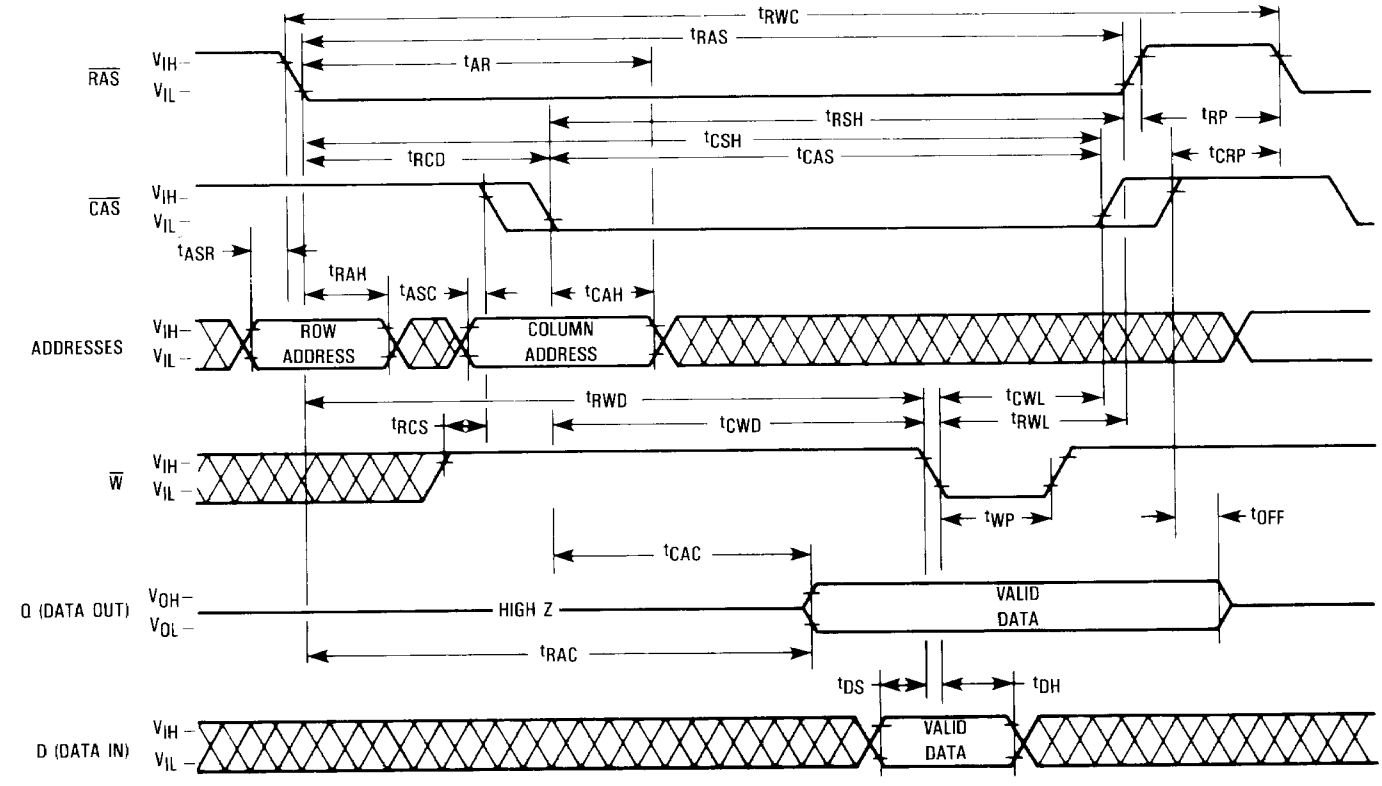


$\overline{RAS}$-ONLY REFRESH CYCLE

(Data-In and $\overline{Write}$ are Don't Care, $\overline{CAS}$ is High)



READ-WRITE/READ-MODIFY-WRITE CYCLE



PACKAGE DIMENSIONS

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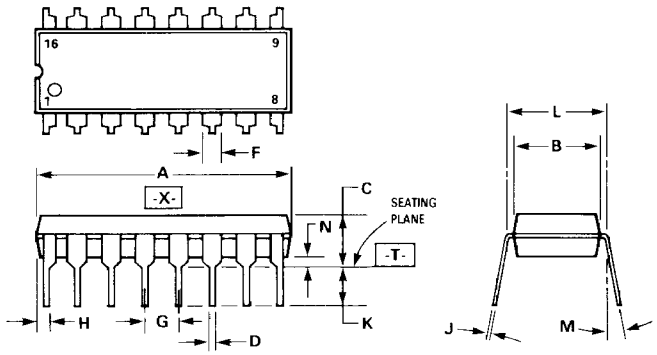
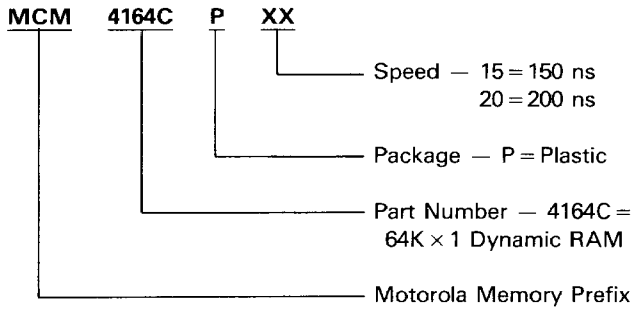


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76 REF		0.030 REF	
J	0.20	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.49	7.75	0.295	0.305
M	0°	10°	0°	10°
N	0.51	1.01	0.020	0.040

NOTES:
1. LEAD POSITIONAL TOLERANCE: ⌀ 0.25 (0.010) M T X M
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. F DIMENSION IS FOR FULL LEADS.
5. ROUNDED CORNERS OPTIONAL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
7. CONTROLLING DIMENSION: INCH.

ORDERING INFORMATION



Full Part Number — MCM4164CP15 or MCM4164CP20

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, the following parameters (t_{RWD}, t_{CWD}) play an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{RWD} or minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{RWD} and t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

PAGE-MODE CYCLES

Page mode operation allows faster successive data operations at the 256 column locations. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 64K dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 8-bit column address field. There are two controlling factors that limit the access to all 256 column locations in one $\overline{RAS}$ clock active operation. These are the refresh interval of the device (2 ms/128 = 15.6 microseconds) and the maximum active time specification for the $\overline{RAS}$ clock (10 microseconds). Since 10 microseconds is the smaller value, the maximum specification of the $\overline{RAS}$ clock on time is the limiting factor of the number of sequential page accesses possible. Ten microseconds will provide approximately (10 microseconds/page mode cycle time) 50 successive page accesses for every row address selected before the $\overline{RAS}$ clock is reset.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{PC}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write or read-while-write type cycle, the conditions normal to that mode of operation will apply in the page mode also. The page mode cycles illustrated show a series of sequential reads separated by a series of sequential writes. This is just one mode of operation. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 2 ms. This is accomplished by sequentially cycling through the 128 row address locations every 2 ms, or at least one row every 15.6 microseconds. A normal read or write operation to the RAM will serve to refresh all the bits (256) associated with that particular row decoded.

$\overline{RAS}$ Only Refresh

When the memory component is in standby the $\overline{RAS}$ only refresh scheme is employed. This refresh method performs a $\overline{RAS}$ only cycle on all 128 row addresses every 2 ms. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and should be inactive or at a V_{IH} level to conserve power.

DEVICE INITIALIZATION

Since the 64K dynamic RAM is a single supply 5 V only device, the need for power supply sequencing is no longer required as was the case in older generation dynamic RAMs. On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 2 ms with device powered up) the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

The row address strobe is the primary "clock" that activates the device and maintains the data when the RAM is in the standby mode. This is the main feature that distinguishes it as a dynamic RAM as opposed to a static RAM. A dynamic RAM is placed in a low power standby mode when the device receives a positive-going row address strobe. The variation in the power dissipation of a dynamic RAM from the active to the standby state is an order of magnitude or more for NMOS devices. This feature is used to its fullest advantage with high density mainframe memory systems, where only a very small percentage of the devices are in the active mode at any one time and the rest of the devices are in the standby mode. Thus, large memory systems can be assembled that dissipate very low power per bit compared to a system where all devices are active continuously.

ADDRESSING THE RAM

The eight address pins on the device are time multiplexed with two separate 8-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe and the column address strobe. A total of sixteen address bits will decode one of the 65,536 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 64K RAM; one is called the page mode cycle (described later) where an 8-bit column address field is presented on the input pins and latched by the $\overline{CAS}$ clock, and the other is the $\overline{RAS}$ only refresh cycle (described later) where a 7-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. In the latter case, the most significant bit on Row Address A7 (pin 9) is not required for refresh.

NORMAL READ CYCLE

A read cycle is referred to as normal read cycle to differentiate it from a page-mode-read cycle, a read-while-write cycle, and read-modify write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available.

This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in is referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds $-$ $[t_{RWL} + t_{RP} + 2t_T]$.

At the start of a write cycle, the data out is in a high-impedance condition and remains inactive throughout the cycle. The data out remains high-impedance because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers. The high-impedance condition of the data out pin during a write cycle can be effectively utilized in a system that has a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.