

SYSTEM BLOCK DIAGRAM

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POWER SYSTEM ARCHITECTURE

The diagram illustrates the power system architecture, showing the flow of power from the AC adapter and battery through various regulators and sequencers to the system components.

Power Sources:

- AC ADAPTER IN (PG 30):** Provides +24V_PBUS and +3V_PMU LDO (PG 31).
- BACKUP BATTERY (PG 31):** Provides +BATT and 14V_PBUS.
- 3S 2P 18650 CELLS:** Provides +BATT.

Regulators and Sequencers:

- INRUSH LIMITER (PG 30):** Protects the AC adapter input.
- BUCK REGULATOR (LTC1625) (PG 31):** Converts +24V_PBUS to +5V_MAIN.
- MAIN 3V/5V DC/DC (LTC3707) (PG 32 STBYMD):** Converts +5V_MAIN to +3V_5V_OK and +3V_MAIN.
- DC/DC (LTC3411) (PG 34):** Converts +3V_MAIN to +1.8V_MAIN (MAXBUS).
- EXT VCC DC/DC (LTC1778) (PG 20):** Converts +5V_MAIN to GPU_VCORE (+1.2V).
- DC/DC (MAX1717) (PG 33):** Converts +5V_MAIN to CPU_VCORE (+1.385V).
- MAX31 DC/DC (MAX1715) (PG 34):** Converts +5V_MAIN to +2.5V_MAIN and +1.5V_MAIN.
- BATTERY CHARGER (MAX1772) (PG 30):** Charges the backup battery.

Timing Diagram:

The timing diagram shows the sequence of events during power-up and shutdown. Key signals include SLEEP, DCDC_EN, DCDC_EN_L, +5V_MAIN, +5V_SLEEP, +3V_MAIN, +3V_SLEEP, 3V_5V_OK, +2_5V_MAIN, +2_5V_SLEEP, +1_5V_MAIN, +1_5V_SLEEP, 1_5V_2_5V_OK (MAX1715 OUTPUT), 1_5V_2_5V_OK (AT LTC1778 RUN/SS), GPU_VCORE (D3HOT), and GPU_VCORE (D3COLD).

POWER BLOCK DIAGRAM

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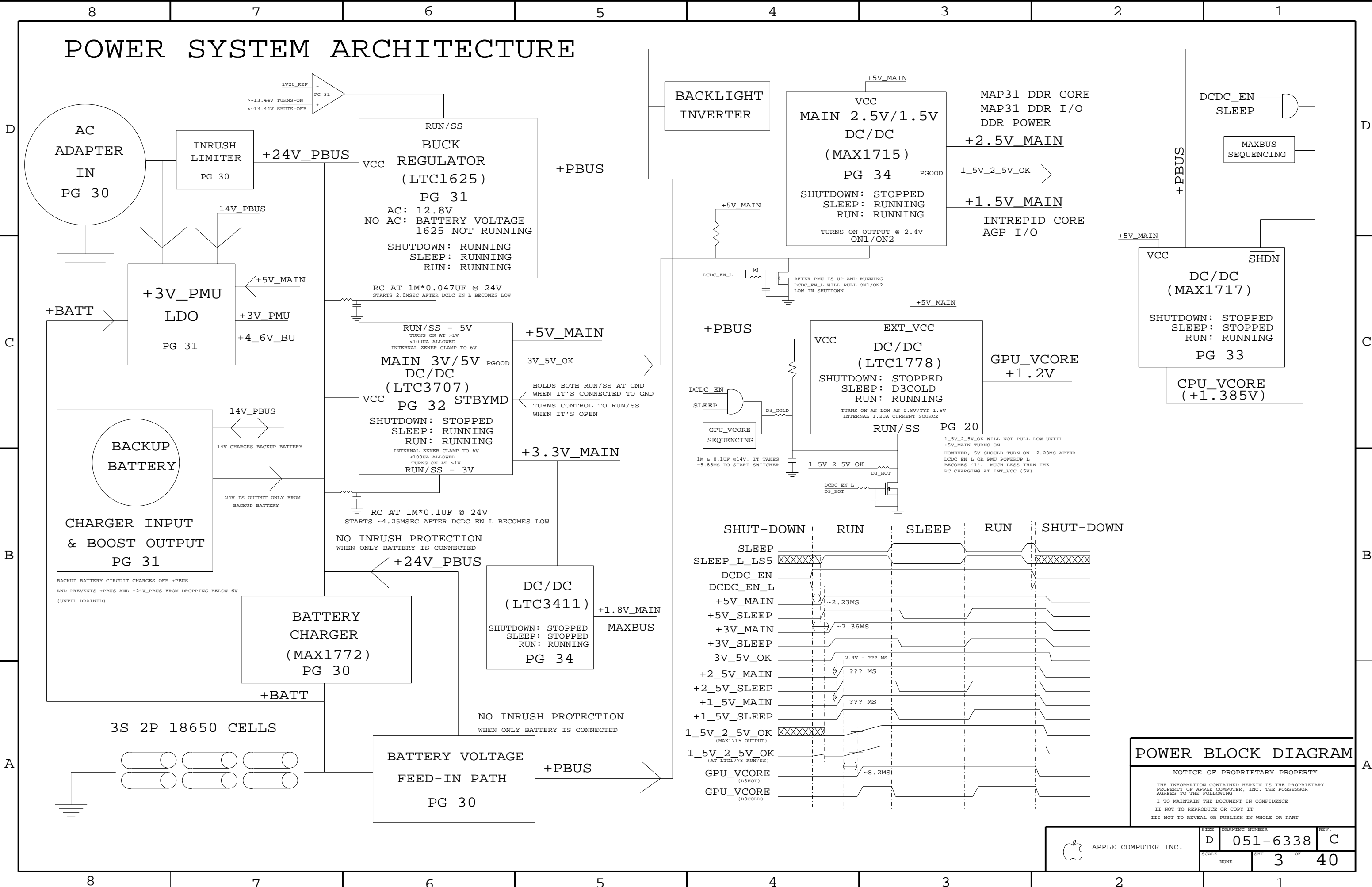
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POWER SYSTEM ARCHITECTURE

The diagram illustrates the power system architecture, showing the flow of power from the AC adapter and battery through various regulators and sequencers to the system components.

Power Sources and Initial Regulation:

- AC ADAPTER IN (PG 30):** Provides +24V_PBUS and +3V_PMU LDO (PG 31).
- BACKUP BATTERY (PG 31):** Provides +BATT, which is charged by the AC adapter and used for the backup battery circuit.
- CHARGER INPUT & BOOST OUTPUT (PG 31):** Manages the backup battery charging and prevents +PBUS and +24V_PBUS from dropping below 6V.
- 3S 2P 18650 CELLS:** Provide +BATT to the BATTERY CHARGER (MAX1772, PG 30) and the BATTERY VOLTAGE FEED-IN PATH (PG 30).

Regulators and Sequencers:

- BUCK REGULATOR (LTC1625, PG 31):** Converts +24V_PBUS to +5V_MAIN. It has a shutdown mode where it runs, sleeps, or runs again.
- DC/DC (LTC3707, PG 32 STBYMD):** Converts +5V_MAIN to +3V_5V_OK and +3V_MAIN. It has a shutdown mode where it stops, sleeps, or runs.
- DC/DC (LTC3411, PG 34):** Converts +3V_MAIN to +1.8V_MAIN. It has a shutdown mode where it stops, sleeps, or runs.
- DC/DC (MAX1715, PG 34):** Converts +5V_MAIN to +2.5V_MAIN and +1.5V_MAIN. It has a shutdown mode where it stops, sleeps, or runs.
- DC/DC (MAX1717, PG 33):** Converts +5V_MAIN to GPU_VCORE (+1.2V) and CPU_VCORE (+1.385V). It has a shutdown mode where it stops, sleeps, or runs.
- GPU_VCORE SEQUENCING:** Manages the GPU_VCORE power-up and shutdown.
- MAXBUS SEQUENCING:** Manages the MAXBUS power-up and shutdown.

Timing Diagram:

The timing diagram shows the sequence of events during power-up and shutdown. The signals are:

- SLEEP
- SLEEP_L_LS5
- DCDC_EN
- DCDC_EN_L
- +5V_MAIN
- +5V_SLEEP
- +3V_MAIN
- +3V_SLEEP
- 3V_5V_OK
- +2_5V_MAIN
- +2_5V_SLEEP
- +1_5V_MAIN
- +1_5V_SLEEP
- 1_5V_2_5V_OK (MAX1715 OUTPUT)
- 1_5V_2_5V_OK (AT LTC1778 RUN/SS)
- GPU_VCORE (D3HOT)
- GPU_VCORE (D3COLD)

The diagram shows the power-up sequence: SLEEP, SLEEP_L_LS5, DCDC_EN, DCDC_EN_L, +5V_MAIN, +5V_SLEEP, +3V_MAIN, +3V_SLEEP, 3V_5V_OK, +2_5V_MAIN, +2_5V_SLEEP, +1_5V_MAIN, +1_5V_SLEEP, 1_5V_2_5V_OK (MAX1715 OUTPUT), 1_5V_2_5V_OK (AT LTC1778 RUN/SS), GPU_VCORE (D3HOT), and GPU_VCORE (D3COLD).

POWER BLOCK DIAGRAM

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POWER SYSTEM ARCHITECTURE

The diagram illustrates the power system architecture, showing the flow of power from the AC adapter and battery through various regulators and sequencers to the system components.

Power Sources:

- AC ADAPTER IN (PG 30):** Provides +24V_PBUS and +3V_PMU LDO (PG 31).
- BACKUP BATTERY (PG 31):** Provides +BATT and +3V_PMU LDO (PG 31).
- 3S 2P 18650 CELLS:** Provides +BATT and BATTERY VOLTAGE FEED-IN PATH (PG 30).

Regulators and Sequencers:

- INRUSH LIMITER (PG 30):** Limits inrush current from the AC adapter.
- BUCK REGULATOR (LTC1625) (PG 31):** Converts +24V_PBUS to +5V_MAIN.
- MAIN 3V/5V DC/DC (LTC3707) (PG 32 STBYMD):** Converts +5V_MAIN to +3V_5V_OK and +3V_MAIN.
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- DC/DC (MAX1717) (PG 33):** Converts +5V_MAIN to CPU_VCORE (+1.385V).
- MAX31 DC/DC (MAX1715) (PG 34):** Converts +5V_MAIN to +2.5V_MAIN and +1.5V_MAIN.
- MAXBUS SEQUENCING:** Controls the power-up and power-down sequence of the system.

Timing Diagram:

The timing diagram shows the power-up and power-down sequence. The signals are: SLEEP, SLEEP_L_LS5, DCDC_EN, DCDC_EN_L, +5V_MAIN, +5V_SLEEP, +3V_MAIN, +3V_SLEEP, 3V_5V_OK, +2_5V_MAIN, +2_5V_SLEEP, +1_5V_MAIN, +1_5V_SLEEP, 1_5V_2_5V_OK (MAX1715 OUTPUT), 1_5V_2_5V_OK (AT LTC1778 RUN/SS), GPU_VCORE (D3HOT), and GPU_VCORE (D3COLD).

POWER BLOCK DIAGRAM

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PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

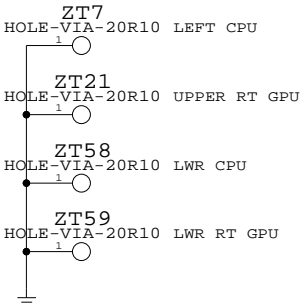
BOARD STACK-UP AND CONSTRUCTION

| 1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA | | | |
|--|-----------------|--|----------------------------------|
| 1 | | | SIGNAL (1/2 OZ + COPPER PLATING) |
| 2 | PREPREG (3 MIL) | | SIGNAL (1/2 OZ) |
| 3 | PREPREG (3 MIL) | | GROUND (1/2 OZ) |
| 4 | CORE (3 MIL) | | SIGNAL (1/2 OZ) |
| 5 | PREPREG (5 MIL) | | CUT POWER PLANE (1 OZ) |
| 6 | CORE (5 MIL) | | CUT POWER PLANE (1 OZ) |
| 7 | PREPREG (5 MIL) | | SIGNAL (1/2 OZ) |
| 8 | CORE (3 MIL) | | GROUND (1/2 OZ) |
| 9 | PREPREG (3 MIL) | | SIGNAL (1/2 OZ) |
| 10 | PREPREG (3 MIL) | | SIGNAL (1/2 OZ + COPPER PLATING) |

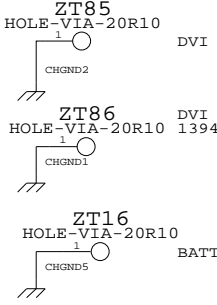
BOARD HOLES

CHASSIS MOUNTS

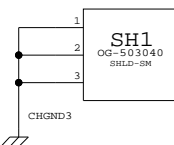
ASICS HEATSINK MOUNTS



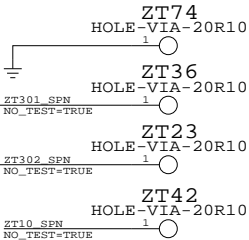
I/O AREA



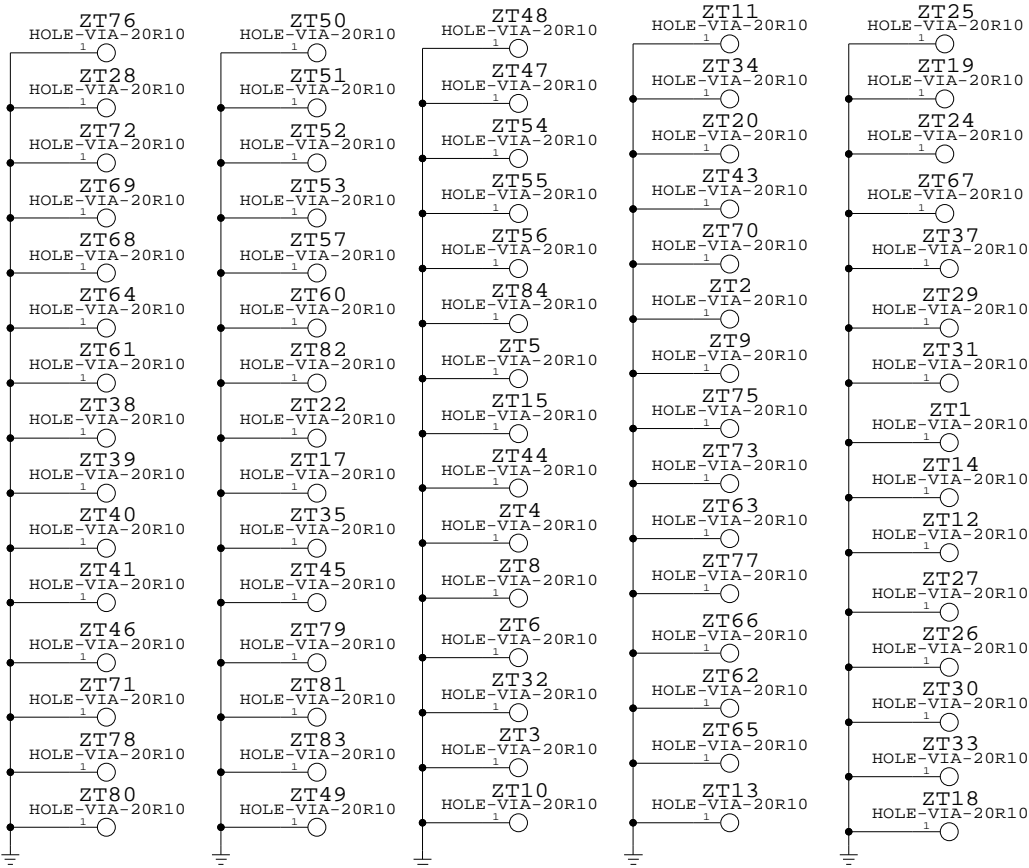
INVERTER



MECH. HOLES



GROUND VIAS



BOARD INFORMATION

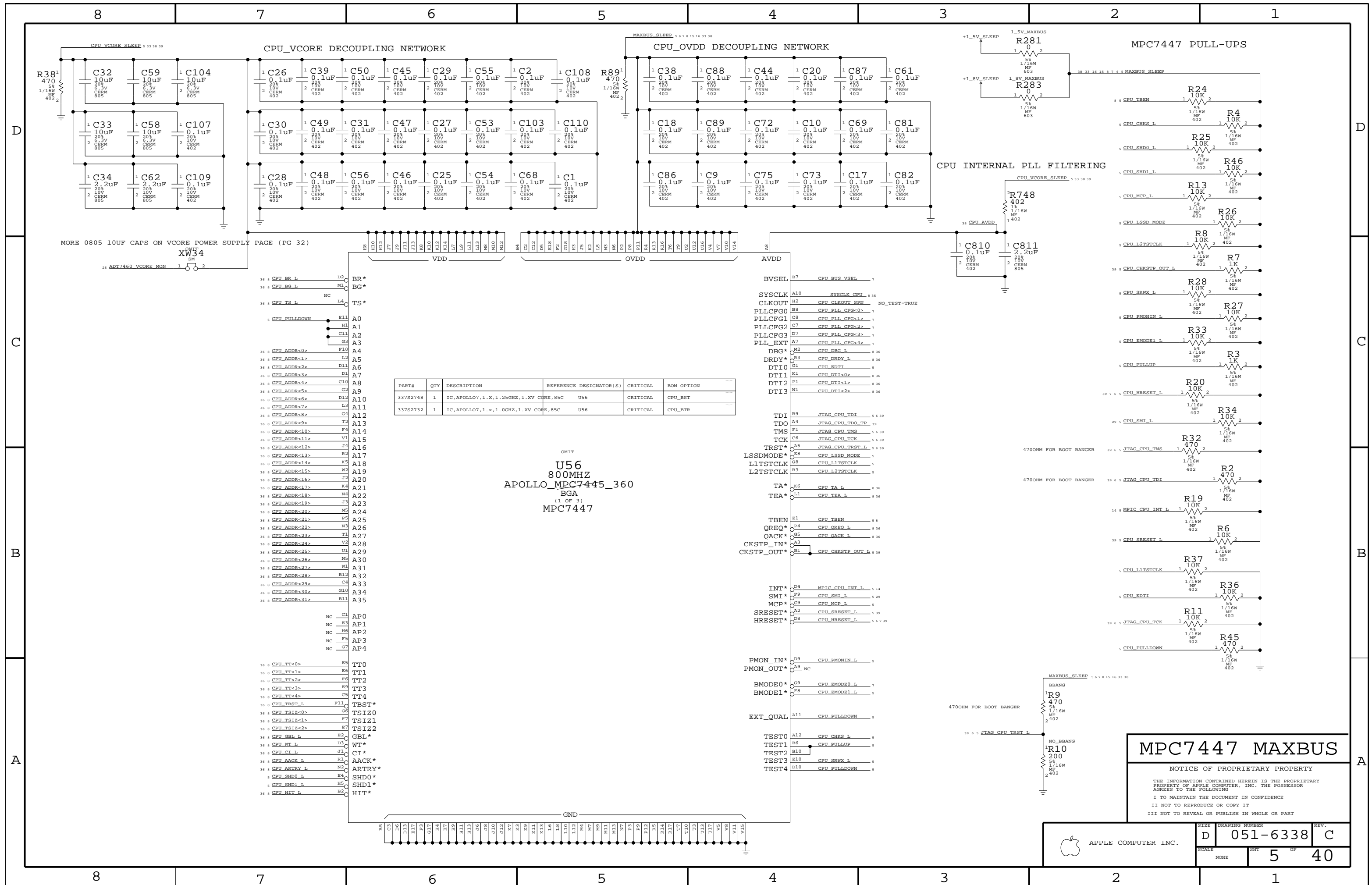
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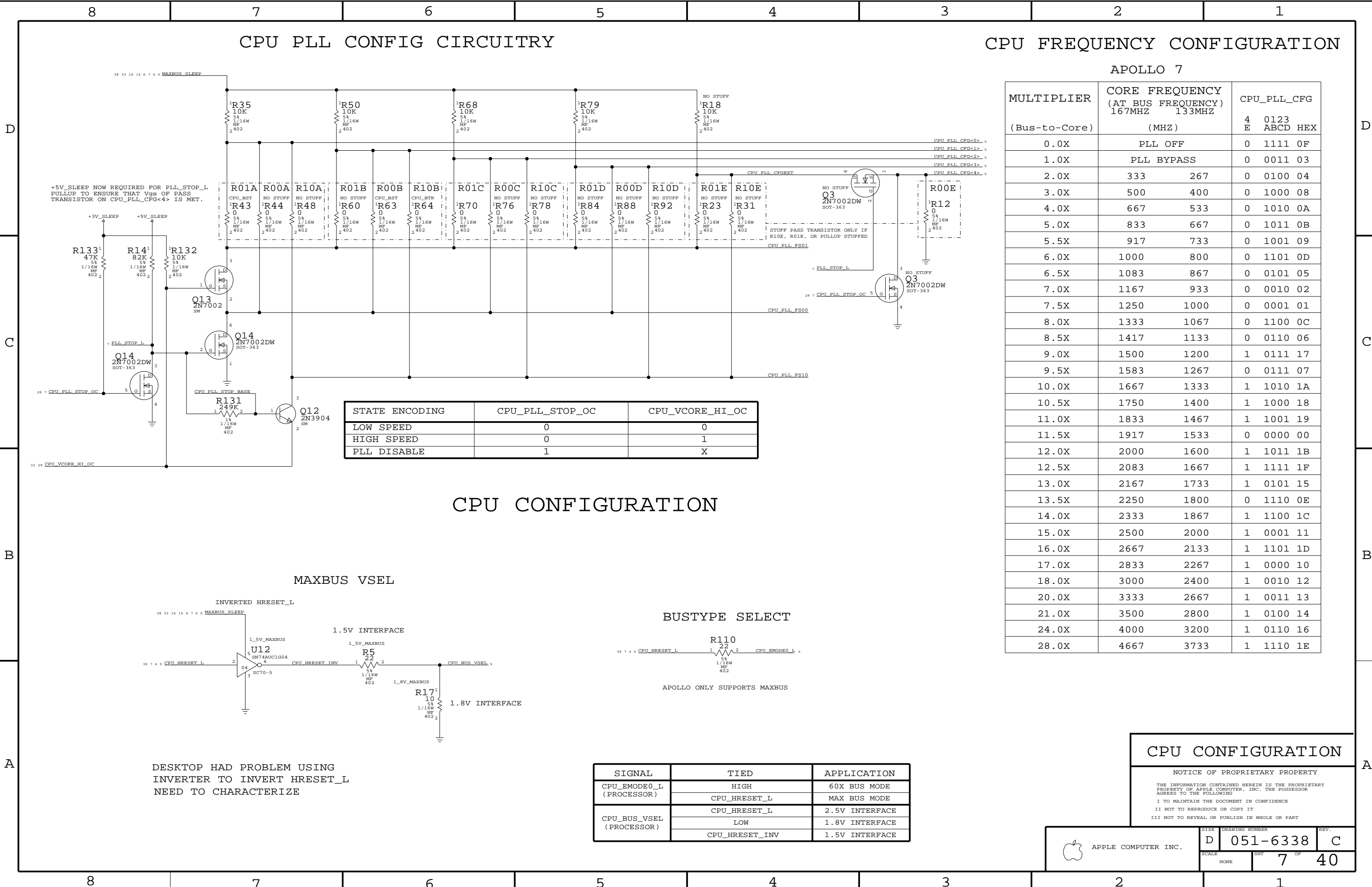
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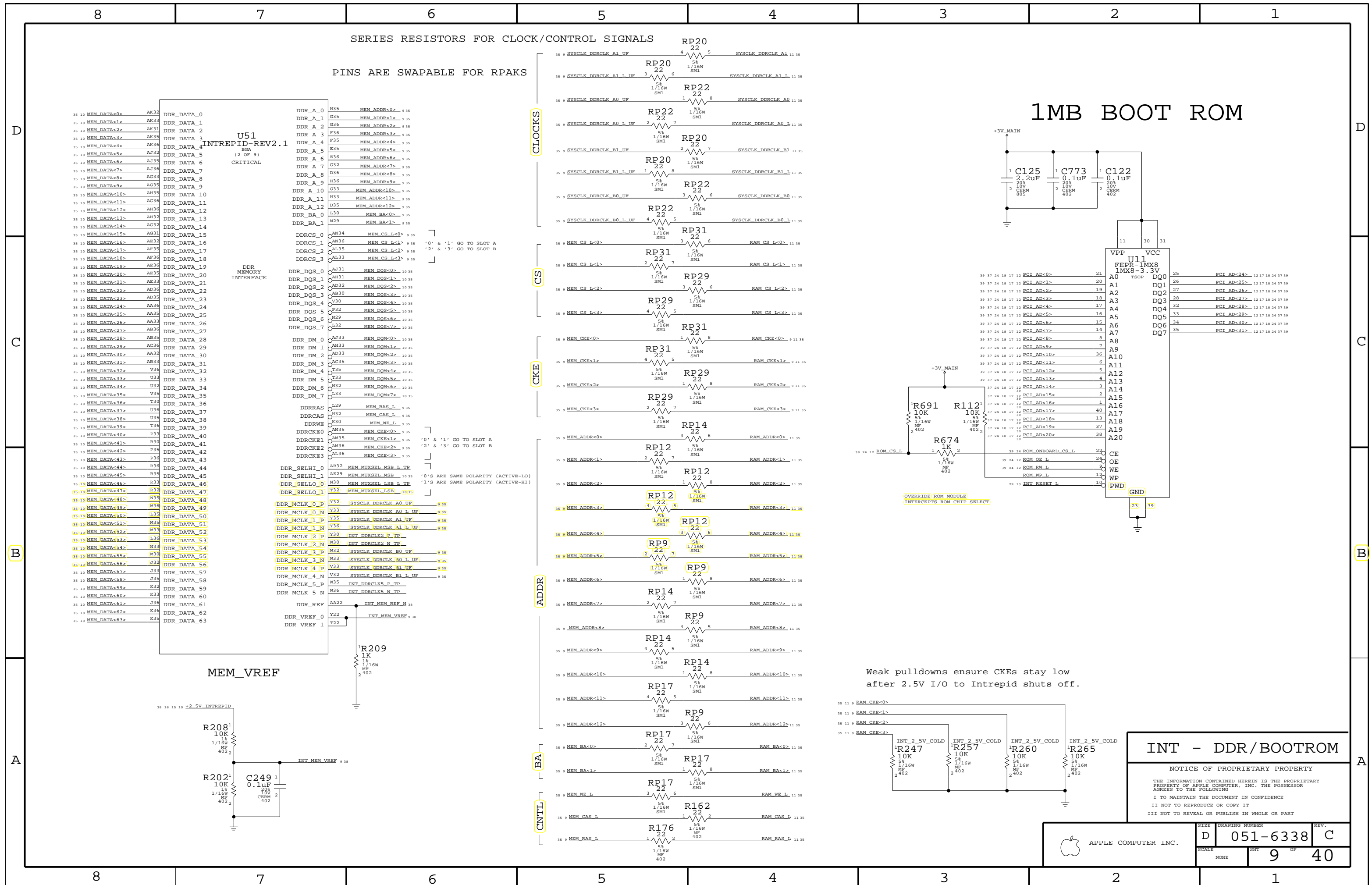


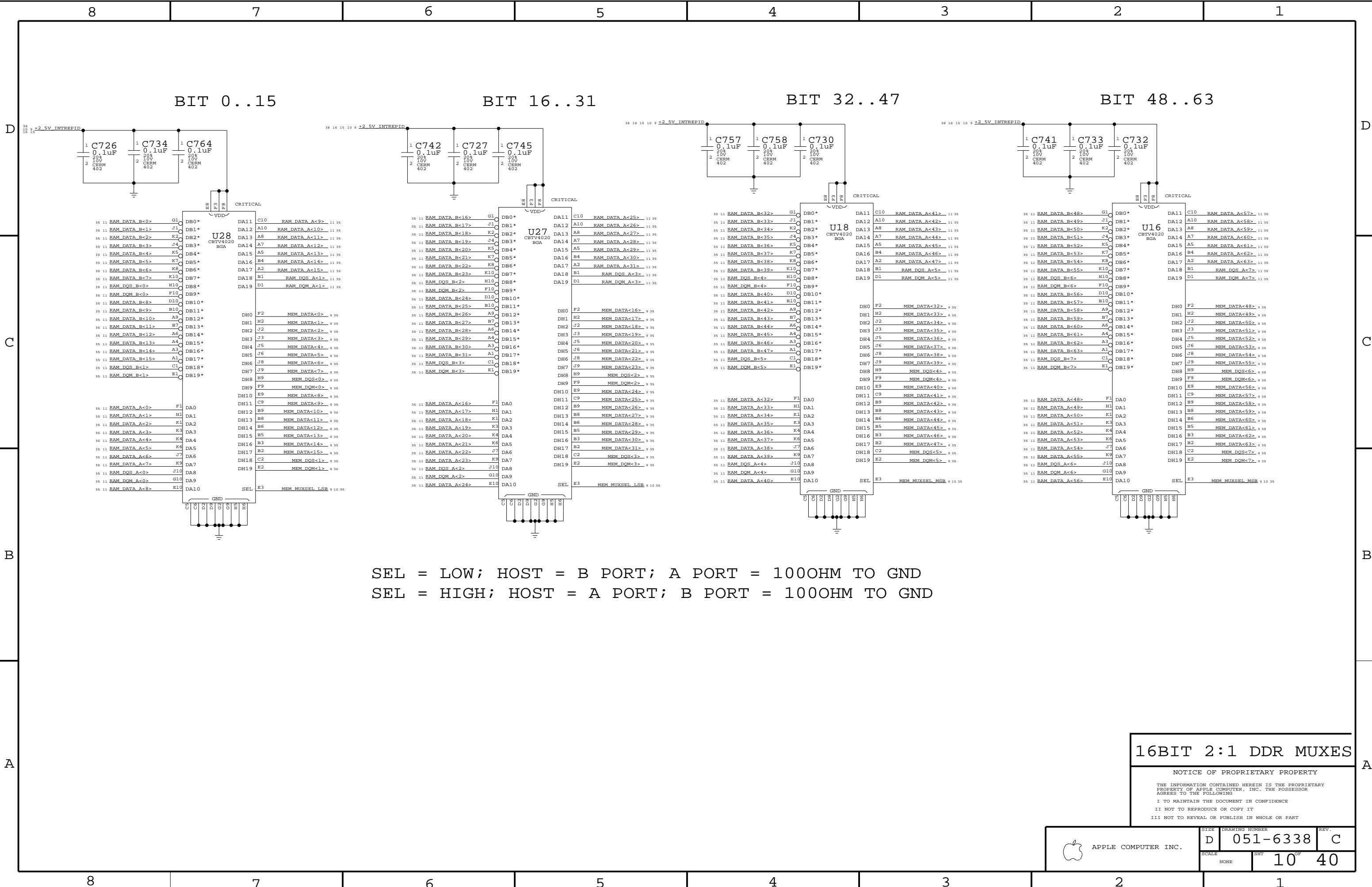
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| D | 051-6338 | C |
| SCALE | SHT | OF |
| NONE | 4 | 40 |









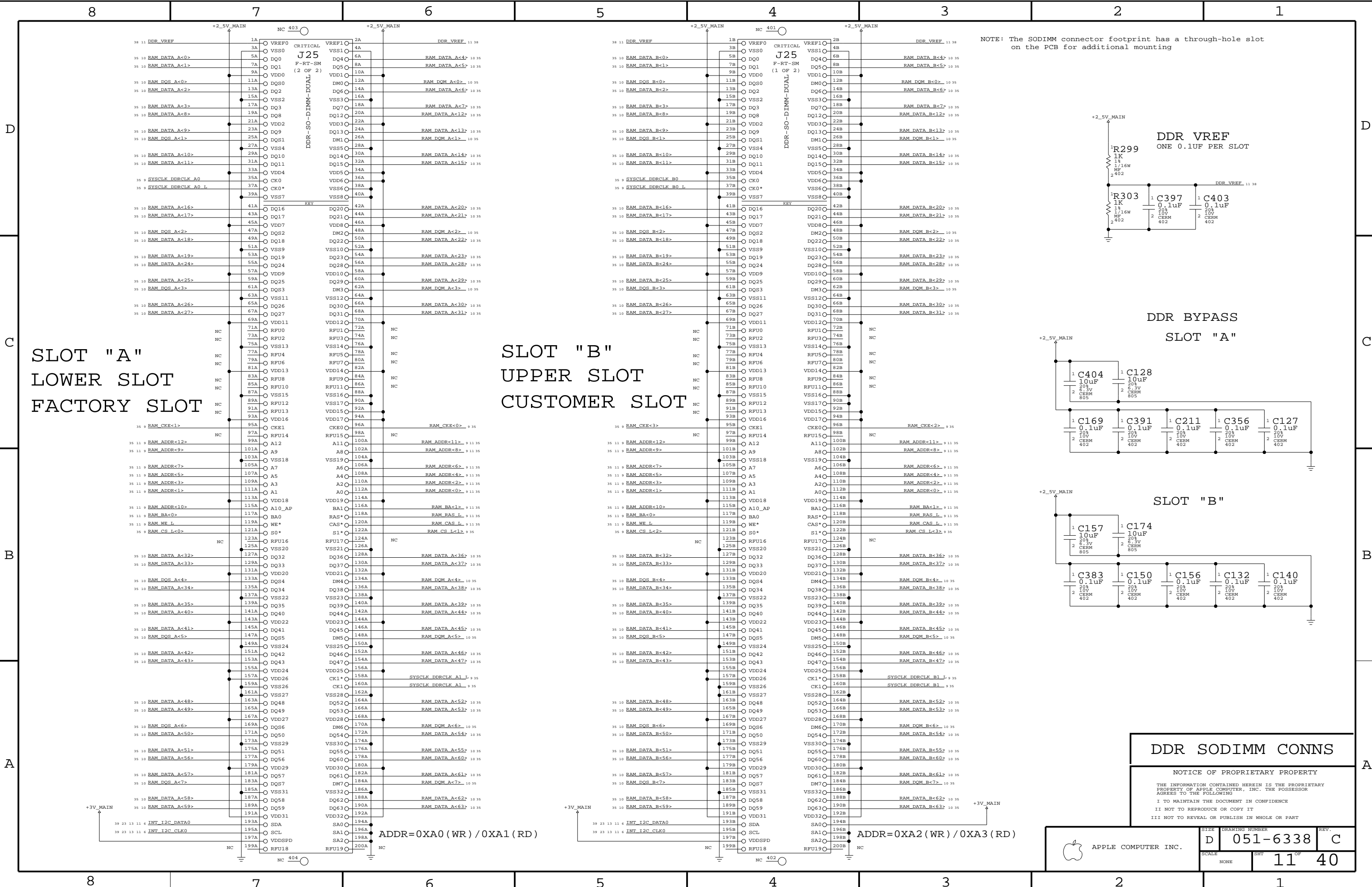
SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

16BIT 2:1 DDR MUXES

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NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting

DDR VREF
ONE 0.1uF PER SLOT

DDR BYPASS
SLOT "A"

SLOT "B"

DDR SODIMM CONNS

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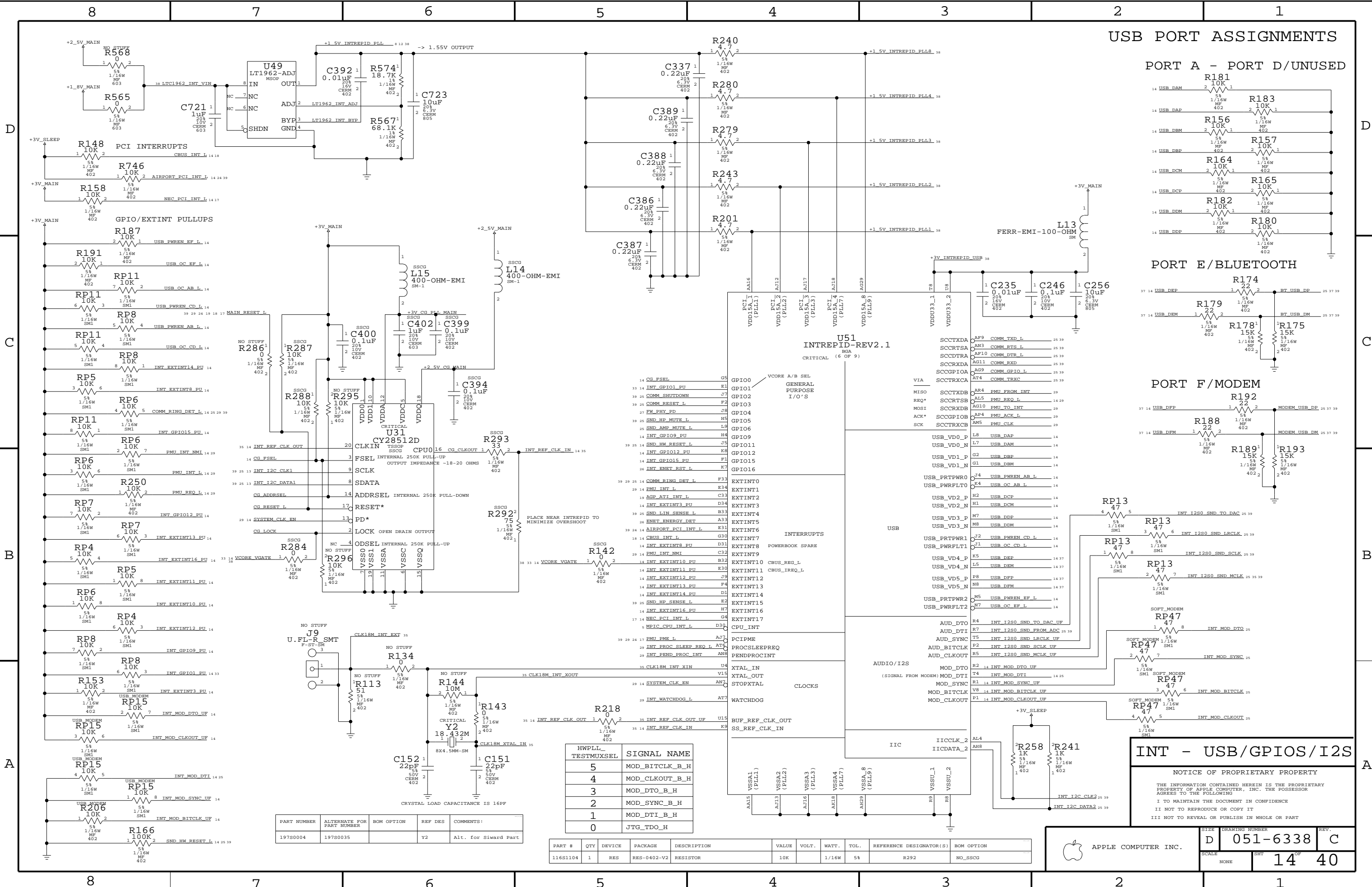


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SIZE: DRAWING NUMBER: REV.

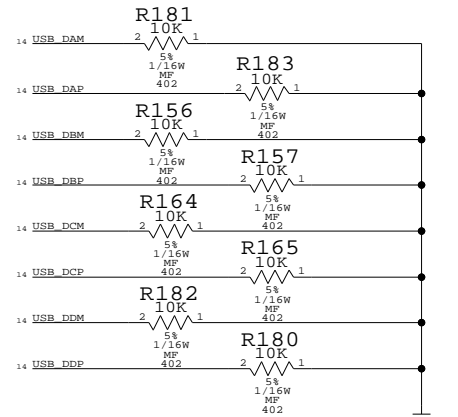
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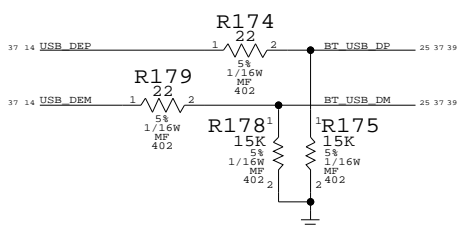


USB PORT ASSIGNMENTS

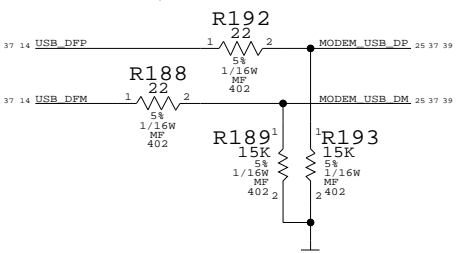
PORT A - PORT D/UNUSED



PORT E/BLUETOOTH



PORT F/MODEM



INT - USB/GPIOS/I2S

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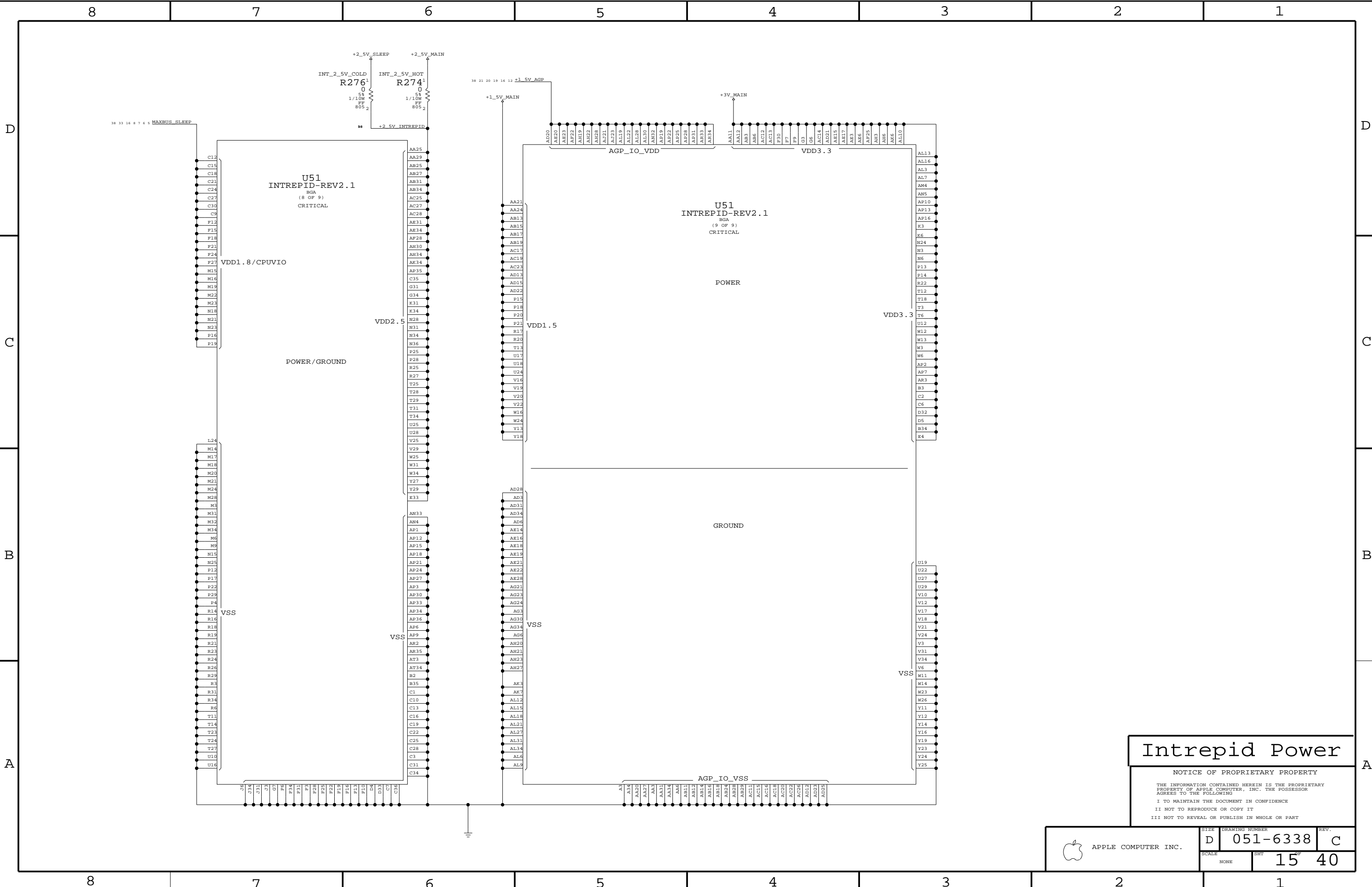
| HWPLL TESTMUXSEL | SIGNAL NAME |
|------------------|----------------|
| 5 | MOD_BITCLK_B_H |
| 4 | MOD_CLKOUT_B_H |
| 3 | MOD_DTO_B_H |
| 2 | MOD_SYNC_B_H |
| 1 | MOD_DTI_B_H |
| 0 | JTG_TDO_H |

| PART # | QTY | DEVICE | PACKAGE | DESCRIPTION | VALUE | VOLT. | WATT. | TOL. | REFERENCE DESIGNATOR(S) | BOM OPTION |
|----------|-----|--------|-------------|-------------|-------|-------|-------|------|-------------------------|------------|
| 116S1104 | 1 | RES | RES-0402-V2 | RESISTOR | 10K | | 1/16W | 5% | R292 | NO_SSCG |

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|-------------|---------------------------|------------|---------|----------------------|
| 19780004 | 19780035 | | Y2 | Alt. for Siward Part |

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Intrepid Power

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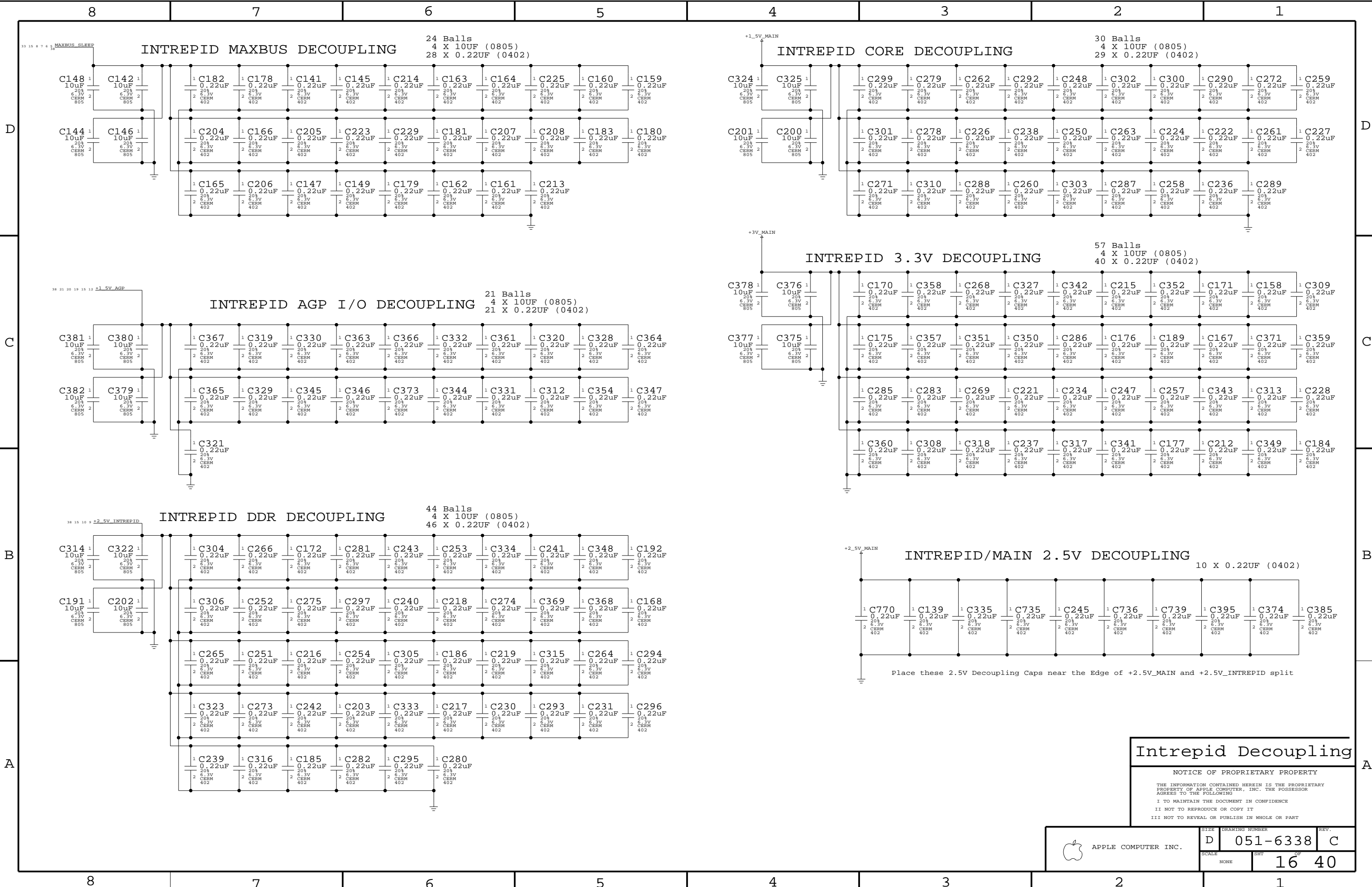
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Intrepid Decoupling

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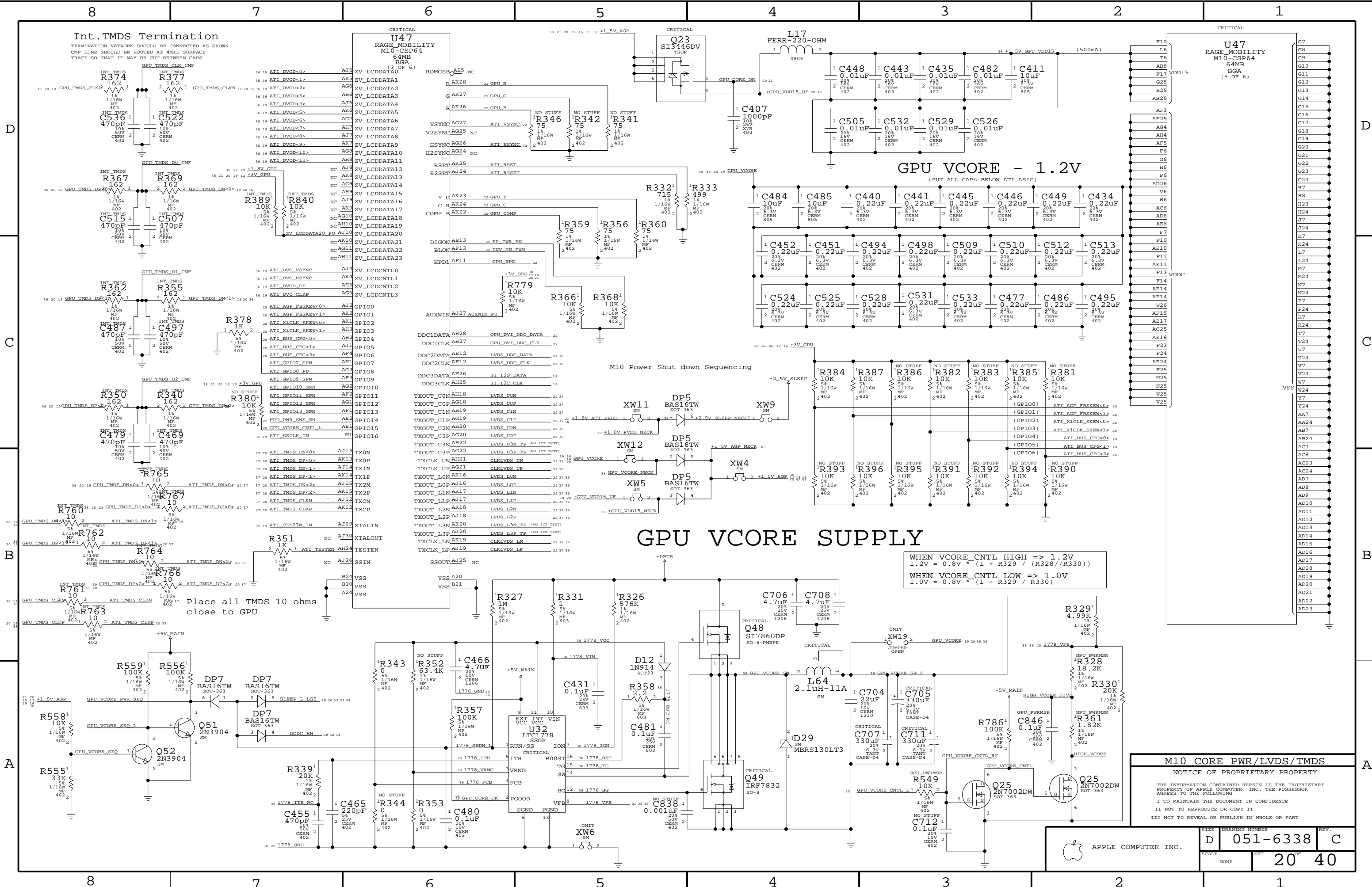
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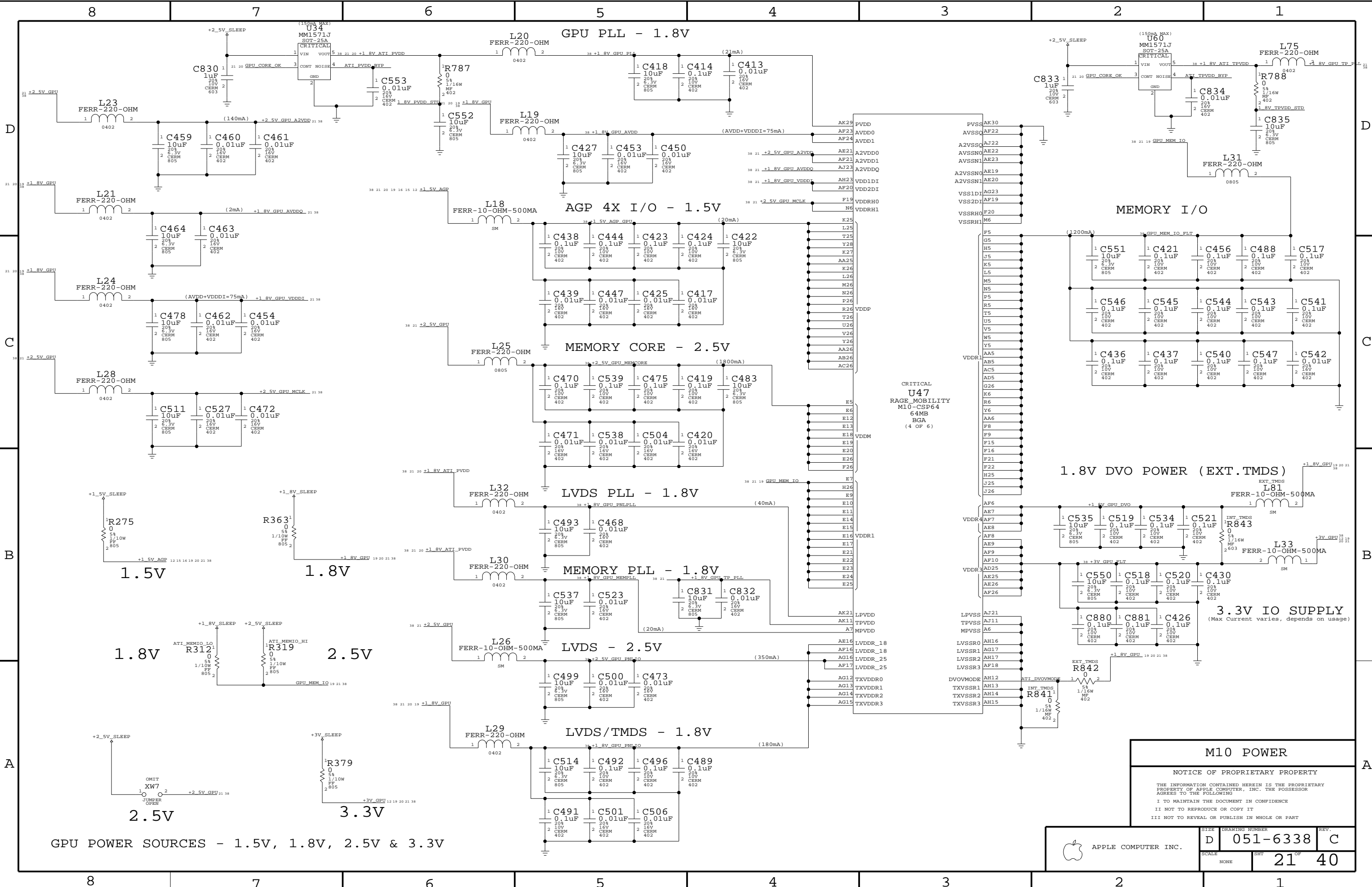
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GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

M10 POWER

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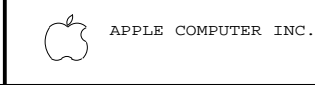
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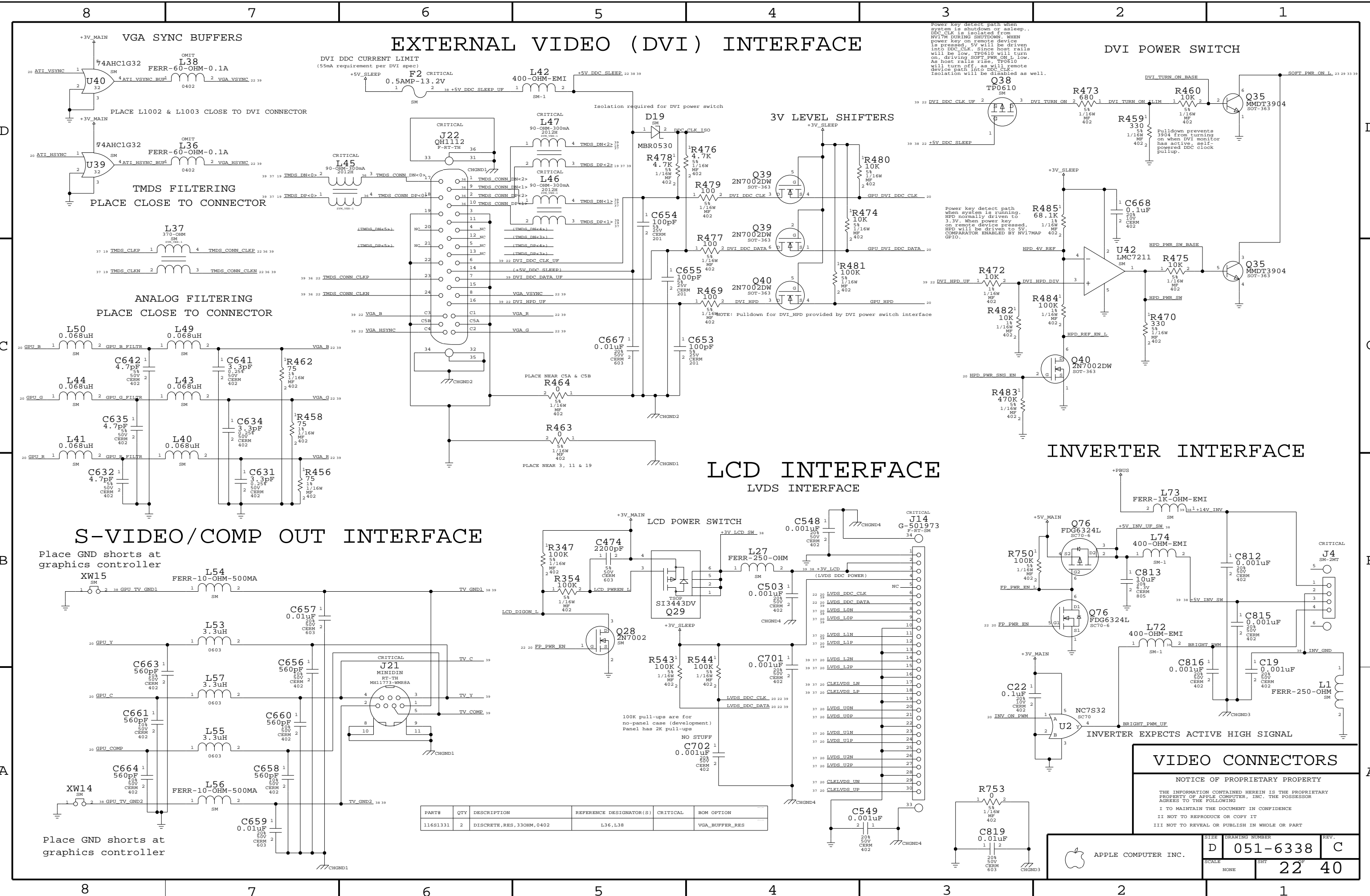
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

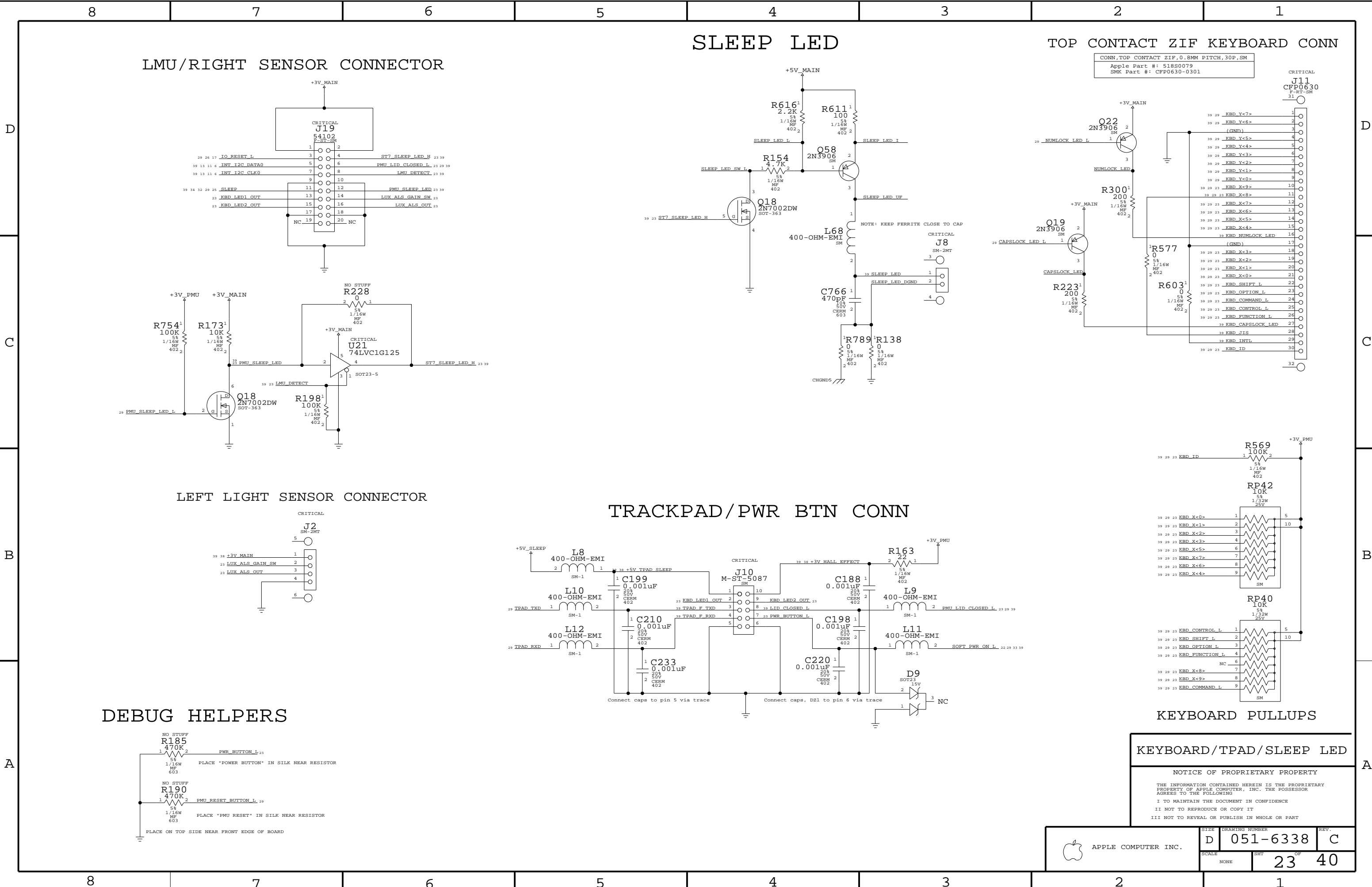
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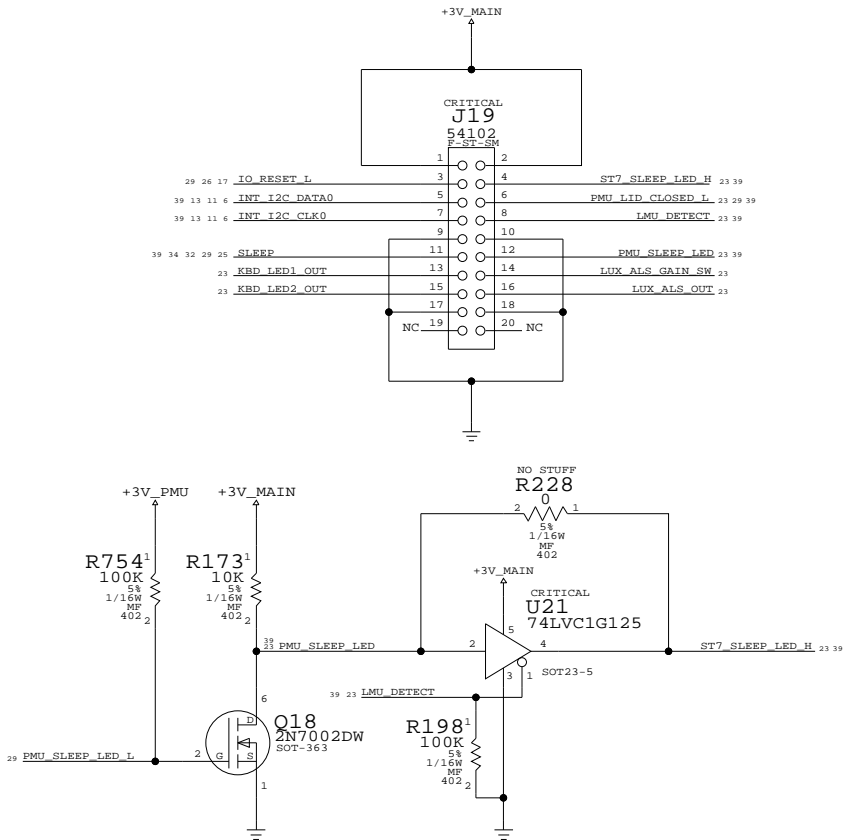
| | | |
|-------|----------------|----------|
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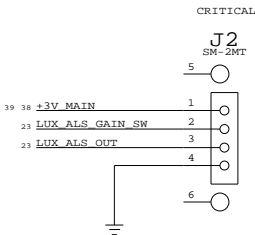




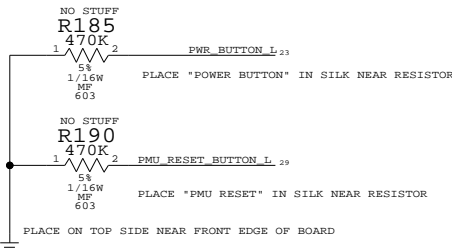
LMU/RIGHT SENSOR CONNECTOR



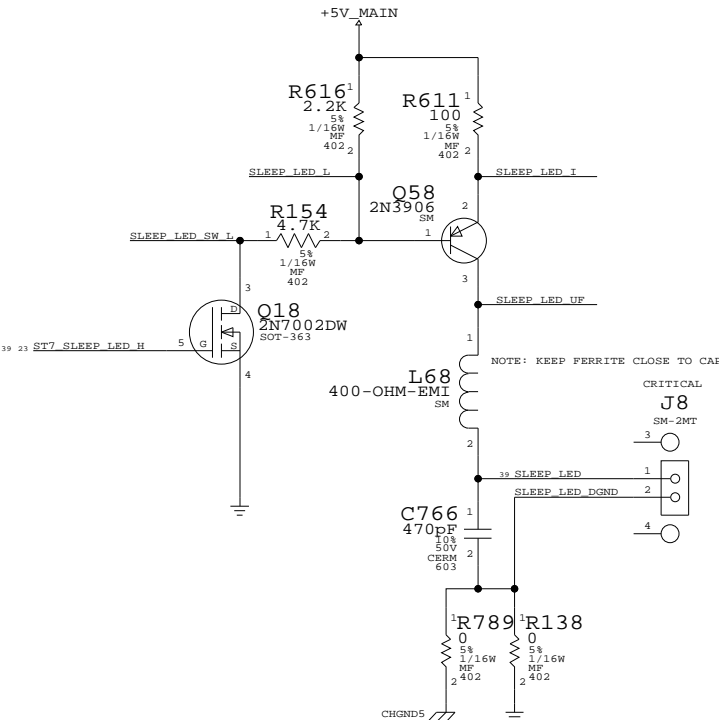
LEFT LIGHT SENSOR CONNECTOR



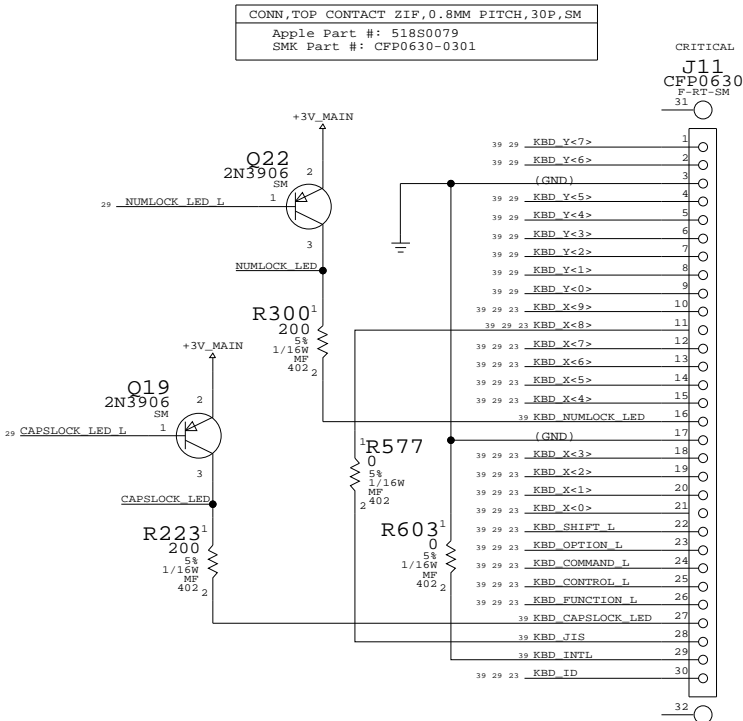
DEBUG HELPERS



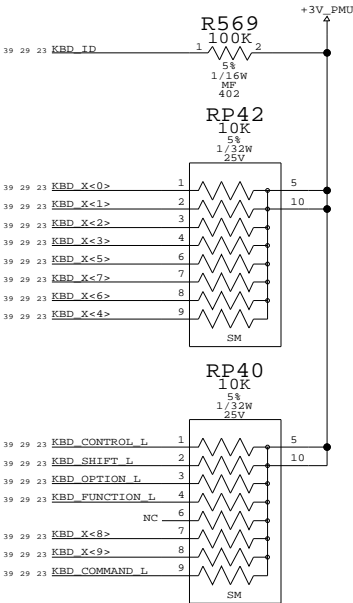
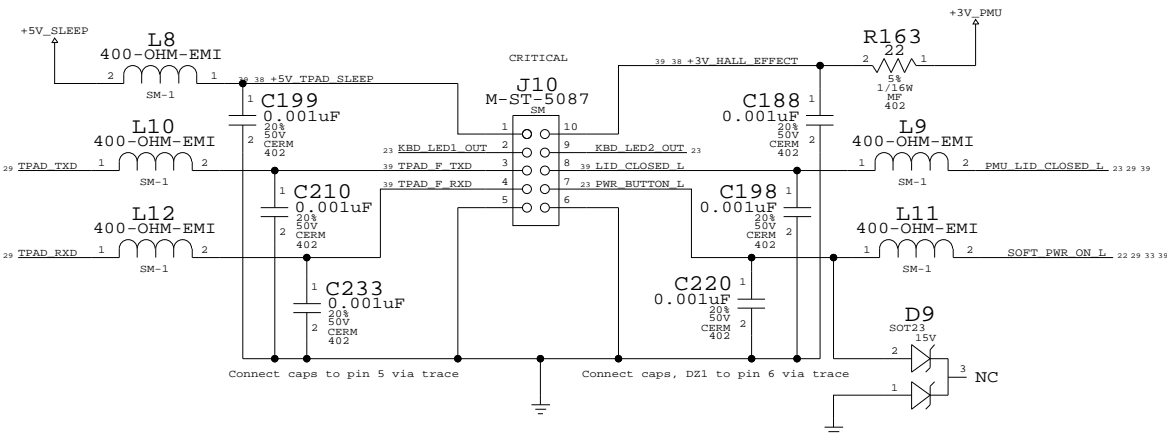
SLEEP LED



TOP CONTACT ZIF KEYBOARD CONN



TRACKPAD/PWR BTN CONN



KEYBOARD PULLUPS

KEYBOARD/TPAD/SLEEP LED

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LEFT I/O & AUDIO BOARD (LIO)

USB MODEM/SOFT MODEM

RIGHT USB BOARD

SERIAL DEBUG INTERFACE

FAN INTERFACE FAN CONTROLLER

FAN/MODEM/SOUND/BACKUP BATT.

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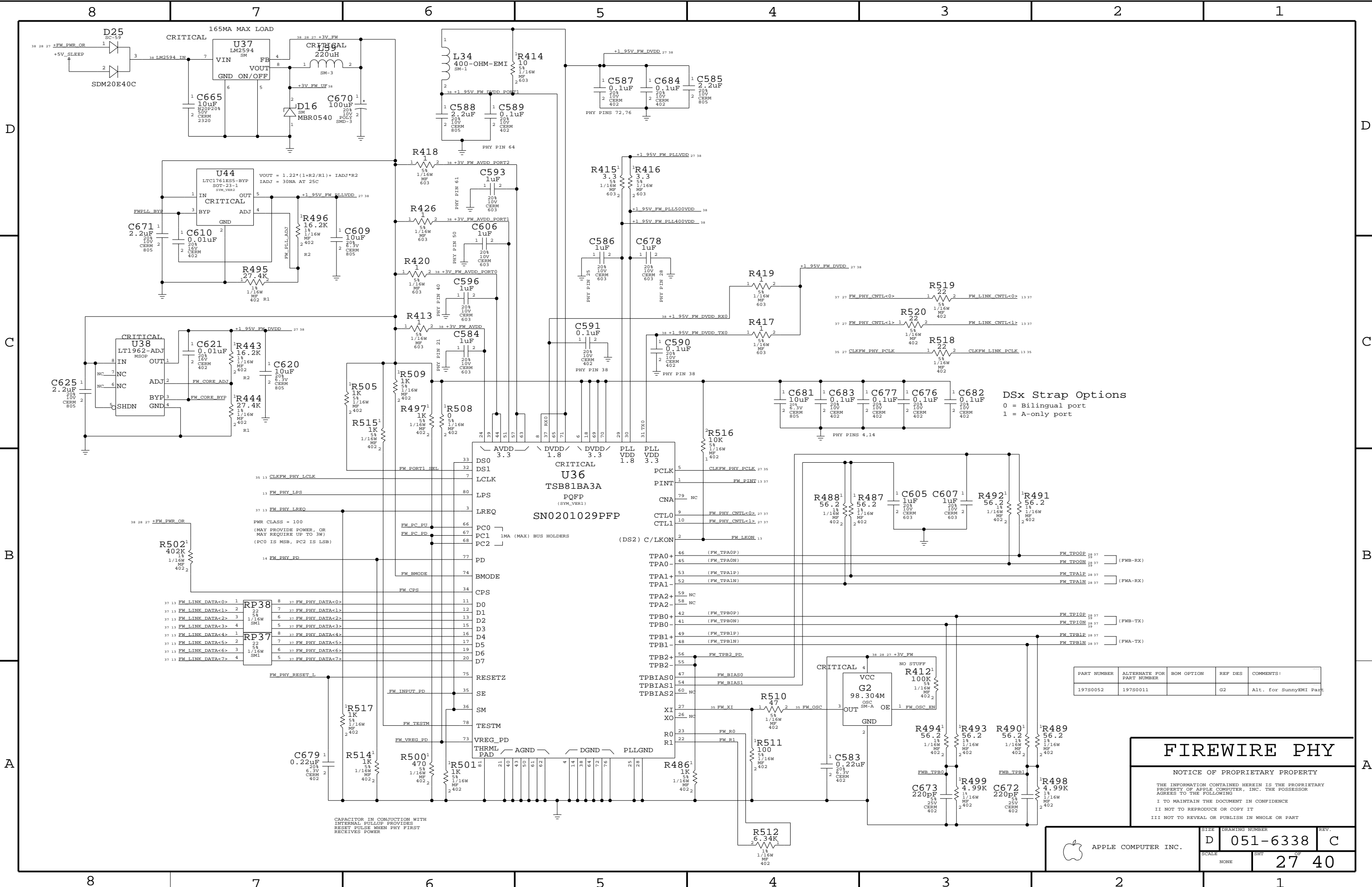
B

B

A

A

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|--|-------------------------|----------|------------|
| 516S0154 | 1 | CONN,PLUG,0.5MM PITCH,1.5MM STACK,40P,GOLD | J3 | CRITICAL | ? |



| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|-------------|---------------------------|------------|---------|------------------------|
| 197S0052 | 197S0011 | | G2 | Alt. for SunnyEMI Part |

FIREWIRE PHY

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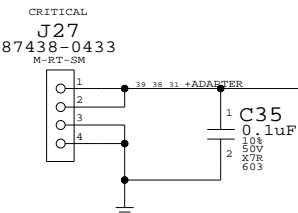
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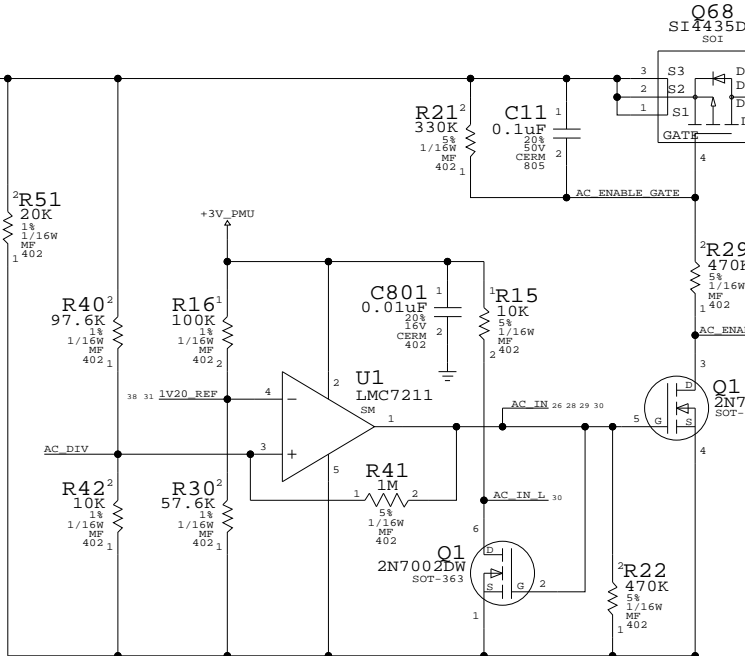
| | | | |
|---------------------|------|----------------|-------|
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| | D | 051-6338 | C |
| SCALE | NONE | | SHEET |
| | 27 | | 40 |

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

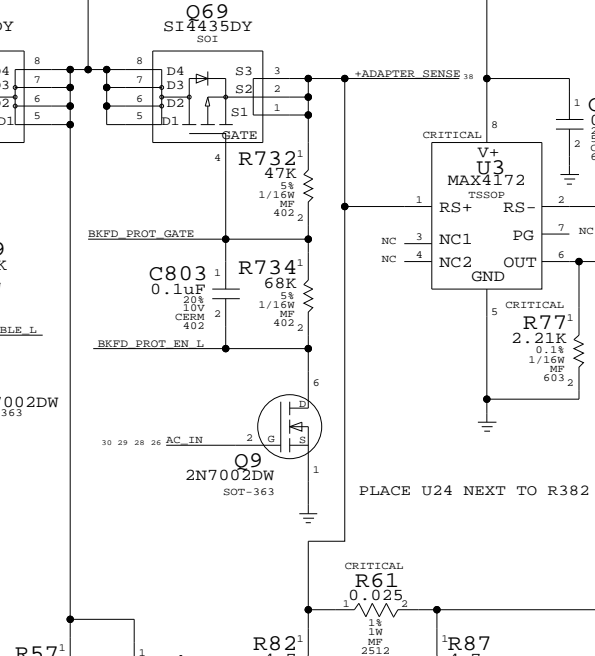


DC INRUSH LIMITER

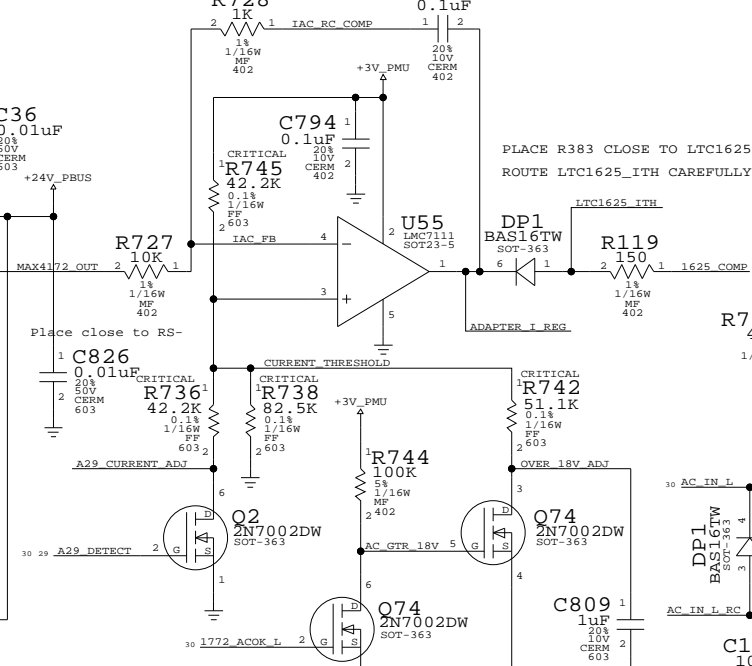


GREATER THAN 13.1V DETECT

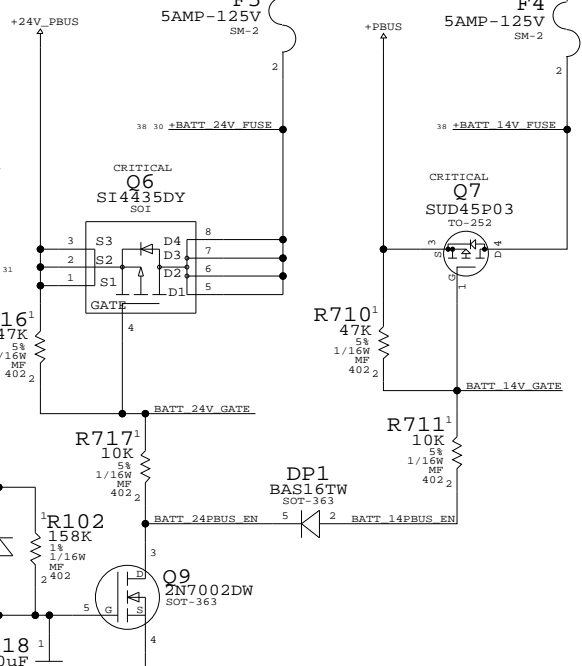
BACKFEED PROTECTION



+PBUS CURRENT LIMIT



BATTERY SWITCH-OVER CIRCUIT

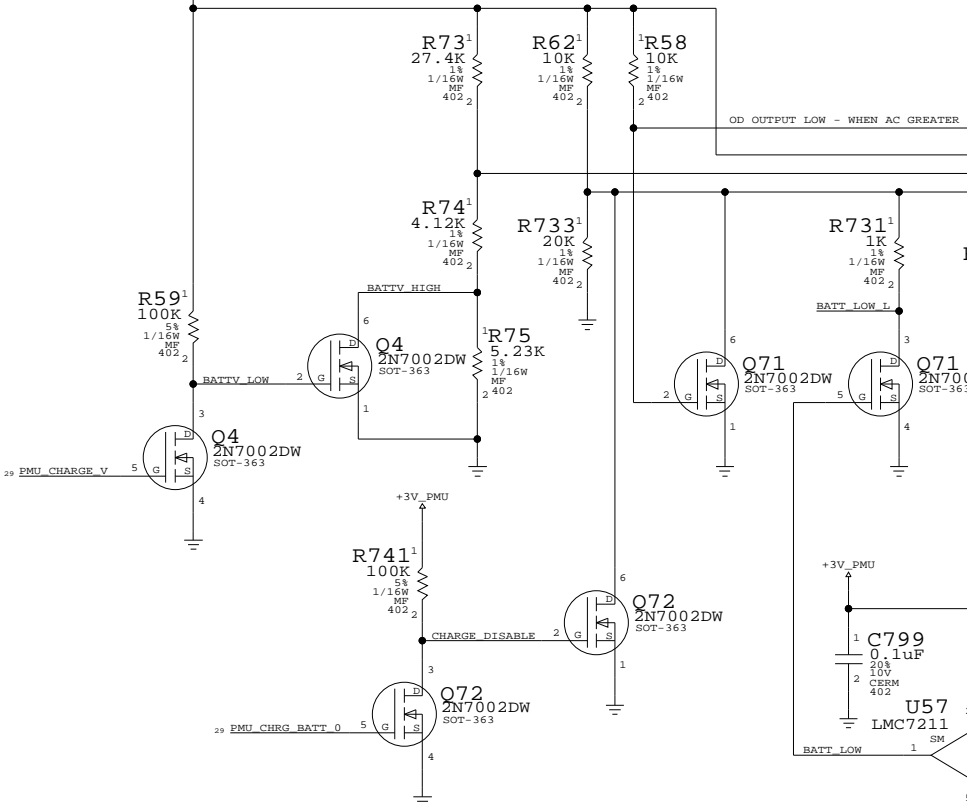


SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE



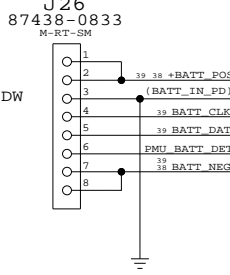
$$V_{BATT} = CELLS \times (4.096 + (0.4096 \times V_{VCTL} / V_{REFIN}))$$

For 4.15V cells, VCTL = 0.123 REFIN
For 4.20V cells, VCTL = 0.245 REFIN

$$I_{CHG} = (0.2048 / R_{g2}) \times (V_{ICTL} / V_{REFIN})$$

BATTERY CONNECTOR

87438-0833

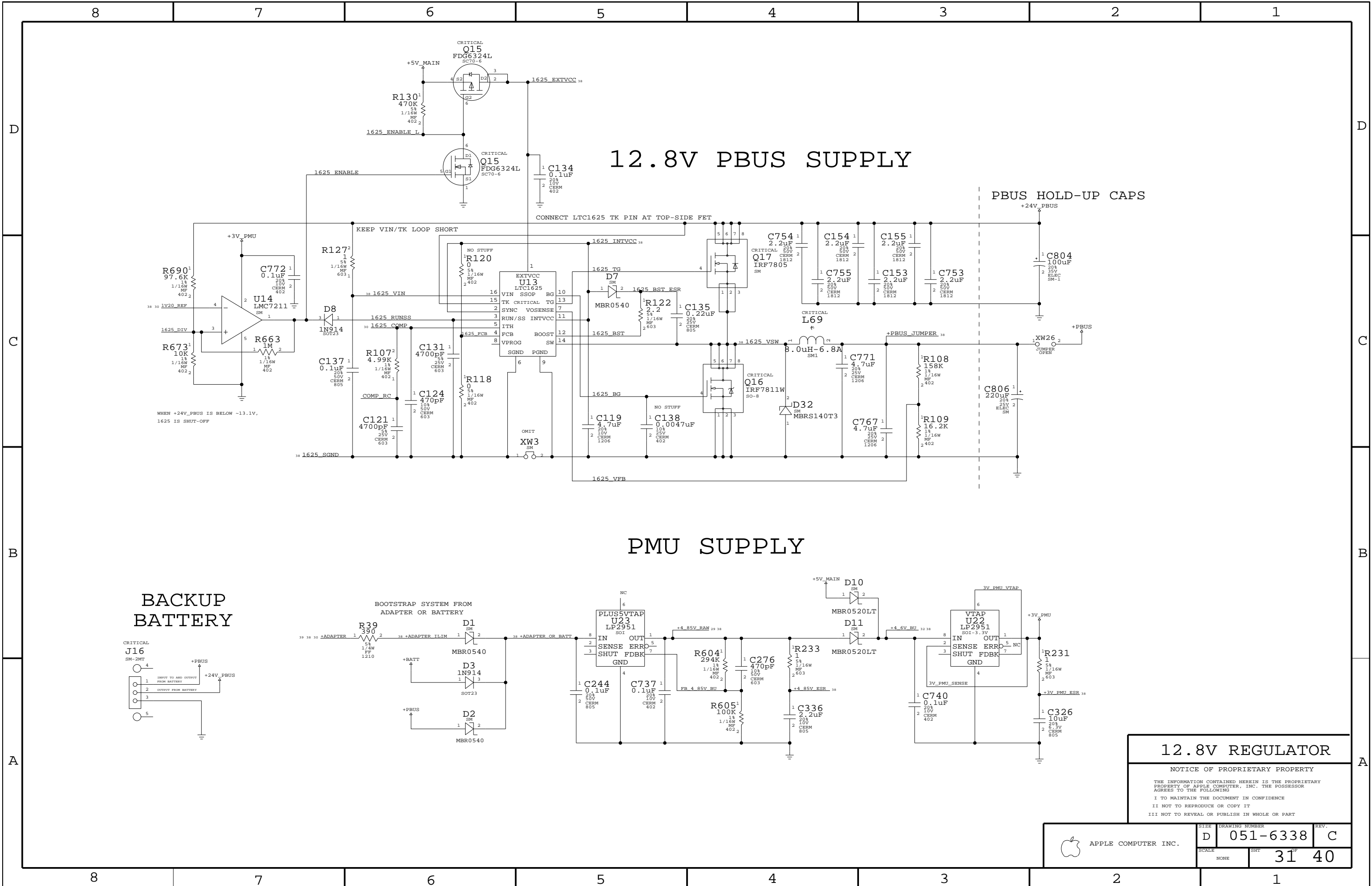


BATTERY CHARGER

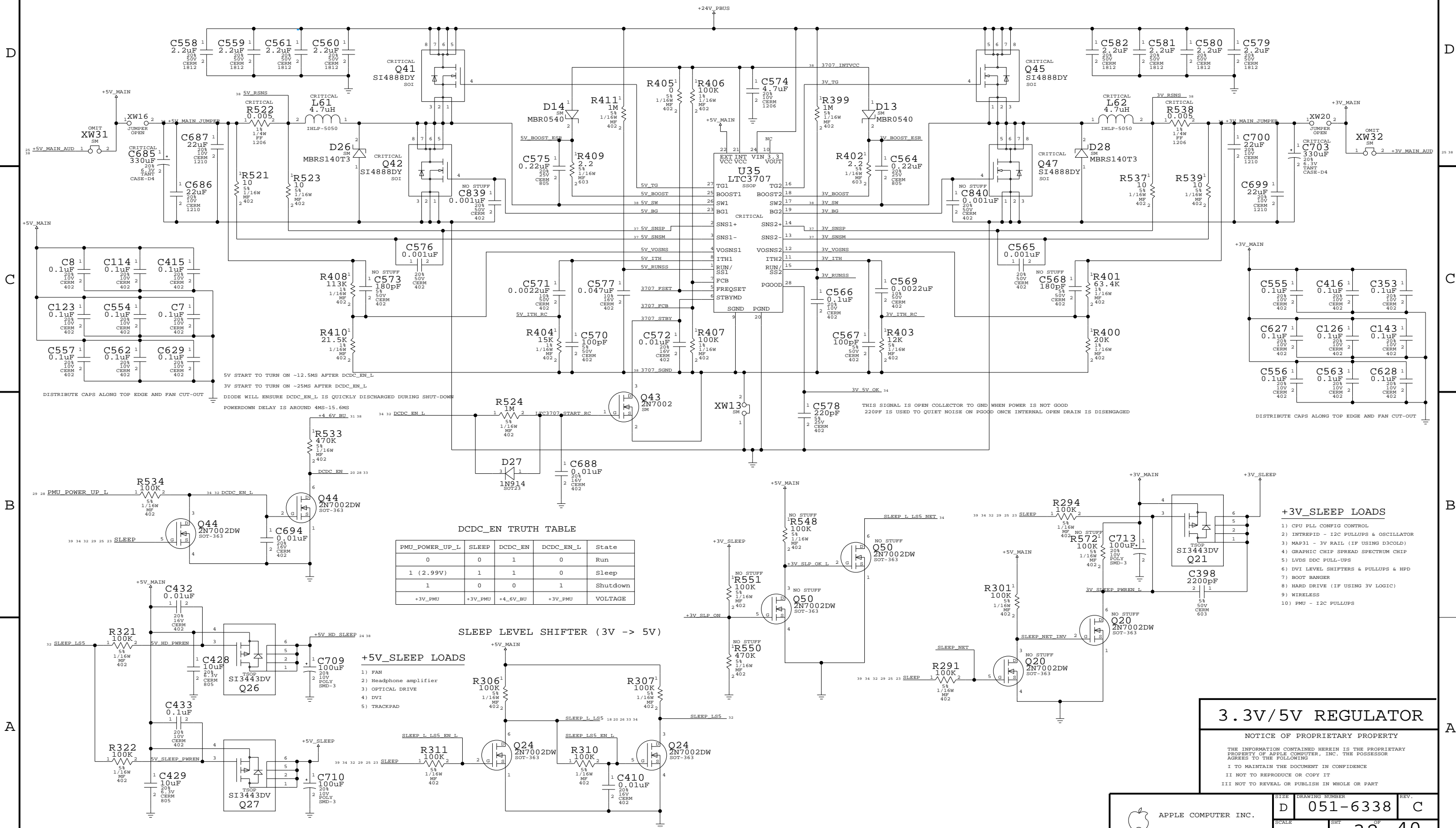
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|---------------------|------|----------------|-------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-6338 | C |
| SCALE | SHT | 30 | OF 40 |



3.3V/5V MAIN SUPPLY



| DCDC_EN TRUTH TABLE | | | | |
|---------------------|---------|---------|-----------|----------|
| PMU_POWER_UP_L | SLEEP | DCDC_EN | DCDC_EN_L | State |
| 0 | 0 | 1 | 0 | Run |
| 1 (2.99V) | 1 | 1 | 0 | Sleep |
| 1 | 0 | 0 | 1 | Shutdown |
| +3V_PMU | +3V_PMU | +4V_BU | +3V_PMU | VOLTAGE |

SLEEP LEVEL SHIFTER (3V -> 5V)

+5V_SLEEP LOADS

- 1) FAN
- 2) Headphone amplifier
- 3) OPTICAL DRIVE
- 4) DVI
- 5) TRACKPAD

+3V_SLEEP LOADS

- 1) CPU PLL CONFIG CONTROL
- 2) INTREPID - I2C PULLUPS & OSCILLATOR
- 3) MAP31 - 3V RAIL (IF USING D3COLD)
- 4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
- 5) LVDS DDC PULL-UPS
- 6) DVI LEVEL SHIFTERS & PULLUPS & HPD
- 7) BOOT BANGER
- 8) HARD DRIVE (IF USING 3V LOGIC)
- 9) WIRELESS
- 10) PMU - I2C PULLUPS

3.3V/5V REGULATOR

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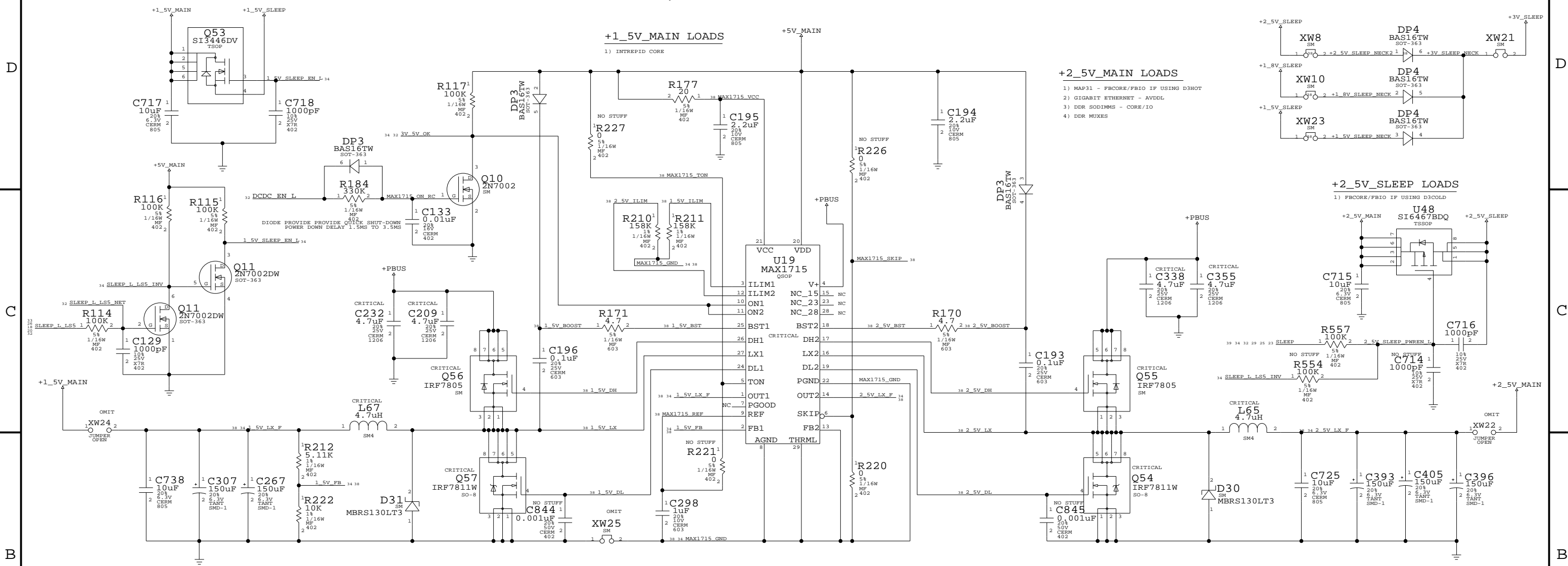
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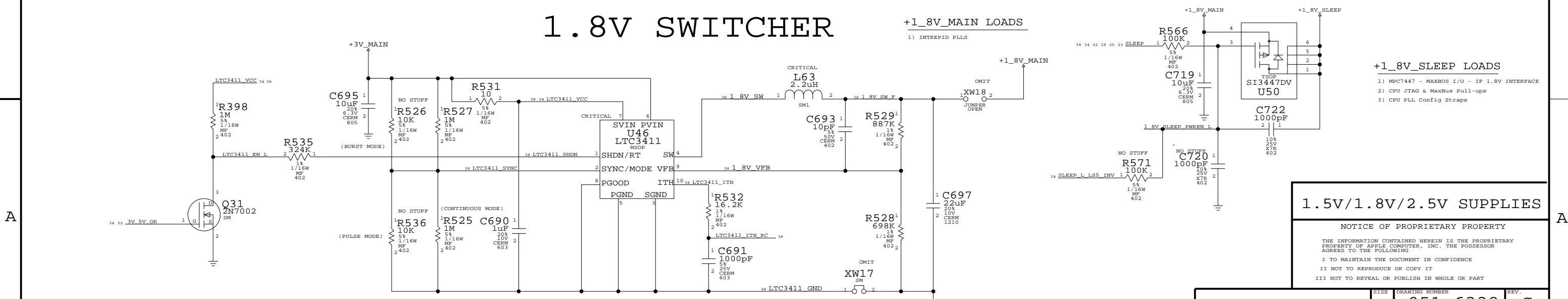
APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|-------|----------------|------|
| D | 051-6338 | C |
| SCALE | SHT | OF |
| NONE | 32 | 40 |

1.5V/2.5V SWITCHER



1.8V SWITCHER



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|---------------------|----------------|----------|------|
| APPLE COMPUTER INC. | DRAWING NUMBER | | REV. |
| | D | 051-6338 | C |
| SCALE | | SHT | 40 |
| NONE | | | |

| Digital Signals (cont'd) | | | | | | | | | | Differential Signals | | | | | | | | | |
|--------------------------|---------------|------------------------|----------------------------|--------------------|-------------|------------------|----------------------------|-------------|------------------|----------------------|------------------|-------------------------------|-------------------------------|---------------------------|------------------|-----------------|----------|----------|--|
| GROUP | SIG_NAME | PROPAGATION_DELAY | MAX_VIAS | MAX_EXPOSED_LENGTH | STUB_LENGTH | NET_SPACING_TYPE | NO_TEST | PULSE_PARAM | | GROUP | SIG_NAME | DIFFERENTIAL_PAIR | RELATIVE_PROPAGATION_DELAY | MAX_EXPOSED_LENGTH | NET_SPACING_TYPE | MAX_VIAS | | | |
| D | AGP | AGP_AD<15..0> | L:S:1:050:1450 | 7 | | | | 66 MHZ | 12 19 | FIREWIRE Zo = 110 | FW_TP10N | FW_TP10 | FW_TP10:G:L:S:0 MIL:5 MIL | 500.0000 | 110 OHM SPACING | | 27 28 39 | | |
| | | AGP_CBE<1..0> | L:S:1:050:1450 | 7 | | | | 66 MHZ | 12 19 | | FW_TP10P | FW_TP10 | FW_TP10:G:L:S:0 MIL:5 MIL | 500.0000 | 110 OHM SPACING | | 27 28 39 | | |
| | | AGP_AD_STB<0> | L:S:1:050 MTL:1450 MTK | | | (250) | 8 MIL SPACING | | 133.0 MHZ | | 12 19 | FW_TP00N | FW_TP00 | FW_TP00:G:L:S:0 MIL:5 MIL | 500.0000 | 110 OHM SPACING | | 27 28 39 | |
| | | AGP_AD_STB<1> | L:S:1:050 MTL:1450 MTK | | | (250) | 8 MIL SPACING | | 133.0 MHZ | | 12 19 | FW_TP00P | FW_TP00 | FW_TP00:G:L:S:0 MIL:5 MIL | 500.0000 | 110 OHM SPACING | | 27 28 39 | |
| | | AGP_AD_STB<2> | L:S:1:050 MTL:1450 MTK | | | (250) | 8 MIL SPACING | | 66 MHZ | | 12 19 | FW_TP01N | FW_TP01 | FW_TP01:G:L:S:0 MIL:5 MIL | 500.0000 | 110 OHM SPACING | | 28 | |
| | | AGP_AD_STB<3> | L:S:1:050 MTL:1450 MTK | | | (250) | 8 MIL SPACING | | 66 MHZ | | 12 19 | FW_TP01P | FW_TP01 | FW_TP01:G:L:S:0 MIL:5 MIL | 500.0000 | 110 OHM SPACING | | 28 | |
| | | AGP_AD_STB<4> | L:S:1:050 MTL:1450 MTK | | | (250) | 8 MIL SPACING | | 66 MHZ | | 12 19 | FW_TP02N | FW_TP02 | FW_TP02:G:L:S:0 MIL:5 MIL | 500.0000 | 110 OHM SPACING | | 28 | |
| | | AGP_AD_STB<5> | L:S:1:050 MTL:1450 MTK | | | (250) | 8 MIL SPACING | | 66 MHZ | | 12 19 | FW_TP02P | FW_TP02 | FW_TP02:G:L:S:0 MIL:5 MIL | 500.0000 | 110 OHM SPACING | | 28 | |
| | | AGP_AD_STB<6> | L:S:1:050 MTL:1450 MTK | | | (250) | 8 MIL SPACING | | 66 MHZ | | 12 19 | FW_TP03N | FW_TP03 | FW_TP03:G:L:S:0 MIL:5 MIL | 500.0000 | 110 OHM SPACING | | 28 | |
| | | AGP_AD_STB<7> | L:S:1:050 MTL:1450 MTK | | | (250) | 8 MIL SPACING | | 66 MHZ | | 12 19 | FW_TP03P | FW_TP03 | FW_TP03:G:L:S:0 MIL:5 MIL | 500.0000 | 110 OHM SPACING | | 28 | |
| | AGP SIDE BAND | AGP_SBA<7..0> | L:S:1:050:1450 | 7 | | | | | 66 MHZ | 12 19 | FW_TPA1P | FW_TPA1 | FW_TPA1:G:L:S:0 MIL:4 | 500.0000 | 110 OHM SPACING | | 27 28 | | |
| | | AGP_SB_STB | L:S:1:050 MTL:1450 MTK | | | (350) | 8 MIL SPACING | | 66.00 MHZ | 12 19 | FW_TPB1N | FW_TPB1 | FW_TPB1:G:L:S:0 MIL:4 | 500.0000 | 110 OHM SPACING | | 27 28 | | |
| | | AGP_SB_STB_L | L:S:1:050 MTL:1450 MTK | | | (350) | 8 MIL SPACING | | 66.00 MHZ | 12 19 | FW_TPB1P | FW_TPB1 | FW_TPB1:G:L:S:0 MIL:4 | 500.0000 | 110 OHM SPACING | | 27 28 | | |
| | | AGP_FRAME_L | L:S:1:250 MTL:1950 MTK | | | | | | 66.00 MHZ | 12 19 | FW_TPI1N | FW_TPI1 | FW_TPI1:G:L:S:0 MIL:4 | 500.0000 | 110 OHM SPACING | | 28 39 | | |
| | | AGP_TRDY_L | L:S:1:250 MTL:1950 MTK | | | | | | 66.00 MHZ | 12 19 | FW_TPI1P | FW_TPI1 | FW_TPI1:G:L:S:0 MIL:4 | 500.0000 | 110 OHM SPACING | | 28 39 | | |
| | | AGP_TRDY_L | L:S:1:250 MTL:1950 MTK | | | | | | 66.00 MHZ | 12 19 | FW_TPO1N | FW_TPO1 | FW_TPO1:G:L:S:0 MIL:4 | 500.0000 | 110 OHM SPACING | | 28 39 | | |
| | | AGP_DEVSEL_L | L:S:1:250 MTL:1950 MTK | | | | | | 66.00 MHZ | 12 19 | FW_TPO1P | FW_TPO1 | FW_TPO1:G:L:S:0 MIL:4 | 500.0000 | 110 OHM SPACING | | 28 39 | | |
| | | AGP_STOP_L | L:S:1:250 MTL:1950 MTK | | | | | | 66.00 MHZ | 12 19 | MDI_P<0> | ENET_MD10 | ENET_MD10:G:L:S:0 MIL:100 MIL | 500.0000 | 110 OHM SPACING | | 26 39 | | |
| | | AGP_PAR | L:S:1:250 MTL:1950 MTK | | | | | | 66.00 MHZ | 12 19 | MDI_M<0> | ENET_MD10 | ENET_MD10:G:L:S:0 MIL:100 MIL | 500.0000 | 110 OHM SPACING | | 26 39 | | |
| | | AGP_REQ_L | L:S:1:250 MTL:1950 MTK | | | | | | 66.00 MHZ | 12 19 | MDI_P<1> | ENET_MD11 | ENET_MD11:G:L:S:0 MIL:100 MIL | 500.0000 | 110 OHM SPACING | | 26 39 | | |
| PCI | AGP_GNT_L | L:S:1:250 MTL:1950 MTK | | | | | | 66.00 MHZ | 12 19 | MDI_M<1> | ENET_MD11 | ENET_MD11:G:L:S:0 MIL:100 MIL | 500.0000 | 110 OHM SPACING | | 26 39 | | | |
| | AGP_RBF_L | L:S:1:250 MTL:1950 MTK | | | | | | 66.00 MHZ | 12 19 | MDI_P<2> | ENET_MD12 | ENET_MD12:G:L:S:0 MIL:100 MIL | 500.0000 | 110 OHM SPACING | | 26 39 | | | |
| | PCI_AD<31..0> | L:S:6000:12500 | | | | MIN DAISY CHAIN | | 33 MHZ | 9 12 17 18 24 39 | MDI_M<2> | ENET_MD12 | ENET_MD12:G:L:S:0 MIL:100 MIL | 500.0000 | 110 OHM SPACING | | 26 39 | | | |
| | PCI_CBE<3..0> | L:S:6000:12500 | | | | MIN DAISY CHAIN | | 33 MHZ | 12 17 18 24 | MDI_P<3> | ENET_MD13 | ENET_MD13:G:L:S:0 MIL:100 MIL | 500.0000 | 110 OHM SPACING | | 26 39 | | | |
| | PCI_FRAME_L | L:S:6000 MTL:12500 MTL | | | | MIN DAISY CHAIN | | 33.00 MHZ | 12 17 18 24 39 | MDI_M<3> | ENET_MD13 | ENET_MD13:G:L:S:0 MIL:100 MIL | 500.0000 | 110 OHM SPACING | | 26 39 | | | |
| | PCI_TRDY_L | L:S:6000 MTL:12500 MTL | | | | MIN DAISY CHAIN | | 33.00 MHZ | 12 17 18 24 39 | CLKLVDS_LN | CLKLVDS_L | LVDS:G:L:S:0 MIL:110 MIL | 500.0000 | 100 OHM SPACING | 4 | 20 22 39 | | | |
| | PCI_TRDY_L | L:S:6000 MTL:12500 MTL | | | | MIN DAISY CHAIN | | 33.00 MHZ | 12 17 18 24 39 | CLKLVDS_LP | CLKLVDS_L | LVDS:G:L:S:0 MIL:110 MIL | 500.0000 | 100 OHM SPACING | 4 | 20 22 39 | | | |
| | PCI_DEVSEL_L | L:S:6000 MTL:12500 MTL | | | | MIN DAISY CHAIN | | 33.00 MHZ | 12 17 18 24 39 | LVDS_L0N | LVDS_L0 | LVDS:G:L:S:0 MIL:110 MIL | 500.0000 | 100 OHM SPACING | | 20 22 39 | | | |
| | PCI_STOP_L | L:S:6000 MTL:12500 MTL | | | | MIN DAISY CHAIN | | 33.00 MHZ | 12 17 18 24 39 | LVDS_L0P | LVDS_L0 | LVDS:G:L:S:0 MIL:110 MIL | 500.0000 | 100 OHM SPACING | | 20 22 39 | | | |
| | PCI_PAR | L:S:6000 MTL:12500 MTL | | | | MIN DAISY CHAIN | | 33.00 MHZ | 12 17 18 24 39 | LVDS_L1N | LVDS_L1 | LVDS:G:L:S:0 MIL:110 MIL | 500.0000 | 100 OHM SPACING | | 20 22 39 | | | |
| C | ULTRA ATA-100 | UIDE_DATA<15..8> | L:S:1:710 | | | (200) | | 100 MHZ | 13 24 | UPPER | LVDS_L1P | LVDS_L1 | LVDS:G:L:S:0 MIL:110 MIL | 500.0000 | 100 OHM SPACING | | 20 22 39 | | |
| | | UIDE_DATA<7> | U:S:1:V:R:P:19.3:1:600 MTL | | | (200) | | 100.0 MHZ | 13 24 | | LVDS_L2N | LVDS_L2 | LVDS:G:L:S:0 MIL:110 MIL | 500.0000 | 100 OHM SPACING | | 20 22 39 | | |
| | | UIDE_DATA<6..0> | L:S:1:600 | | | (200) | | 100 MHZ | 13 24 | | LVDS_L2P | LVDS_L2 | LVDS:G:L:S:0 MIL:110 MIL | 500.0000 | 100 OHM SPACING | | 20 22 39 | | |
| | | UIDE_ADDR<2..0> | L:S:1:650 | | | (200) | NEED TO MATCH DELAY TO 250 | 100 MHZ | 13 24 | | CLKLVDS_UN | CLKLVDS_U | LVDS:G:L:S:0 MIL:110 MIL | 500.0000 | 100 OHM SPACING | 4 | 20 22 | | |
| | | UIDE_RST_L | L:S:1:400 MTL | | | (200) | | 100.0 MHZ | 13 24 | | CLKLVDS_UP | CLKLVDS_U | LVDS:G:L:S:0 MIL:110 MIL | 500.0000 | 100 OHM SPACING | 4 | 20 22 | | |
| | | UIDE_DIOW_L | L:S:1:400 MTL | | | (200) | | 100.0 MHZ | 13 24 | | LVDS_U0N | LVDS_U0 | LVDS:G:L:S:0 MIL:110 MIL | 500.0000 | 100 OHM SPACING | | 20 22 | | |
| | | UIDE_DIOR_L | L:S:1:600 MTL | | | (200) | 10 MIL SPACING | 100.0 MHZ | 13 24 | | LVDS_U0P | LVDS_U0 | LVDS:G:L:S:0 MIL:110 MIL | 500.0000 | 100 OHM SPACING | | 20 22 | | |
| | | UIDE_DMAC_L | L:S:1:400 MTL | | | (200) | | 100.0 MHZ | 13 24 | | LVDS_U1N | LVDS_U1 | LVDS:G:L:S:0 MIL:110 MIL | 500.0000 | 100 OHM SPACING | | 20 22 | | |
| | | UIDE_CS0_L | L:S:1:500 MTL | | | (200) | | 100.0 MHZ | 13 24 | | LVDS_U1P | LVDS_U1 | LVDS:G:L:S:0 MIL:110 MIL | 500.0000 | 100 OHM SPACING | | 20 22 | | |
| | | UIDE_CS1_L | L:S:1:500 MTL | | | (200) | | 100.0 MHZ | 13 24 | | LVDS_U2N | LVDS_U2 | LVDS:G:L:S:0 MIL:110 MIL | 500.0000 | 100 OHM SPACING | | 20 22 | | |
| | EIDE | UIDE_DMARQ | L:S:1:400 MTL | | | (200) | | | 100.0 MHZ | 13 | TMD5 Zo = 100 | LVDS_U2P | LVDS_U2 | LVDS:G:L:S:0 MIL:110 MIL | 500.0000 | 100 OHM SPACING | | 20 22 | |
| | | UIDE_IOCHRDY | L:S:1:600 MTL | | | (200) | 10 MIL SPACING | 100.0 MHZ | 13 24 | TMDS_CLKN | | CLKTMDS | TMDS:G:L:S:0 MIL:50 MIL | 500.0000 | 100 OHM SPACING | 5 | 19 22 | | |
| | | UIDE_INTRO | L:S:1:400 MTL | | | (200) | | 100.0 MHZ | 13 | TMDS_CLKP | | CLKTMDS | TMDS:G:L:S:0 MIL:50 MIL | 500.0000 | 100 OHM SPACING | 5 | 19 22 | | |
| | | HD_DATA<15..0> | L:S:5000:6500 | 7 | | (200) | | 100 MHZ | 24 | TMDS_DN<0> | | TMDS_D0 | TMDS:G:L:S:0 MIL:50 MIL | 500.0000 | 100 OHM SPACING | 8 | 19 22 39 | | |
| | | HD_ADDR<2..0> | L:S:5000:6500 | 7 | | (200) | | 100 MHZ | 24 | TMDS_DP<0> | | TMDS_D0 | TMDS:G:L:S:0 MIL:50 MIL | 500.0000 | 100 OHM SPACING | 8 | 19 22 39 | | |
| | | HD_RESET_L | L:S:4000 MTL:6000 MTL | | | (200) | TOTAL UIDE+HD SKEW <500MIL | 100.0 MHZ | 24 | TMDS_DN<1> | | TMDS_D1 | TMDS:G:L:S:0 MIL:50 MIL | 500.0000 | 100 OHM SPACING | 8 | 19 22 39 | | |
| | | HD_DIOW_L | L:S:3000 MTL:5200 MTL | | | (200) | | 100.0 MHZ | 24 | TMDS_DP<1> | | TMDS_D1 | TMDS:G:L:S:0 MIL:50 MIL | 500.0000 | 100 OHM SPACING | 8 | 19 22 39 | | |
| | | HD_DIOR_L | L:S:6100 MTL:6150 MTL | | | (200) | 10 MIL SPACING | 100.0 MHZ | 24 | TMDS_DN<2> | | TMDS_D2 | TMDS:G:L:S:0 MIL:50 MIL | 500.0000 | 100 OHM SPACING | 8 | 19 22 39 | | |
| | | HD_DMAC_L | L:S:4500 MTL:6000 MTL | | | (200) | | 100.0 MHZ | 24 | TMDS_DP<2> | | TMDS_D2 | TMDS:G:L:S:0 MIL:50 MIL | 500.0000 | 100 OHM SPACING | 8 | 19 22 39 | | |
| | | HD_CS0_L | L:S:3000 MTL:6000 MTL | | | (200) | | 100.0 MHZ | 24 | ATI_TMDS_CLKN | | ATI_CLKTMDS | ATITMDS:G:L:S:0 MIL:50 MIL | 200.0000 | 100 OHM SPACING | 5 | 20 | | |
| EIDE INTREPID | HD_CS1_L | L:S:3000 MTL:6000 MTL | | | (200) | | | 100.0 MHZ | 24 | ATI_TMDS_CLKP | ATI_CLKTMDS | ATITMDS:G:L:S:0 MIL:50 MIL | 200.0000 | 100 | | | | | |

| | | | | | | | | |
|--|--|---|---|---|---|---|---|---|
| | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| | REVISION HISTORY | | | | | | | |
| | Proto Release | | | | | | | |
| | 7/22/02 - Initial acquisition of schematic (from 051-6278 Rev 01) Added P59 80-DIMM connector as placeholder (p.12) Added P59 LVDS connector as placeholder (p.22) Changed J9 to 10 pin Elco connector for modem (p.25) Changed PBUS holdup caps to P59 electrolytic cans (p.30) | | | | | | | |
| | 7/23/02 - Removed L3 (p.8) Replaced processor with 360 pin Apollo (p.5,6) 7/24/02 - Added P68 Between battery and PBUS rails for airline power (p.29) 8/10/02 - Added USB 2.0 (p.18) | | | | | | | |
| | 8/20/02 - Removed spare pullup straps for Intrepid (p.9) Removed USB overcurrent protection [to be placed on other boards] (p.18) Changed right USB board connector to 16 pin Hirose connector (p.26) Changed L10 board connector to 40 pin Molex connector (p.26) Added 6 bypass caps to MAXBUS_SLEEP and CPU_VCORE_SLEEP (p.5) | | | | | | | |
| | 8/26/02 - Removed 32 bypass caps for +3V MAIN at Intrepid (p.16) Removed 5 bypass caps for +2.5V MAIN at Intrepid (p.6) Removed 3 bypass caps for +1.5V AGP at Intrepid (p.16) Removed 4 bypass caps for MAXBUS_MAIN at Intrepid (p.16) | | | | | | | |
| | 8/27/02 - Changed main battery connector to BP24067-R1, which is close to final (p.29) | | | | | | | |
| | 8/29/02 - Added dedicated Boot Banger circuit (p.6) Added 5 bypass caps to each 80-DIMM connector (p.11) Added quad voltage circuit for bus slewing architecture (p.32) | | | | | | | |
| | 8/30/02 - Changed to low profile 32.768kHz crystal for PMU (p.28) Changed to Q11 adapter detection scheme (p.28) | | | | | | | |
| | 9/03/02 - Corrected upper LVDS single pin nets (p.20) Removed unintentional extra pulldown resistor at Intrepid (p.14) | | | | | | | |
| | 9/17/02 - Numerous changes to stay in sync with P84 (all) | | | | | | | |
| | 9/18/02 - Changed battery connector back to P84 part (p.29) Added LMU circuitry to eliminate extra board (p.23) Changed to P84 dual channel LVDS connector to reduce 12R cable losses(p.22) | | | | | | | |
| | 9/19/02 - Removed unnecessary battery fets (due to 3S only design) (p.29) Modified chassis gnds on some components (all) Corrected battery connector [same as P84] (p.29) Removed P93 support (p.25) Removed second fuse from FW ports [single fuse provides adequate power] (p.27) | | | | | | | |
| | 9/23/02 - Replaced BCM5421 with Marvell 88E1111 (p.26) Increased MAX_VIA_COUNT by two on most nets with this constraint for uVia (p.34,35) | | | | | | | |
| | 9/27/02 - Corrected cpu, memory bus constraints to match manhattan lengths (p.34) Swapped pins on L33, L35 for layout (p.31) Changed V6 to smaller foot factor crystal (p.26) | | | | | | | |
| | 9/30/02 - Changed J19 (DC-in) to proper 4-pin connector (p.29) Corrected holes and chassis gnds (p.4,all) | | | | | | | |
| | 10/01/02 - Removed Intrepid 1.x specific circuitry (p.13) 10/03/02 - Numerous pin-swaps to accomodate board layout (all) 10/08/02 - Added caps for functional test points (p.37) | | | | | | | |
| | 10/09/02 - Changed 16 pin connectors (modem and right USB) to Foxconn parts (p.23) 10/10/02 - Changed NCL pins high per documentation (p.17) Added 10K pullup to CG_ADDRSEL and 10K pulldown to CG_FSEL on CY28512 (p.14) Added SSCQ/NO_SSCQ stuffing options for CY28512 circuit (p.14) Removed CPU_VCORE pullup to 5V to eliminate potential 3V/5V current path (p.32) Added second FW port power fuse (p.27) Removed INT_CPUFB_IN cap per P84 (p.8) Replaced INT_FET2 Fets with TSPF8133 battery charger and 14V PBUS switchers (p.29,30) Renamed optical interface for consistency (p.24,37) Corrected PLL_CKREF for Apollo 7 (needed to make keys be zero) (p.5,7) Removed temporary P84 constraints and finished up AGP clock changes (p.12,34) Added stuffing options to power fans off 3V or 5V (p.25) | | | | | | | |
| | 10/11/02 - Replaced DVI EMI caps with 0201 versions (p.22) | | | | | | | |
| | 10/14/02 - Changed J18 to RJ45 with integrated magnetics (p.26) 10/15/02 - Moved FireWire connectors and port power switch to separate page (p.28) Changed SMBus pullups to 7.15k, 1k as per 1Books/P84 [involved component net swaps] (p.29) Added 0603 resistors as shorting pads for power up and reset (p.45) Changed INT_MOD_SYNC, INT_MOD_DTI and INT_MOD_BITCLK to pulldowns per ERS [LA clk not used] (p.14) Added damping resistor option to LMU crystal (p.23) Changed INT_FST_FLEEN_PD to pulldown only [LA CLK not used] (p.13) Removed FW_LKON from Intrepid EXTINT3 [no longer used], pullup added (p.14) Changed BNRMS_HRES to 3V_SLEEP (p.24) Changed FW_PC_PD, FW_PC_PU resistors to 5s (p.27) Added 1K pulldown and net FW_PD2 to FW_PHY (p.27) | | | | | | | |
| | 10/16/02 - Implemented new FW power switch and current limit (p.28) Added +14V PBUS to +PBUS (p.all) Added +PBUS current limiting circuit, removed battery charging current limit circuit (p.30) Changed FW_PHY pin 081 to make Port 1 1394s only (p.27) | | | | | | | |
| | 10/21/02 - Updated CY28512 clock chip to Rev B (p.14) Added full support for non-zero CPU_FLL_CFG4s in run state (p.7) Changed FW_PHY pin 081 to make Port 1 1394s only (p.27) | | | | | | | |
| | 10/22/02 - Changed LMU/sleep LED interface per P84 (p.23) 10/23/02 - Changed LMU/JTAG/J22 pinout/pullup/pulldown strategy per P84 (p.23) Changed fan fets to S14460V per P84 (p.25) Pinned out audio connector (p.25) Pinned out right USB connector (p.25) Pinned out modem connector (p.25) Added 2 functional test points to wireless connector (p.24,38) Renamed FW low voltage power rails (p.27,37) P84 (p.33) Renamed Vcore VID nets to be consistent with P84 (p.33) Removed redundancy in DDR memory constraints (p.35) Changed FW DDI strap to pullup to sleep off port (p.27) Cleaned up CY28512B circuit as per P84 [powered off main, output divider and strap tweaks] (p.14) Updated PCI clock series B values per P84 (p.23) Changed power rail for A10 to +5V_SLEEP and for GPU VDDOVD per P84 (p.21,37) Split FW_VEND into FW_VEND1 and FW_VEND2 (p.28,37) Added TP nets to GPU for XOR-tree testing (p.19-21) Removed fan PWM output pullups to +5V_SLEEP and for PWM power supply (p.25) | | | | | | | |
| | 10/28/02 - Added FW thermal pad ground hole back in (p.27) | | | | | | | |
| | 10/30/02 - Changed fan power rails to common net (p.25) | | | | | | | |
| | 10/31/02 - Added wireless RF_DISABLE_L pullup and AIRPORT_CLKRUN_L pulldown (p.24) | | | | | | | |
| | 11/05/02 - Added 6 decoupling caps to CPU_VCORE_SLEEP (p.5) Broke out quad OR-gate to discrete components for better placement (p.22,29) | | | | | | | |
| | 11/06/02 - Changed 10 uF FW current limit output cap to two 4.7 uF caps (p.28) Added 3 decoupling caps to CPU_VCORE_SLEEP (p.4) Added 9 decoupling caps to each of +5V_MAIN and +3V_MAIN (p.32) Removed C017, jumper for CPU_VCORE_SLEEP (p.35) Added decoupling cap to PMU reset OR gates (p.29) Changed FireWire PHY to Z17 (p.27) Added bulk caps to fan connectors (p.25) Added alternate chassis gnd connection for sleep LED (p.23) | | | | | | | |
| | 11/11/02 - Removed +3V_MAIN option for P50 card (p.24) 11/13/02 - Removed LMU and associated circuitry (p.23) 11/14/02 - Implemented D3cold for all PCI devices (p.12,14,18) 11/25/02 - Renamed all components (all pages) 11/26/02 - Removed chokes from 1394s data pairs (p.27,28) | | | | | | | |
| | EVT RELEASE | | | | | | | |
| | 12/13/02 - Added 12 pF caps to source of 33MHz PCI clocks since they can not be buried (p.12) Replaced ALM1031 with AD7460 [12C Address Changes] (p.25) Added AD7460 hookups to GPU thermal diode (p.2,1,25) Added FireWire B ESD protection circuits (p.28) Removed hole from FireWire ground pad (p.7) DDR memory connector renamed to J25 (p.11) Removed J4210 from FireWire port power (p.28) Added F10,F20 as placeholders and experiment guides (p.28) Added diodes to OR +5V_SLEEP into FW_PHY power supply (p.27) 12/26/02 - Updated CPU p/ns to production p/ns (p.5) Updated PCI source clock and internal upFeading straps (p.8) Changed bootROM FWD signal to INT_RESET_L per P84 (p.9) Added C82 pulldowns per P84 (p.9) Updated ethernet series Rs per P84 [Clocks to 10 ohms, data to 22 ohms] (p.13) Updated SSCQ/NO_SSCQ BOM option (p.14) Renamed line-in and headphone sense lines to reflect active low signals (p.14,25,39) Added 0 ohm Rs to make 2.5V Intrepid rail hot or cold (p.15,16,38) NO STUFFED entire 1.5V LDO circuit (p.15) Stuffed USB OC1/FP0N filters for 0 Ohm constant [due to new port current limiters] (p.17) Renamed USB OC1/FP0N signals for left/right ports (p.17,39) Updated GPU VCore to stay in sync with P84 [jitter improvement] (p.20) Added EMI caps to LVDS_DDC_CLK, INT_I2S0_SND_MCLK, INT_I2S0_SND_SCLK per P84 (p.22,25) Added R800,R801 for eventual thermal diode in CPU (p.25) Renamed R2000 to R789, R2001 to R802, R2002 to R803 (p.25) Renamed F10 to F1, F20 to F2 [deleted old F1,F2] (p.28) Added caps to FW EMI circuit that were missed (p.28) Changed MAX4172 power source to save current on battery [per P84] (p.30) Updated 1.5V/2.5V switcher BOM to stay in sync with P84 [FET change and current limits] (p.34) Replaced all 132S1061 [1uF,0805,10V,20s] with 132S0046 [1uF,0603,10V,20s] (p.14,15,27,30,33,34) Replaced all 138S0251 [1uF,0603,6.3V,10s] with 132S0046 [1uF,0603,10V,20s] (p.27,30) Updated FireWire fuse topology to that of P84 (p.28) Updated system and power block diagrams (p.2,3) 01/03/03 - Corrected +2.5V_INTREPID connections to muxes and reference (p.9,10) 01/07/03 - Added NO_TEST nets to pads of DDR connector arms (p.11) 01/08/03 - Added ZNF002 circuits to ensure speakers are muted during power-up (p.25) Changed R164 to 511 ohms to avoid low CPU clock amplitude (p.8) 01/09/03 - Added required pulldown to output of DVI_HPD sense comparator (p.22) Swapped R443 and R444 values to ensure Vgs < -4.5V (p.28) Updated S-video filter values to those of P84 (p.22) 01/10/03 - ZT7,ZT23,ZT61,ZT76,ZT89,ZT87,ZT22,ZT38,ZT60,ZT42 & ZT17 are changed to HOLE-VIA-20R10 (p.4) 01/13/03 - Add L53, L54, L55 for TMDS Data<0+2> Diff Pair (p.22) 01/14/03 - Add C821 - C821 (total 10 0.22uF caps) for 2.5V Intrepid Decoupling (p.16) Add C822 & C823 at Wireless Card connector MAIN_RESET_L & RF_DISABLE_L_SPN (p.24) Change MATCHED_DELAY to 50 for all TMDS DIFF PAIR (p.37) Change MATCHED_DELAY to 50 for all TMDS DIFF PAIR (p.37) Add R810 & R811 for ALWAYS-ON FANS in Acrylic Build (p.25) Remove NV31/17 components (p.19-21) 01/28/03 - Add M10 (p.19-21) 02/07/03 - Add Power Net Constraints for M10 (p.38) Replace Singing PBUS Cap C49,C50,C67,C68,C80,C81,C95,C96,C108,C109,C120,C121 with 12600035 (or alt. 1260036) (p.33) 02/11/03 - Add FW Power Net Constraints (p.38) Change signal constraints for AGP signals (p.36) Add LMU connector and components (p.23) Edit I2C table for LMU (p.13) Change R580 to 19.6k (p.14) Connect Clock Slewing RESET# to MAIN_RESET_L (p.14) Change Ferrite Bead of ATI power supply to correct values (p.21) Remove C141 PBUS CAP (p.31) 02/12/03 - Change and Rotate Keyboard Connector (p.23) Add ATI Power sequencing Circuit for M10 Power-up and Power-down (p.19-22, p.32-35) | | | | | | | |
| | EVT RELEASE (continue) | | | | | | | |
| | 02/13/03 - Add C825 (p.30) 02/17/03 - Rename all Reference Designators | | | | | | | |
| | EVT ENCLOSURE RELEASE | | | | | | | |
| | 03/13/03 - Change 3-P FAN connectors to 4-P (p.25) Add PU at PMU_SLEEP_LED_L for LMU (p.23) Change stuffing option for clock slewing (p.25) Change ATI M10 GPIO8 to Pull-down (p.20) Remove Memory_MUX 0ohm Resistors (p.10) | | | | | | | |
| | 03/28/03 - Due to MLB outline change at DVI connector, CHGN01 has to be melted into CHGN1 & CHGN2 (P 4 & 22) Separate +3V and +5V traces running from 3/5V supply to 40Pin LIO connector (P 25 & 32) R601 change from 100K to 4.7K (P 29) Change airline detect to 13.1V or greater, R40 and R690 to 97.6K ohm (P 30 & 31) Add C826 at U3 RS3 - pin (P 30) Change D3 to 1N914 PN Junction Diode(P 31) | | | | | | | |
| | 03/31/03 - Change AGPTSTRT Pull-up to 470hm (it was 400hm) (P 20) Change C843 10uF Cap to 1206 package part (P 28) Change all 1210 4.7uF to 1206 4.7uF Cap (138S0531) (various pages) Modify FAN circuit to PWM active low signal (P25) | | | | | | | |
| | 04/08/03 - Add SOFT MODEM support (P 14 & 25) Add 10-pin ELCO connector for Serial Debug Interface (P 25) Change Q1 from S144350V to SUD45P03-10 (P 30) Remove U34 RS3AB (P 30) | | | | | | | |
| | 04/11/03 - Change FW Schottky Diode to a 3A part 371S0159 (P 28) Change PBUS L69 and VCORE L71 inductor (P 31 & 33) Change battery fets to S14460V per P84 (p.25) Change all 6 VCORE Caps to 220uF AL Poly cap 128S0024 (P 33) Add Mitaumi MM1571J regulator to provide 1.8V TPVDD (P 2) Change U34 to Mitaumi MM1571J part for ATI FLL 1.8V rail(P 21) | | | | | | | |
| | 04/16/03 - Add FW Port Shutdown/PowerOn Circuit (P 28) Change the I2C Pull-up for Sound/Modem to 1K ohm (P 14) | | | | | | | |
| | 04/17/03 - Change 3V/5V inductors (152S0137) L61 & L62 (P 32) | | | | | | | |
| | 04/21/03 - Add 12 ICT JTAG TEST PADS (P 39) | | | | | | | |
| | 04/23/03 - Invert ATI GPIO15 signal, no stuff pull-up resistor (P 20) Combine Q35 and Q36 into a Dual Package Part (P 22) SWAP the AD7460 Temperature Sense pair (P 2) Change FW PHY to production part (P 26) | | | | | | | |
| | 04/24/03 - Remove +3V_CBUS_SLEEP and U5, use +3V_SLEEP directly (P 14,18,24) Add 0402 Res between ATI_PVDD/TPVDD rail and 10uF caps for stability purpose (P 21) Add Mitaumi MM1571J regulator to provide 1.8V TPVDD (P 2) Add Sense Resistor to Vcore power rail, remove one 220uF cap <back to EVTA design> (P 33) | | | | | | | |
| | 04/25/03 - Change C826 to 0.01uF 50V Cap (P 30) | | | | | | | |
| | 04/30/03 - No stuff R676 to prevent +3V rail leakage (P 33) | | | | | | | |
| | 05/02/03 - L45,L46,L47 is using Common Mode Choke TDK ACM2012D Part, will replace with ACM2012H Part if available (P 22) | | | | | | | |
| | DVT RELEASE | | | | | | | |
| | 05/21/03 - Swap +PBUS and +24V_PBUS at Backup Battery Connector - J16 (p.31) 05/27/03 - Change Q62 timing specification (p.13) Change Q62 & Q65 to S17860DP part (p.33) Change C843 10uF Cap to 1206 package part (P 28) Enable VCore Burst(Skip) Mode by no stuffing R67 (p.33) Enable VCore Burst Mod by changing R406 & R407 to 100K ohm (p.32) Change Q48 to IRF7832 part (p.20) Change Q49 to IRF7832 part (p.20) Enable CPUCore Burst Mode by changing R358 to 2.2 ohm, no stuffing R344 and stuffing R343 (p.20) Reduce audible noise by changing L64 to 152S0139 (p.20) Change C840,C841,C842,C843,C844,C845 Opt caper near power switchers FETs (p.20, 32 & 34) Change PWM_L Fan Input (both L&R Fans) to +5V_SLEEP pull-up (p.25) Change C840,C841,C842,C843,C844,C845 Opt caper near power switchers FETs (p.20, 32 & 34) 05/30/03 - Change C840,C841,C842,C843,C844,C845 Opt caper near power switchers FETs (p.20, 32 & 34) 06/03/03 - Add CPU Core Voltage offset option circuit (p.33) 06/05/03 - Change FW-B connector to S1450058 with internal shield pins (p.28) 06/06/03 - Add four 0ohm jumper, in case there is no sw support for the multi-stage VCore (p.38) Change the +2.5V sleep FET to reduce Voltage drop on the rail (p.34) 06/12/03 - Change CBUS & USB2 REQ LINE Pullup to +3V_MAIN (p.12) Add 0 ohm at USB AVSS GND (p.17) Change TMDS common mode choke to TDK AMC2012-900H part (p.22) Change HD DMACLK L pullup R213 to 10K (p.24) Add C847,C851 & C852 at ENET CLK for EMC (p.13 & 26) Change Q34 to FDS3672 (p.28) Change Q82 pin#4 connection to system digital GND (p.33) Add C848 150uF cap at J3 for +5V_MAIN USB2 power (p.25) Add C853 1000uF cap at Q64 (p.30) Add RC at AD7460 power rail for noise isolation (p.25) Isolate THERM1 signal at AD7460 by using double inverters for THERM1_OC (p.25) Remove redundant pullup R601 for THERM1_OC (p.29) Remove SMD EMI appling at CHGN05 (p.23) Add additional PWM/GND pins at J17 for R-USB board (p.25) 06/13/03 - New 5001HM connector with 4 through-hole mounting pins (p.11) Change CPU config stuffing option at R63 and R64 (p.7) Stuff R288 for Cypress CLK chip (p.14) Move CBUS PCI_REQ_L back to +3V_SLEEP rail pull-up (p.12) Change the TMDS Termination Resistor values to 162ohm (p.20) Connect C847 at R160.1 (p.13) Add 1000uF caps at AD7460 D+plus/minus pairs (p.25) Add S1182 DVI transmitter to prevent leakage from DVI connector to the system (p.19&20) 06/16/03 - Replace C705,C707,C711,C703 & C685 with part 128S0025 (p.20&32) Remove R271 resistor (p.34) Edit Signal Constraints for TMDS routing and ENET routing (p.36&37) | | | | | | | |
| | DVT2 RELEASE | | | | | | | |
| | 07/06/03 - Change R97 & R98 to 0402 package (p.33) No Stuff R835 (p.19) Change R198 to 100K ohm resistor (p.23) Add Common Mode Choke L77 & L76 at PMB pairs (p.28) Removed current monitoring IC for firewire port power (p.28) Changed RP52,RP53,RP56,RP57 to 22ohm for EMI (p.19) | | | | | | | |
| | PRODUCTION RELEASE | | | | | | | |
| | 07/28/03 - Change BOM option for C51,C52,C77,C78,C91,C92,C111 to 8.2uF Panasonic AL cap only (p. 34) 08/05/03 - Change +3V/5V ITH compensation and No-Stuff Feed Forward Caps (p. 32) Change CPU VCore setting for both BEST and BETTER configurations (p. 33) 08/07/03 - Change CPU VCore setting for both BEST and BETTER configurations again (p. 33) | | | | | | | |
| | PRODUCTION RELEASE (Version C) | | | | | | | |
| | 08/18/03 - Change CPU VCore setting for BEST configuration to: 1.335V(High)->1.080V(Low) (p. 33) | | | | | | | |
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